

FEATURES

Fixed gain of 20 dB
Operational frequency of 1 MHz to 2.7 GHz
Linear output power up to 9 dBm
Input/output internally matched to 50 Ω
Temperature and power supply stable
Noise figure: 5.3 dB
Power supply: 3 V or 5 V

APPLICATIONS

VCO buffers
General Tx/Rx amplification
Power amplifier predrivers
Low power antenna drivers

GENERAL DESCRIPTION

The AD8353 is a broadband, fixed-gain, linear amplifier that operates at frequencies from 1 MHz up to 2.7 GHz. It is intended for use in a wide variety of wireless devices, including cellular, broadband, CATV, and LMDS/MMDS applications.

By taking advantage of ADI's high performance, complementary Si bipolar process, these gain blocks provide excellent stability over process, temperature, and power supply. This amplifier is single-ended and internally matched to 50 Ω with a return loss of greater than 10 dB over the full operating frequency range.

The AD8353 provides linear output power of 9 dBm with 20 dB of gain at 900 MHz when biased at 3 V and an external RF choke is connected between the power supply and the output pin. The dc supply current is 42 mA. At 900 MHz, the output third-order intercept (OIP3) is greater than 23 dBm and is 19 dBm at 2.7 GHz.

FUNCTIONAL BLOCK DIAGRAM

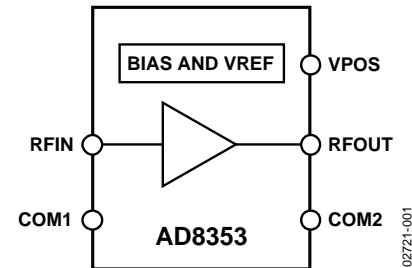


Figure 1.

The noise figure is 5.3 dB at 900 MHz. The reverse isolation (S_{12}) is -36 dB at 900 MHz and -30 dB at 2.7 GHz.

The AD8353 can also operate with a 5 V power supply; in which case, no external inductor is required. Under these conditions, the AD8353 delivers 8 dBm with 20 dB of gain at 900 MHz. The dc supply current is 42 mA. At 900 MHz, the OIP3 is greater than 22 dBm and is 19 dBm at 2.7 GHz. The noise figure is 5.6 dB at 900 MHz. The reverse isolation (S_{12}) is -35 dB.

The AD8353 is fabricated on ADI's proprietary, high performance, 25 GHz, Si complementary, bipolar IC process. The AD8353 is available in a chip scale package that uses an exposed paddle for excellent thermal impedance and low impedance electrical connection to ground. It operates over a -40°C to $+85^{\circ}\text{C}$ temperature range, and an evaluation board is also available.

Rev. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Typical Performance Characteristics	7
Applications.....	1	Theory of Operation	13
Functional Block Diagram	1	Basic Connections.....	13
General Description	1	Applications.....	14
Revision History	2	Low Frequency Applications Below 100 MHz.....	14
Specifications.....	3	Evaluation Board	15
Absolute Maximum Ratings.....	5	Outline Dimensions	16
ESD Caution.....	5	Ordering Guide	16
Pin Configuration and Function Descriptions.....	6		

REVISION HISTORY

12/05—Rev. A to Rev. B

Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Figure 16.....	9
Changes to Figure 32.....	11
Moved Figure 39 to Page 15; Renumbered Sequentially.....	15
Changes to Ordering Guide.....	16

8/05—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Product Title.....	1
Changes to Features, Figure 1, and General Description.....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Figure 2 and Table 4.....	6
Changes to Figure 3 caption and Figure 6 caption.....	7
Changes to Figure 17 caption and Figure 20 caption	9
Changes to Basic Connections Section.....	13
Added Low Frequency Applications Below 100 MHz Section.	14
Changes to Table 5.....	15
Changes to Ordering Guide	16
Updated Outline Dimensions	16

2/02—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, 100 nH external inductor between RFOUT and VPOS, $Z_0 = 50\ \Omega$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		1		2700	MHz
Gain	f = 900 MHz		19.8		dB
	f = 1.9 GHz		17.7		dB
	f = 2.7 GHz		15.6		dB
Delta Gain	f = 900 MHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-0.97		dB
	f = 1.9 GHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.15		dB
	f = 2.7 GHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.34		dB
Gain Supply Sensitivity	VPOS $\pm 10\%$, f = 900 MHz		0.04		dB/V
	f = 1.9 GHz		-0.004		dB/V
	f = 2.7 GHz		-0.04		dB/V
Reverse Isolation (S_{12})	f = 900 MHz		-35.6		dB
	f = 1.9 GHz		-34.9		dB
	f = 2.7 GHz		-30.3		dB
RF INPUT INTERFACE					
Input Return Loss	Pin RFIN				
	f = 900 MHz		22.3		dB
	f = 1.9 GHz		20.9		dB
	f = 2.7 GHz		11.2		dB
RF OUTPUT INTERFACE					
Output Compression Point	Pin RFOUT				
	f = 900 MHz, 1 dB compression		9.1		dBm
	f = 1.9 GHz		8.4		dBm
Delta Compression Point	f = 2.7 GHz		7.6		dBm
	f = 900 MHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.46		dB
	f = 1.9 GHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.17		dB
Output Return Loss	f = 2.7 GHz, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1		dB
	f = 900 MHz		26.3		dB
	f = 1.9 GHz		16.9		dB
	f = 2.7 GHz		13.3		dB
DISTORTION/NOISE					
Output Third-Order Intercept	f = 900 MHz, $\Delta f = 1\text{ MHz}$, $P_{IN} = -28\text{ dBm}$		23.6		dBm
	f = 1.9 GHz, $\Delta f = 1\text{ MHz}$, $P_{IN} = -28\text{ dBm}$		20.8		dBm
	f = 2.7 GHz, $\Delta f = 1\text{ MHz}$, $P_{IN} = -28\text{ dBm}$		19.5		dBm
Output Second-Order Intercept	f = 900 MHz, $\Delta f = 1\text{ MHz}$, $P_{IN} = -28\text{ dBm}$		31.6		dBm
	f = 900 MHz		5.3		dB
	f = 1.9 GHz		6		dB
Noise Figure	f = 2.7 GHz		6.8		dB
POWER INTERFACE					
Supply Voltage	Pin VPOS	2.7	3	3.3	V
Total Supply Current		35	41	48	mA
Supply Voltage Sensitivity			15.3		mA/V
Temperature Sensitivity	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		60		$\mu\text{A}/^\circ\text{C}$

AD8353

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, no external inductor between RFOUT and VPOS, $Z_O = 50\ \Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		1		2700	MHz
Gain	$f = 900\text{ MHz}$		19.5		dB
	$f = 1.9\text{ GHz}$		17.6		dB
	$f = 2.7\text{ GHz}$		15.7		dB
Delta Gain	$f = 900\text{ MHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-0.96		dB
	$f = 1.9\text{ GHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.18		dB
	$f = 2.7\text{ GHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.38		dB
Gain Supply Sensitivity	VPOS $\pm 10\%$, $f = 900\text{ MHz}$		0.09		dB/V
	$f = 1.9\text{ GHz}$		-0.01		dB/V
	$f = 2.7\text{ GHz}$		-0.09		dB/V
Reverse Isolation (S_{12})	$f = 900\text{ MHz}$		-35.4		dB
	$f = 1.9\text{ GHz}$		-34.6		dB
	$f = 2.7\text{ GHz}$		-30.2		dB
RF INPUT INTERFACE					
Input Return Loss	Pin RFIN				
	$f = 900\text{ MHz}$		22.9		dB
	$f = 1.9\text{ GHz}$		21.7		dB
	$f = 2.7\text{ GHz}$		11.5		dB
RF OUTPUT INTERFACE					
Output Compression Point	Pin RFOUT				
	$f = 900\text{ MHz}$		8.3		dBm
	$f = 1.9\text{ GHz}$		8.1		dBm
	$f = 2.7\text{ GHz}$		7.5		dBm
Delta Compression Point	$f = 900\text{ MHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.05		dB
	$f = 1.9\text{ GHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.49		dB
	$f = 2.7\text{ GHz}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		-1.33		dB
Output Return Loss	$f = 900\text{ MHz}$		27		dB
	$f = 1.9\text{ GHz}$		22		dB
	$f = 2.7\text{ GHz}$		14.3		dB
DISTORTION/NOISE					
Output Third-Order Intercept	$f = 900\text{ MHz}, \Delta f = 1\text{ MHz}, P_{IN} = -28\text{ dBm}$		22.8		dBm
	$f = 1.9\text{ GHz}, \Delta f = 1\text{ MHz}, P_{IN} = -28\text{ dBm}$		20.6		dBm
	$f = 2.7\text{ GHz}, \Delta f = 1\text{ MHz}, P_{IN} = -28\text{ dBm}$		19.5		dBm
Output Second-Order Intercept	$f = 900\text{ MHz}, \Delta f = 1\text{ MHz}, P_{IN} = -28\text{ dBm}$		30.3		dBm
Noise Figure	$f = 900\text{ MHz}$		5.6		dB
	$f = 1.9\text{ GHz}$		6.3		dB
	$f = 2.7\text{ GHz}$		7.1		dB
POWER INTERFACE					
Supply Voltage	Pin VPOS	4.5	5	5.5	V
Total Supply Current		35	42	52	mA
Supply Voltage Sensitivity			4.3		mA/V
Temperature Sensitivity	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		45.7		$\mu\text{A}/^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Power (re: 50 Ω)	10 dBm
Equivalent Voltage	700 mV rms
Internal Power Dissipation	
Paddle Not Soldered	325 mW
Paddle Soldered	812 mW
θ_{JA} (Paddle Soldered)	80°C/W
θ_{JA} (Paddle Not Soldered)	200°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 sec)	240°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD8353

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

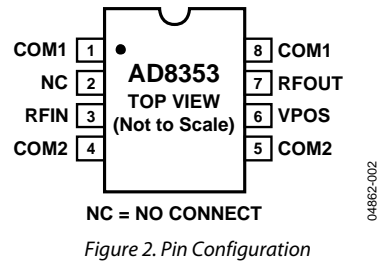


Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	COM1	Device Common. Connect to low impedance ground.
2	NC	No Connection.
3	RFIN	RF Input Connection. Must be ac-coupled.
4, 5	COM2	Device Common. Connect to low impedance ground.
6	VPOS	Positive Supply Voltage.
7	RFOUT	RF Output Connection. Must be ac-coupled.

TYPICAL PERFORMANCE CHARACTERISTICS

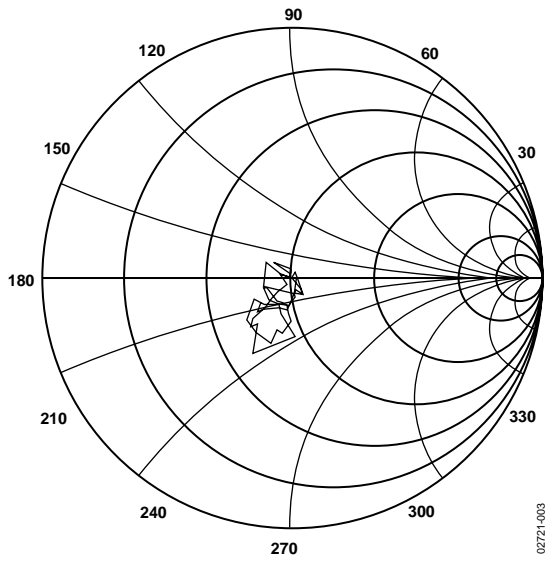


Figure 3. S_{11} vs. Frequency, $V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, $dc \leq f \leq 3\text{ GHz}$

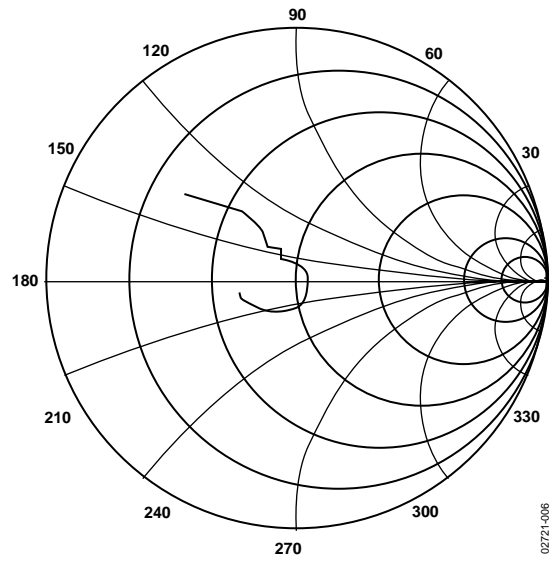


Figure 6. S_{22} vs. Frequency, $V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, $dc \leq f \leq 3\text{ GHz}$

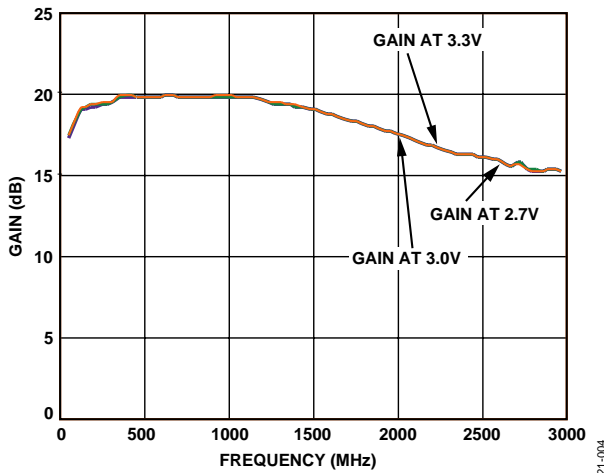


Figure 4. Gain vs. Frequency, $V_S = 2.7\text{ V}$, 3 V , and 3.3 V , $T_A = 25^\circ\text{C}$

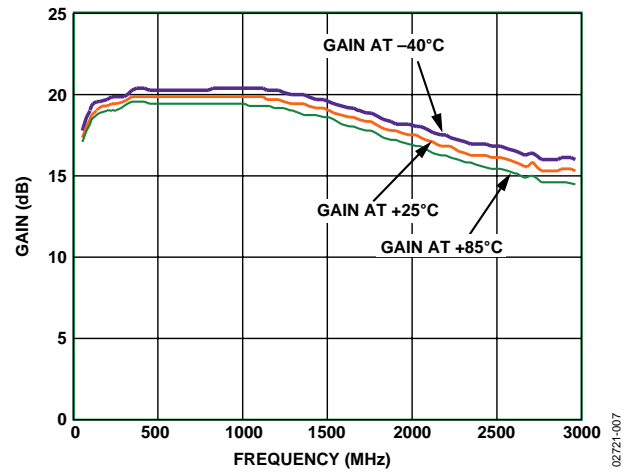


Figure 7. Gain vs. Frequency, $V_S = 3\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

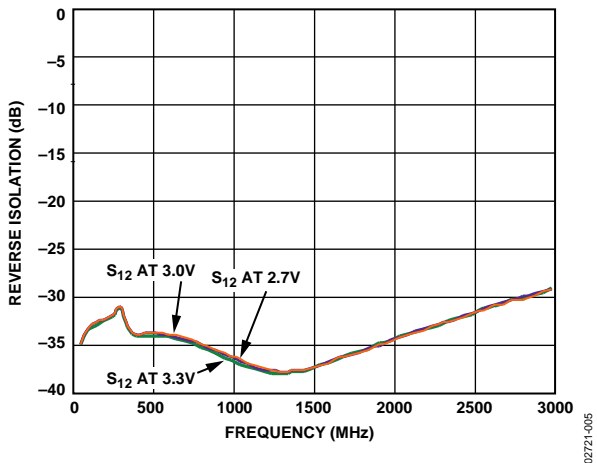


Figure 5. Reverse Isolation vs. Frequency, $V_S = 2.7\text{ V}$, 3 V , and 3.3 V , $T_A = 25^\circ\text{C}$

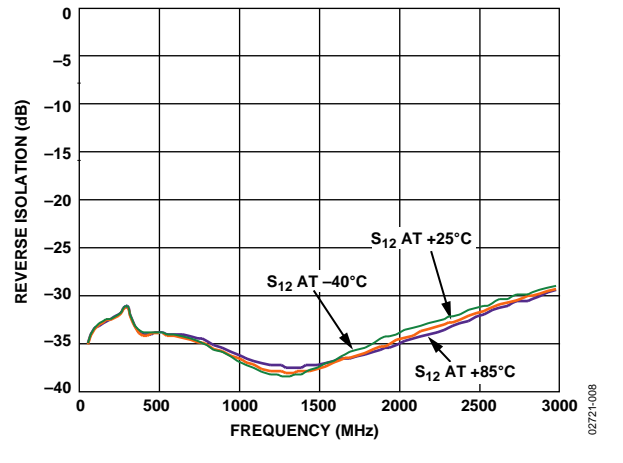


Figure 8. Reverse Isolation vs. Frequency, $V_S = 3\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

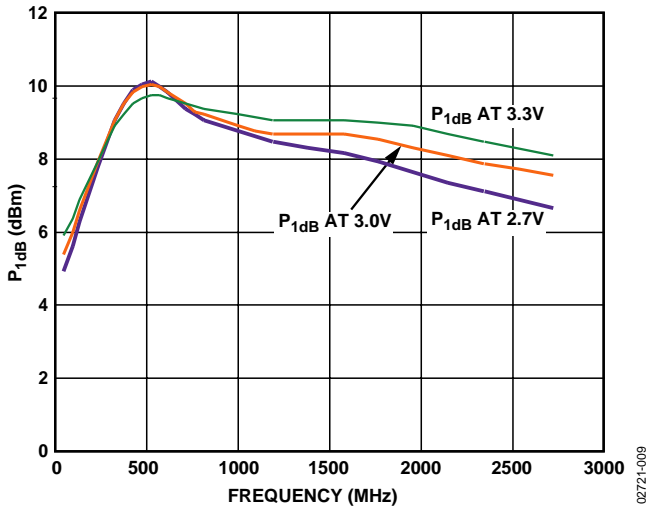


Figure 9. P_{1dB} vs. Frequency, $V_S = 2.7V, 3V,$ and $3.3V, T_A = 25^\circ C$

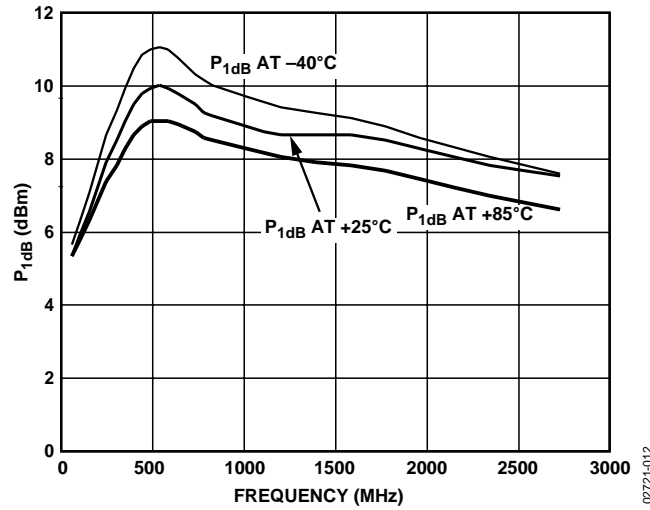


Figure 12. P_{1dB} vs. Frequency, $V_S = 3V, T_A = -40^\circ C, +25^\circ C,$ and $+85^\circ C$

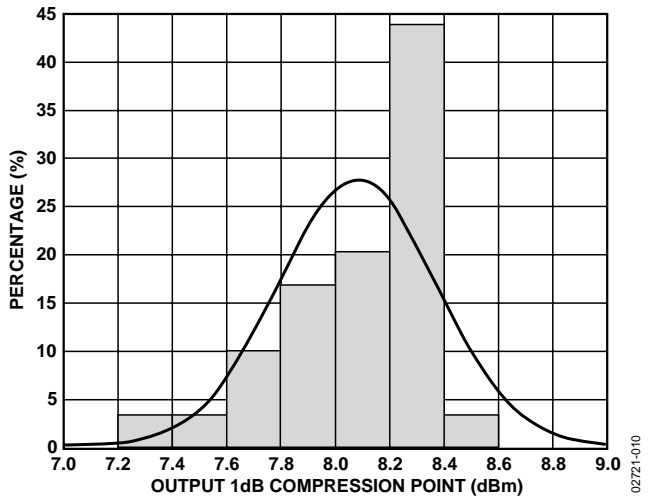


Figure 10. Distribution of P_{1dB} , $V_S = 3V, T_A = 25^\circ C, f = 2.2 GHz$

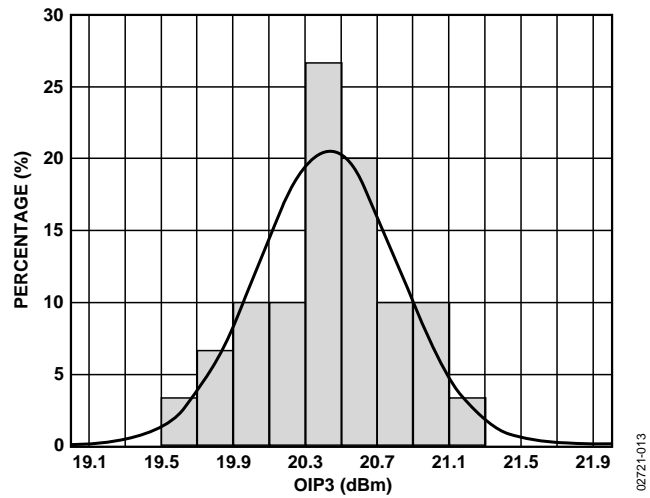


Figure 13. Distribution of $OIP3$, $V_S = 3V, T_A = 25^\circ C, f = 2.2 GHz$

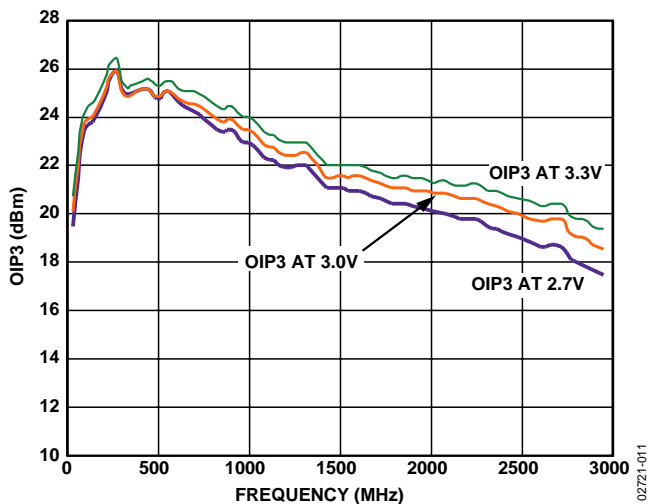


Figure 11. $OIP3$ vs. Frequency, $V_S = 2.7V, 3V,$ and $3.3V, T_A = 25^\circ C$

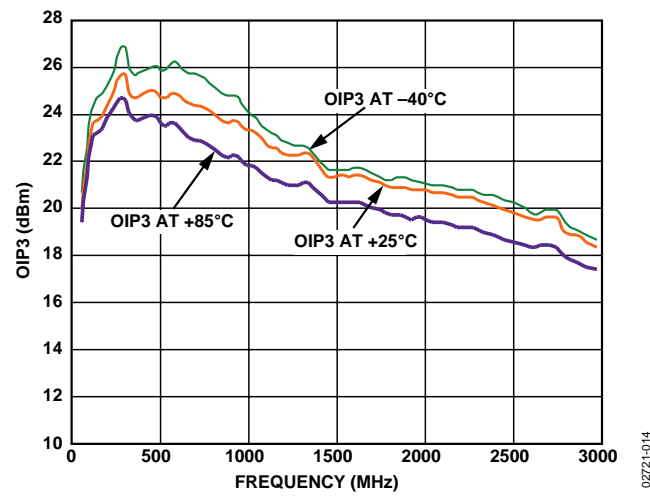


Figure 14. $OIP3$ vs. Frequency, $V_S = 3V, T_A = -40^\circ C, +25^\circ C,$ and $+85^\circ C$

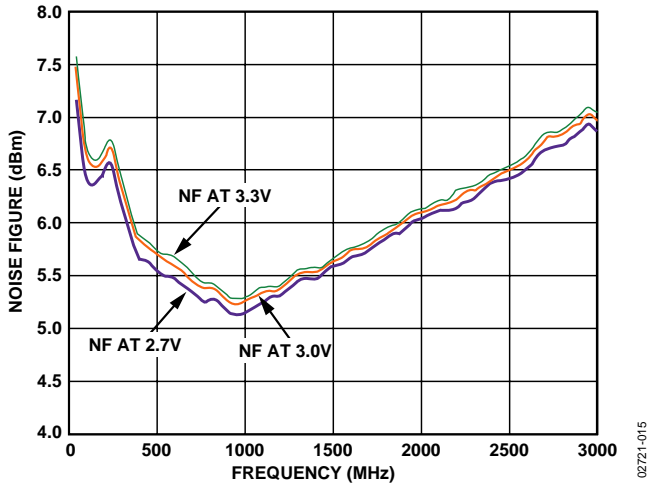


Figure 15. Noise Figure vs. Frequency, $V_S = 2.7\text{ V}$, 3 V , and 3.3 V , $T_A = 25^\circ\text{C}$

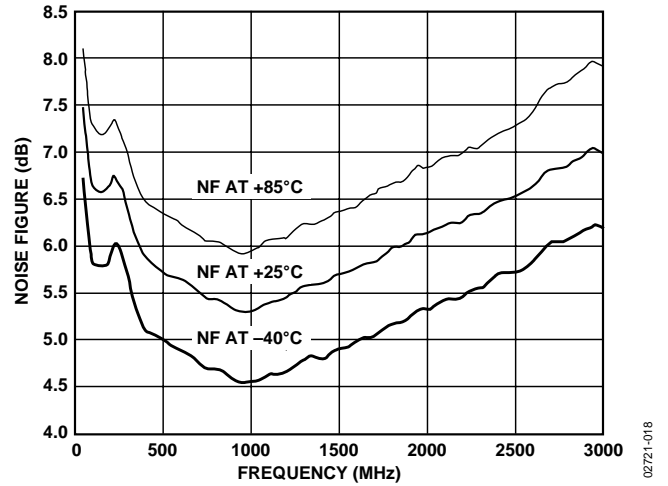


Figure 18. Noise Figure vs. Frequency, $V_S = 3\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

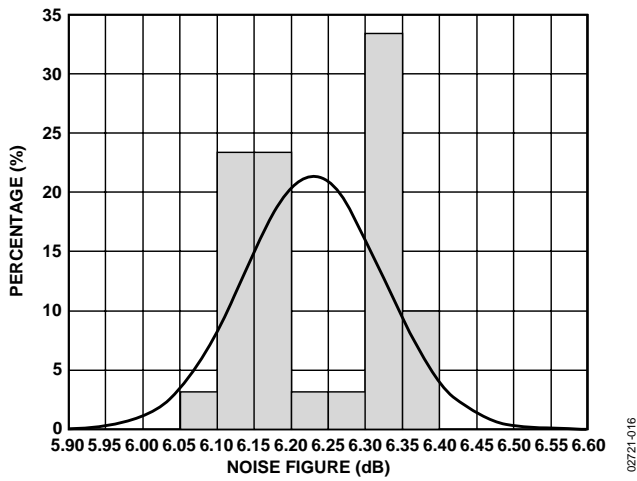


Figure 16. Distribution of Noise Figure, $V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 2.2\text{ GHz}$

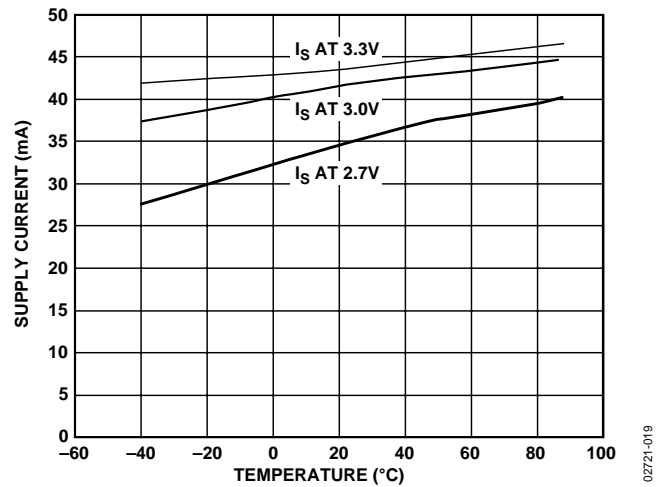


Figure 19. Supply Current vs. Temperature, $V_S = 2.7\text{ V}$, 3 V , and 3.3 V

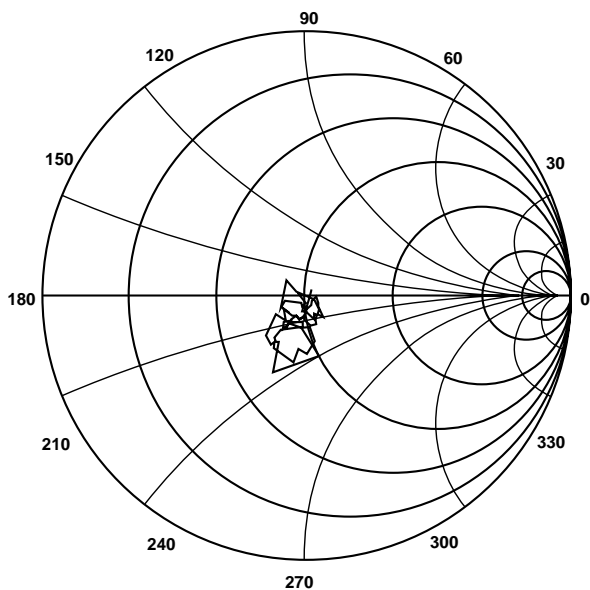


Figure 17. S_{11} vs. Frequency, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $dc \leq f \leq 3\text{ GHz}$

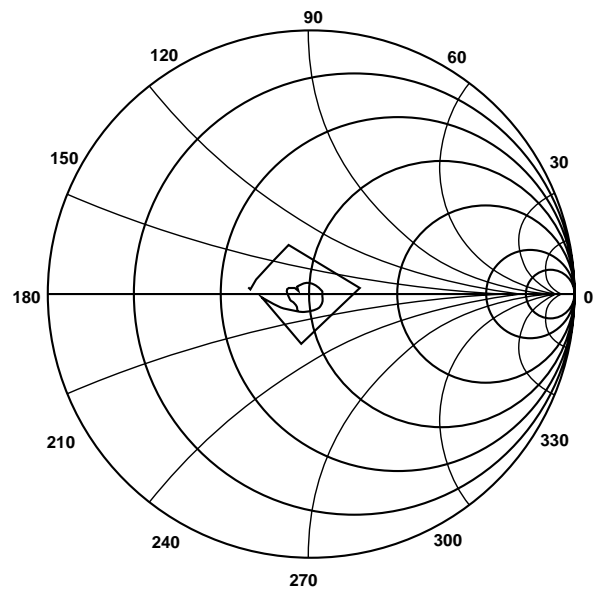


Figure 20. S_{22} vs. Frequency, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $dc \leq f \leq 3\text{ GHz}$

AD8353

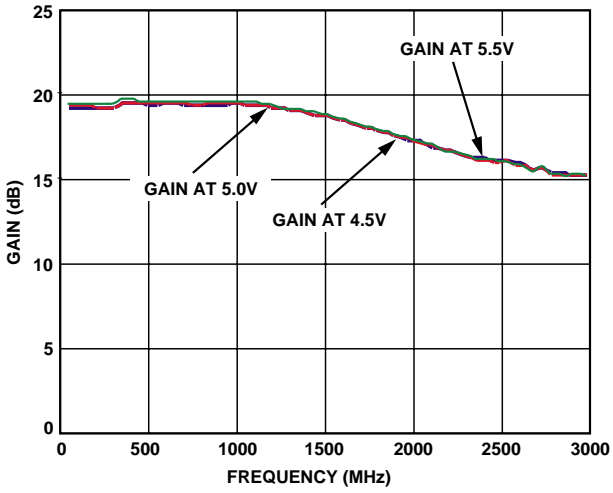


Figure 21. Gain vs. Frequency, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V , $T_A = 25^\circ\text{C}$

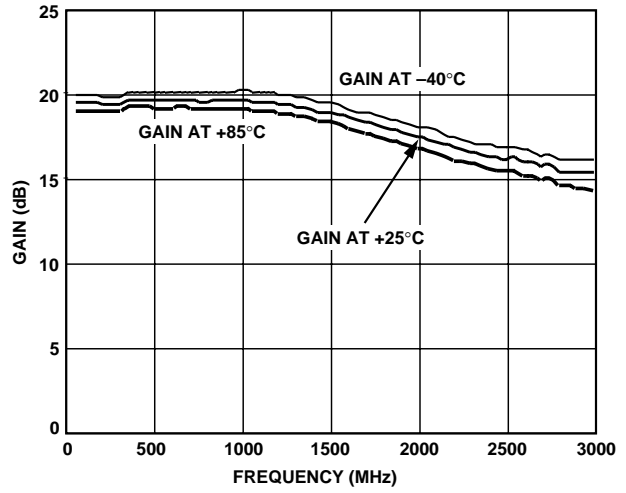


Figure 24. Gain vs. Frequency, $V_S = 5\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

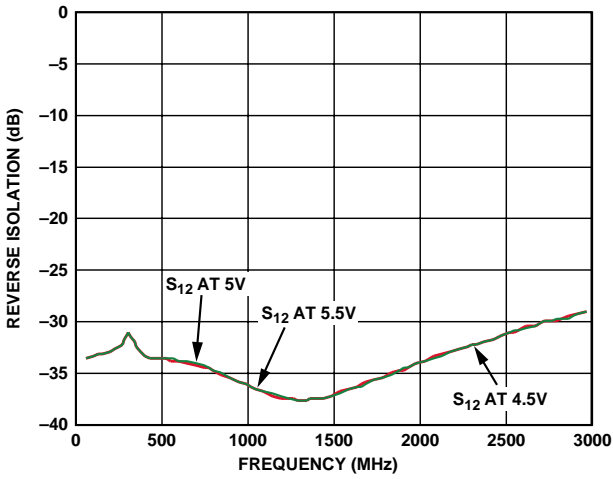


Figure 22. Reverse Isolation vs. Frequency, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V , $T_A = 25^\circ\text{C}$

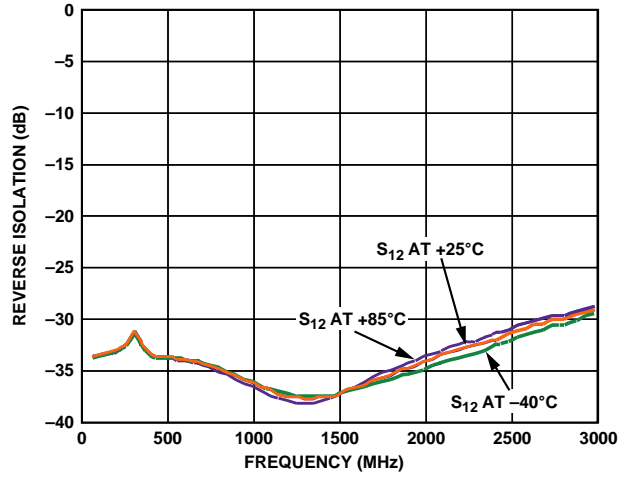


Figure 25. Reverse Isolation vs. Frequency, $V_S = 5\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

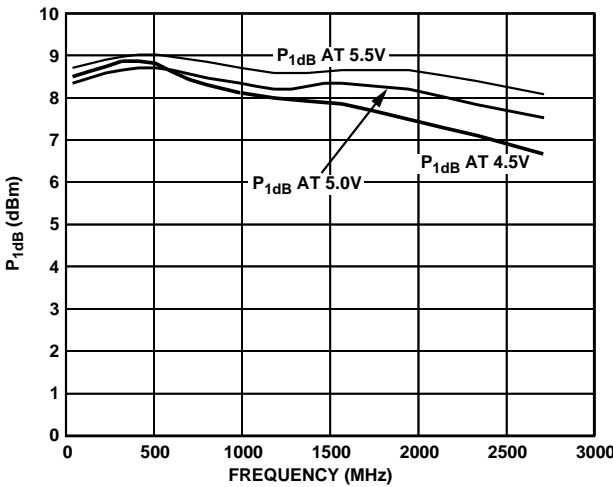


Figure 23. P_{1dB} vs. Frequency, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V , $T_A = 25^\circ\text{C}$

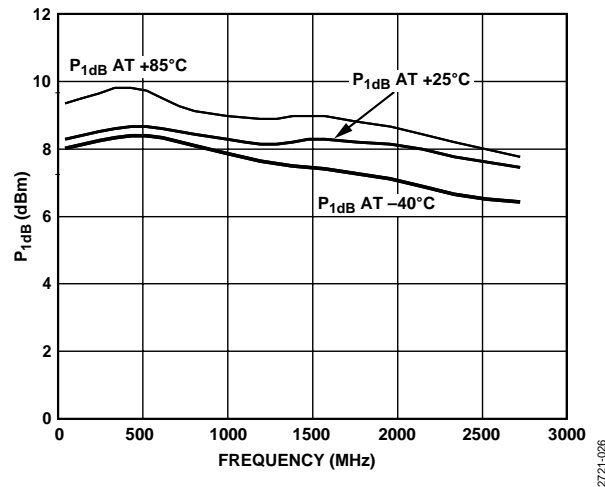


Figure 26. P_{1dB} vs. Frequency, $V_S = 5\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

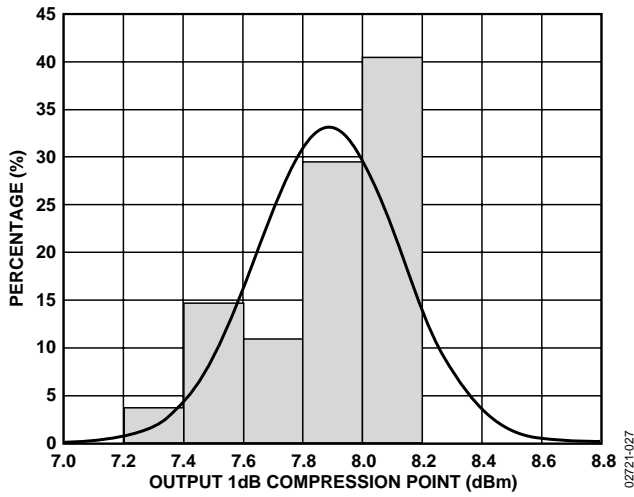


Figure 27. Distribution of P_{1dB} , $V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 2.2\text{ GHz}$

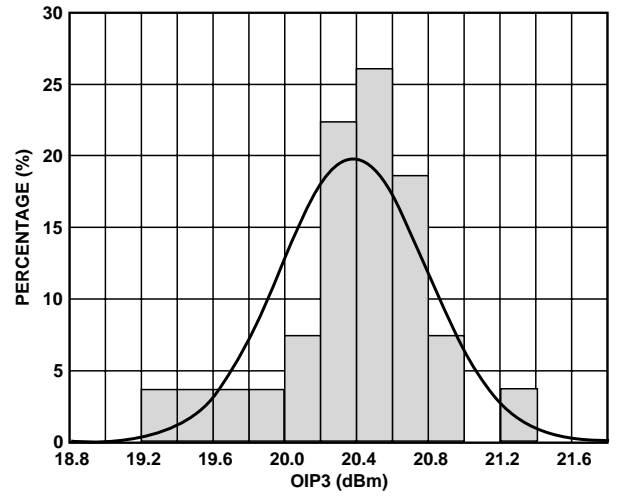


Figure 30. Distribution of OIP3, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 2.2\text{ GHz}$

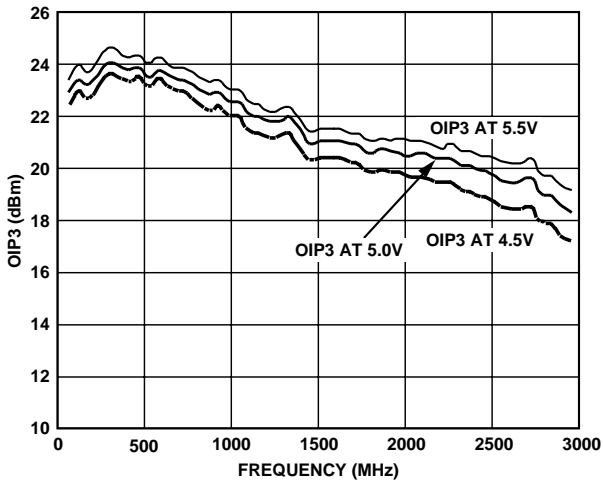


Figure 28. OIP3 vs. Frequency, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V , $T_A = 27^\circ\text{C}$

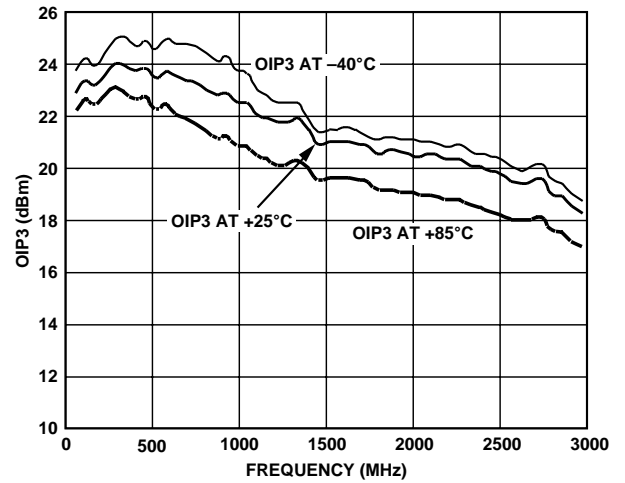


Figure 31. OIP3 vs. Frequency, $V_S = 5\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

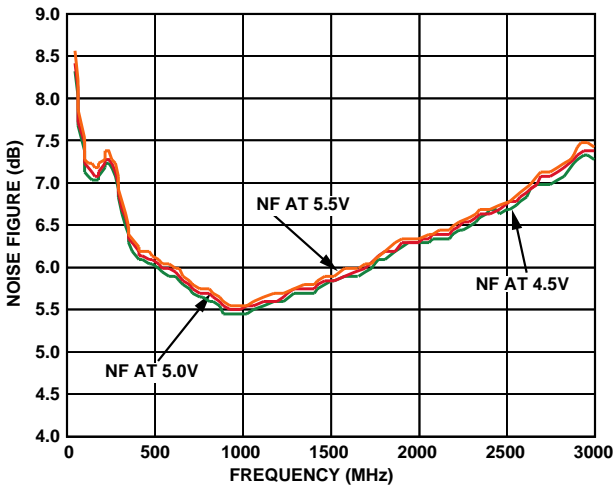


Figure 29. Noise Figure vs. Frequency, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V , $T_A = 25^\circ\text{C}$

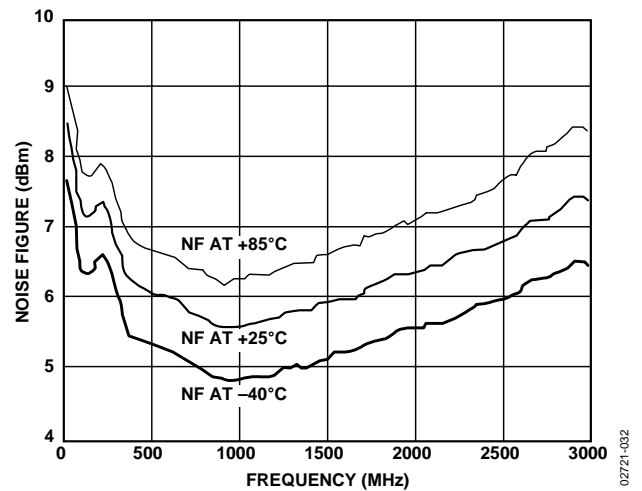


Figure 32. Noise Figure vs. Frequency, $V_S = 5\text{ V}$, $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, and $+85^\circ\text{C}$

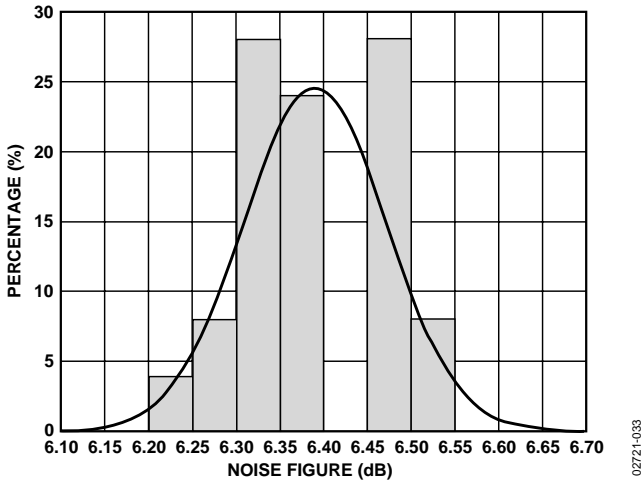


Figure 33. Distribution of Noise Figure, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 2.2\text{ GHz}$

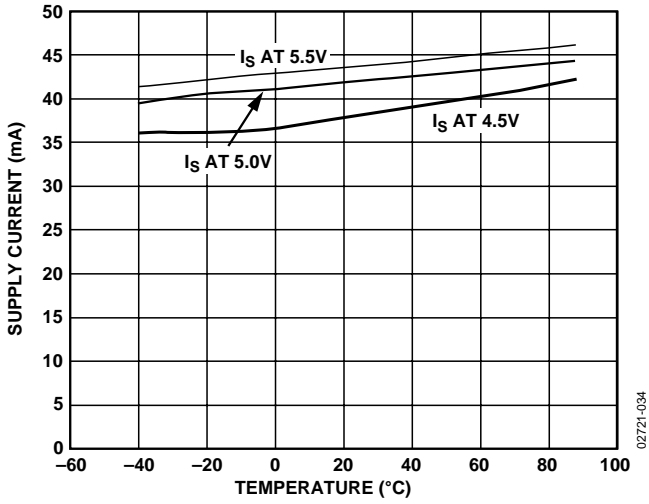


Figure 34. Supply Current vs. Temperature, $V_S = 4.5\text{ V}$, 5 V , and 5.5 V

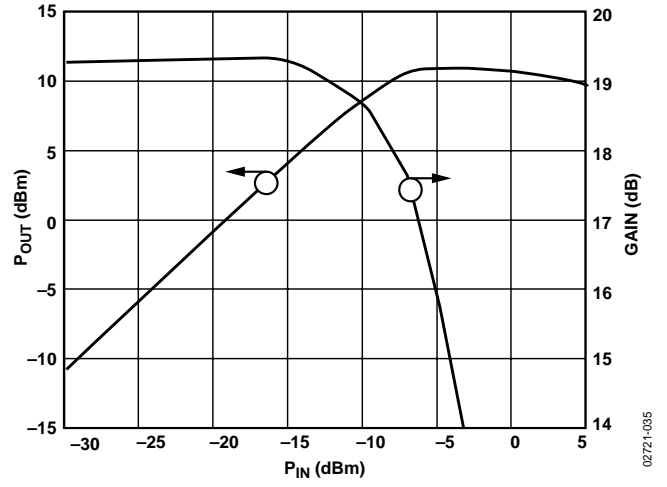


Figure 35. Output Power and Gain vs. Input Power, $V_S = 3\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 900\text{ MHz}$

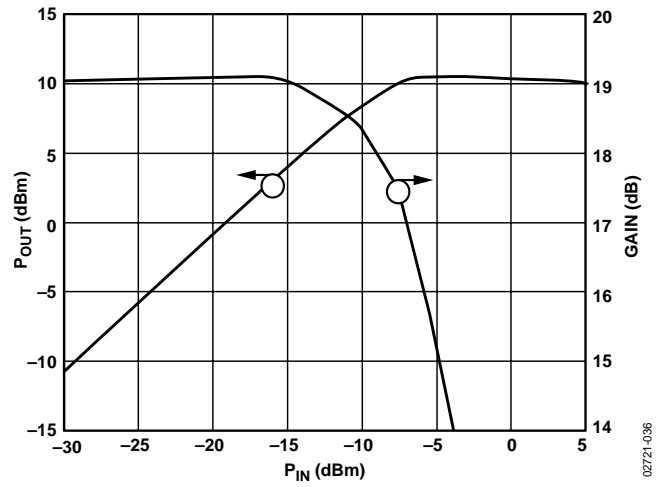


Figure 36. Output Power and Gain vs. Input Power, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $f = 900\text{ MHz}$

THEORY OF OPERATION

The AD8353 is a 2-stage, feedback amplifier employing both shunt-series and shunt-shunt feedback. The first stage is degenerated and resistively loaded and provides approximately 10 dB of gain. The second stage is a PNP-NPN Darlington output stage, which provides another 10 dB of gain. Series-shunt feedback from the emitter of the output transistor sets the input impedance to 50 Ω over a broad frequency range. Shunt-shunt feedback from the amplifier output to the input of the Darlington stage helps to set the output impedance to 50 Ω . The amplifier can be operated from a 3 V supply by adding a choke inductor from the amplifier output to VPOS. Without this choke inductor, operation from a 5 V supply is also possible.

BASIC CONNECTIONS

The AD8353 RF gain block is a fixed gain amplifier with single-ended input and output ports whose impedances are nominally equal to 50 Ω over the frequency range 1 MHz to 2.7 GHz. Consequently, it can be directly inserted into a 50 Ω system with no impedance matching circuitry required. The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required. A complete set of scattering parameters is available at www.analog.com.

The input pin (RFIN) is connected directly to the base of the first amplifier stage, which is internally biased to approximately 1 V; therefore, a dc blocking capacitor should be connected between the source that drives the AD8353 and the input pin, RFIN.

It is critical to supply very low inductance ground connections to the ground pins (Pin 1, Pin 4, Pin 5, and Pin 8) as well as to the backside exposed paddle. This ensures stable operation.

The AD8353 is designed to operate over a wide supply voltage range, from 2.7 V to 5.5 V. The output of the part, RFOUT, is taken directly from the collector of the output amplifier stage. This node is internally biased to approximately 2.2 V when the supply voltage is 5 V. Consequently, a dc blocking capacitor should be connected between the output pin, RFOUT, and the load that it drives. The value of this capacitor is not critical, but it should be 100 pF or larger.

When the supply voltage is 3 V, it is recommended that an external RF choke be connected between the supply voltage and the output pin, RFOUT. This increases the dc voltage applied to the collector of the output amplifier stage, which improves performance of the AD8353 to be very similar to the performance produced when 5 V is used for the supply voltage. The inductance of the RF choke should be approximately 100 nH, and care should be taken to ensure that the lowest series self-resonant frequency of this choke is well above the maximum frequency of operation for the AD8353. For lower frequency operation, use a higher value inductor.

Bypass the supply voltage input, VPOS, using a large value capacitance (approximately 0.47 μ F or larger) and a smaller, high frequency bypass capacitor (approximately 100 pF) physically located close to the VPOS pin.

The recommended connections and components are shown in Figure 40.

APPLICATIONS

The AD8353 RF gain block can be used as a general-purpose, fixed gain amplifier in a wide variety of applications, such as a driver for a transmitter power amplifier (see Figure 37). Its excellent reverse isolation also makes this amplifier suitable for use as a local oscillator buffer amplifier that would drive the local oscillator port of an upconverter or downconverter mixer (see Figure 38).

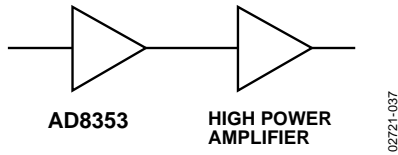


Figure 37. AD8353 as a Driver Amplifier

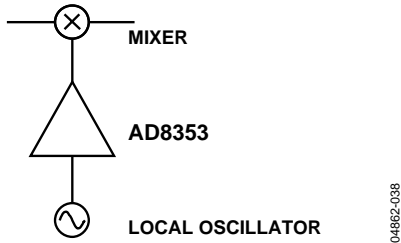


Figure 38. AD8353 as a LO Driver Amplifier

LOW FREQUENCY APPLICATIONS BELOW 100 MHz

The AD8353 RF gain block can be used below 100 MHz. To accomplish this, the series dc blocking capacitors, C1 and C2, need to be changed to a higher value that is appropriate for the desired frequency. C1 and C2 were changed to 0.1 μ F to accomplish the sweep in Figure 39.

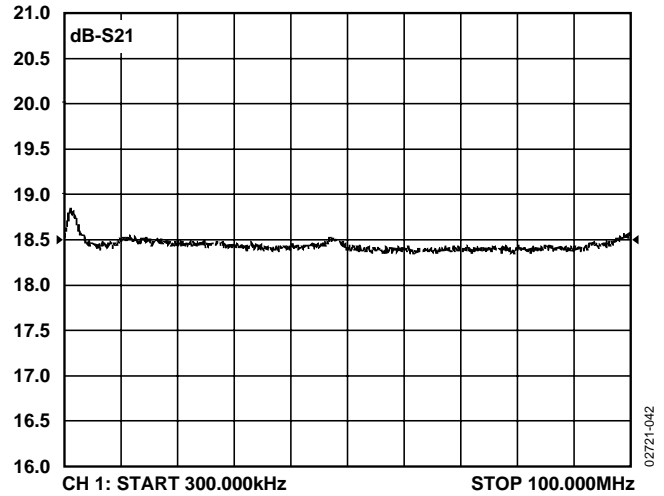


Figure 39. Low Frequency Application from 300 kHz to 100 MHz at 5 V VPOS, -12 dBm Input Power

EVALUATION BOARD

Figure 40 shows the schematic of the AD8353 evaluation board. Note that L1 is shown as an optional component that is used to obtain maximum gain only when $V_P = 3$ V. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by a 0.47 μ F and a 100 pF capacitor.

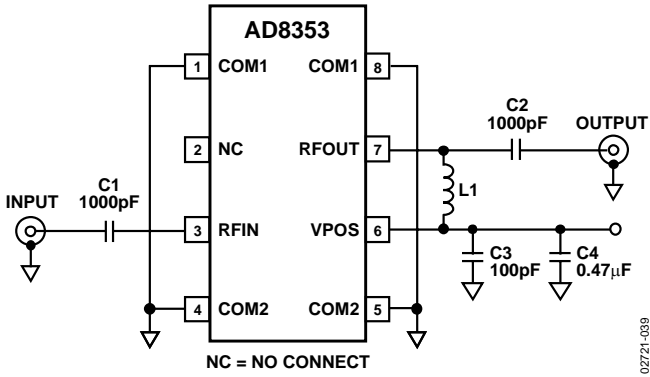


Figure 40. Evaluation Board Schematic

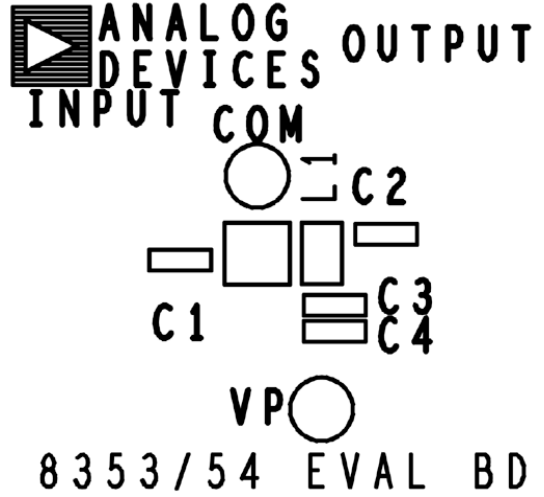


Figure 41. Silkscreen Top

Table 5. Evaluation Board Configuration Options

Component	Function	Default Value
C1, C2	AC coupling capacitors.	1000 pF, 0603
C3	High frequency bypass capacitor.	100 pF, 0603
C4	Low frequency bypass capacitor.	0.47 μ F, 0603
L1	Optional RF choke, used to increase current through output stage when $V_P = 3$ V. Not recommended for use when $V_P = 5$ V.	100 nH, 0603

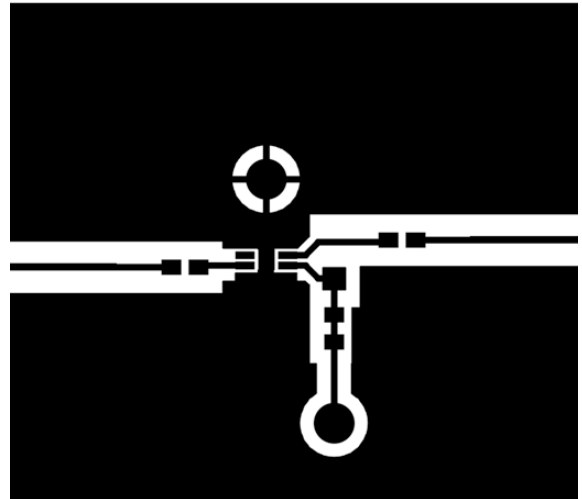


Figure 42. Component Side

OUTLINE DIMENSIONS

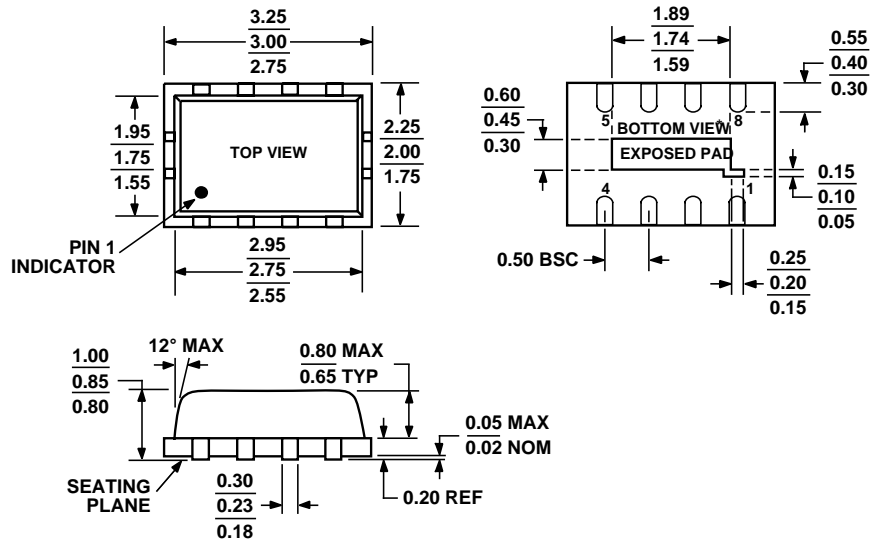


Figure 43. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
 2 mm × 3 mm Body, Very Thin, Dual Lead
 CP-8-1
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8353ACP-R2	-40°C to +85°C	8-Lead LFCSP_VD	CP-8-1	JB
AD8353ACP-REEL7	-40°C to +85°C	8-Lead LFCSP_VD, 7" Tape and Reel	CP-8-1	JB
AD8353ACPZ-REEL7 ¹	-40°C to +85°C	8-Lead LFCSP_VD, 7" Tape and Reel	CP-8-1	OE
AD8353-EVAL		Evaluation Board		

¹ Z = Pb-free part.