TEXAS INSTRUMENTS

TLC5540/TLC5510/TLC5510A/ TLV5540/TLV5510

Evaluation Module

User's Guide

1999

Mixed-Signal Products

SLAU007C

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Preface

Read This First

About This Manual

The purpose of this user's guide is to serve as a reference book for the TLC5540/TLC5510/TLC5510A/TLV5510/TLV5540 devices. This document provides information to assist managers and hardware/software engineers in application development.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 Overview
- Chapter 2 Circuit Description
- Chapter 3 Physical Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following documents may be ordered by contacting the Texas Instruments Product Information Center at one of the numbers listed on the next page, or, they may be downloaded at:

http://www–s.ti.com/sc/docs/psheets/pids2.htm

TLC5510/TLC5510A Data Sheet (literature number SLAS095) contains electrical specifications, available temperature options, general overview of the device, and application information.

TLC5540 Data Sheet (literature number SLAS105) contains electrical specifications, available temperature options, general overview of the device, and application information.

TLV5510 Data Sheet (literature number SLAS124) contains electrical specifications, available temperature options, general overview of the device, and application information.

TLV5540 Data Sheet (literature number SLAS192) contains electrical specifications, available temperature options, general overview of the device, and application information.

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Chapter 1

Overview

This chapter gives an overview of the TLC5540/TLC5510/TLC5510A/ TLV5540/TLV5510 evaluation module (EVM).

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1.1 Purpose

The TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 evaluation module (EVM) provides a platform for lab prototype evaluation of the Texas Instruments TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 8-bit, high-speed analog-to-digital converters.

Since practical operation can be acheived in excess of 40 MHz, the circuit layout is critical and does not lend itself to classic breadboarding techniques. In fact, proper operation requires use of surface-mount components.

1.2 Power Supply Requirements

The TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 EVM is designed to be powered by regulated lab power supplies. Three lab supplies are required for the best performance.

Table 1–1. Power Supplies

Connector	Supply	If Amp Used		By-pass Amp	
		TLC5540/5510/ 5510A	TLV5540/5510	TLC5510/ 5540/5510A	TLV5510/5540
J2	Positive analog supply	5 V ±10%	3.6 V MIN	5 V ±10%	3.6 V – 2.7 V
J3	Negative analog supply	–5 V ±10%	–3.6 MIN	N/A	N/A
J8	Digital supply	5 V ±10%	3.6 V – 3.3 V	5 V ±10%	3.6 V – 2.7 V

The 5 V/3.6 V and –5 V/–3.6 V analog supplies share an analog ground plane. The digital supply uses an isolated ground plane.

The two ground planes can be easily connected by soldering jumpers from E21 to E22 or from E13 to E14. This allows the user to adapt the EVM to various grounding conditions that can exist in an evaluation circuit interface.

Chapter 2

Circuit Description

This chapter describes the EVM circuit and its operation.

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2.1 EVM Analog Input

The EVM analog input signal is applied to BNC connector J4 by one of four methods:

- Direct
- Amplifier input (dc coupled)
- Amplifier input (ac coupled)
- User supplied input

2.1.1 Direct Input

To route the signal directly to the TLC5540/TLC5510/TLC5510A/ TLV5540/TLV5510 input, solder jumpers from E7 to E8 and from E23 to E12. This provides a 50-Ohm load (R5) at input connector J4. The input signal must be dc biased to the specifications defined by the data sheet. The TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 is connected using its internal bias resistors. Jumper J6 bypasses one of the internal bias resistors and thus alters the input bias range required by the input signal. With J6 installed, the voltage range of the TLC5540/TLC5510 is 0 V – 2.28 V and TLV5540/TLV5510 is 0 V – 2.74 V (at 3.3 V_{DDA}).

The TLC5510A uses only the center internal bias resistor with an externally-applied regulated 4-V reference to generate the device reference voltage. Hence the input signal range applied to J4 can be between 0 V – 4 V.

The input signal is bandlimited to 12 MHz by the LC filter consisting of FB5, R15, and C5. For a bandwidth of 20 MHz, select a value for C5 in the 15 pF to 33 pF range.

2.1.2 Amplifier Input, DC Coupled

A THS3001 high-speed transconductance operational amplifier provides buffering for dc-coupled amplifier-input signals. The amplifier circuit provides a flat response to 300 MHz with a gain of two. It can drive a low impedance load.

The values of R6 and R8 set the amplifier gain to two.

The gain can be reduced to one by removing R6. Since the inverting input is a low-impedance current-controlled input, R8 must remain in the circuit, and its value must be changed to 1 kΩ. This resistance value is critical because it controls the high frequency response of the circuit. The TLC5510A amplifier gain is set to one.

The output roll-off filter, consisting of R4 and C14, provides a small amount of filtering against frequencies in excess of 20 MHz (f_S/2). The value of C14 can be altered to change the filter characteristics, or C14 can be removed entirely. In most cases, R4 should be retained to lower the direct capacitive load on the operational amplifier, thereby avoiding high frequency peaking of the output signal.

Resistor R7 also provides isolation against a direct capacitive load (such as a scope probe) on the test point terminal.

The amplifier output circuit is connected to the TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 by soldering a jumper between terminals E10 and E12.

The amplifier input can be either dc coupled or ac coupled to the input. Table 2–1 shows the jumpers required to select either input coupling method.

Table 2–1. Amplifier Input Coupling

Coupling	Jumper Terminals
dc	E3 to E4
ac	E1 to E2

2.1.3 Amplifier Input, AC Coupled

Potentiometer R2 controls the dc input bias for amplifier ac-coupled inputs. This allows the bias to be varied from near ground to near 5 V/3.6 V (analog). With an amplifier gain of two, the output approaches the positive power supply when the bias potentiometer approaches 2.5 V for the TLC5510/TLC5560 and 1.8 V for the TLV5510/TLV5540.

For a 4-V input and a gain of 1 (R6 removed and R8 set to 1 kΩ for optimum settling time and minimum ringing) bias potentiometer R2 is adjusted such that E1 is at 2 V and the amplifier output swing is 0 V to 4 V at TP2. With an amplifier supply voltage of +5 V the output positive peak will be distorted slightly; therefore, it is necessary to adjust the 5-V supply to 5.56 V in order to prevent clipping of the amplifier output voltage.

The low frequency response pole is dominated by the 4.7-μF capacitor (C6) and the resistance setting of the potentiometer.

2.1.4 Input Bias Operational Range

Jumper J6 determines the signal input range (0 to full scale) at the analog input of the TLC5540/TLC5510/TLC5510A/TLV5570/TLV5540. Table 2–2 shows the effects of J6.

Table 2–2. Input Voltage Setting

Jumper J6	TLC5540/TLC5510 Input Voltage Range @ 5 V_{DDA}	TLV5540/TLV5510 Input Voltage Range @ 3.3 V_{DDA}	TLC5510A Input Voltage Range @ 5 V_{DDA}
Removed	0.6 V to 2.6 V	0.66 V to 2.87 V	0 V to 4 V (J11 and J16 installed)
Installed	0 V to 2.28 V	0 V to 2.74 V	0 V to 4 V (J11 and J16 installed)

Other output ranges can be configured. See the TLC5540/TLC5510/ TLC5510A/TLV5540/TLV5510 data sheets.

2.1.5 Test Points

Test points TP1 and TP2 provide an oscilloscope connection to monitor the output of the analog input conditioning amplifier stage as follows:

Table 2–3. Test Points

Test Point	Connection
TP1	Analog ground
TP2	Analog output of THS3001

2.1.6 User Supplied Input Circuit

A breadboarding area allows the use of custom input filters or other signal conditioning circuits. To route the input signal to the breadboarding area (terminal E24), solder a jumper between terminals E5 and E6.

To route the signal from the breadboard area (terminal E25) to the TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 input, solder a jumper between terminals E11 and E12.

Only one of the above configurations should be used at one time to prevent excessive capacitance on the signal path. This excessive capacitance can degrade the input signal quality at high frequencies.

2.2 Digital Output

An octal high-speed latch (U4) provides buffered digital data. The factory configuration uses this latch as a buffer to drive the 22-ohm line damping resistors.

Pin 24 on the output connector (J5) can be used to drive the U4 output to a high impedance (3-state) allowing a bus interface to external circuitry. To do so, the jumper between terminals E17 and E18 must be removed to remove the ground connection. Logic 1 applied to J5 pin 24 makes the latch output a 3-state output.

This latch can be transparent by using external circuitry to drive the strobe input (pin 11). The jumper at E19 and E20 must be removed and the external drive be connected to E19. A logic 0 on this input captures and holds the input data on the output. A logic 1 allows the outputs to follow the inputs.

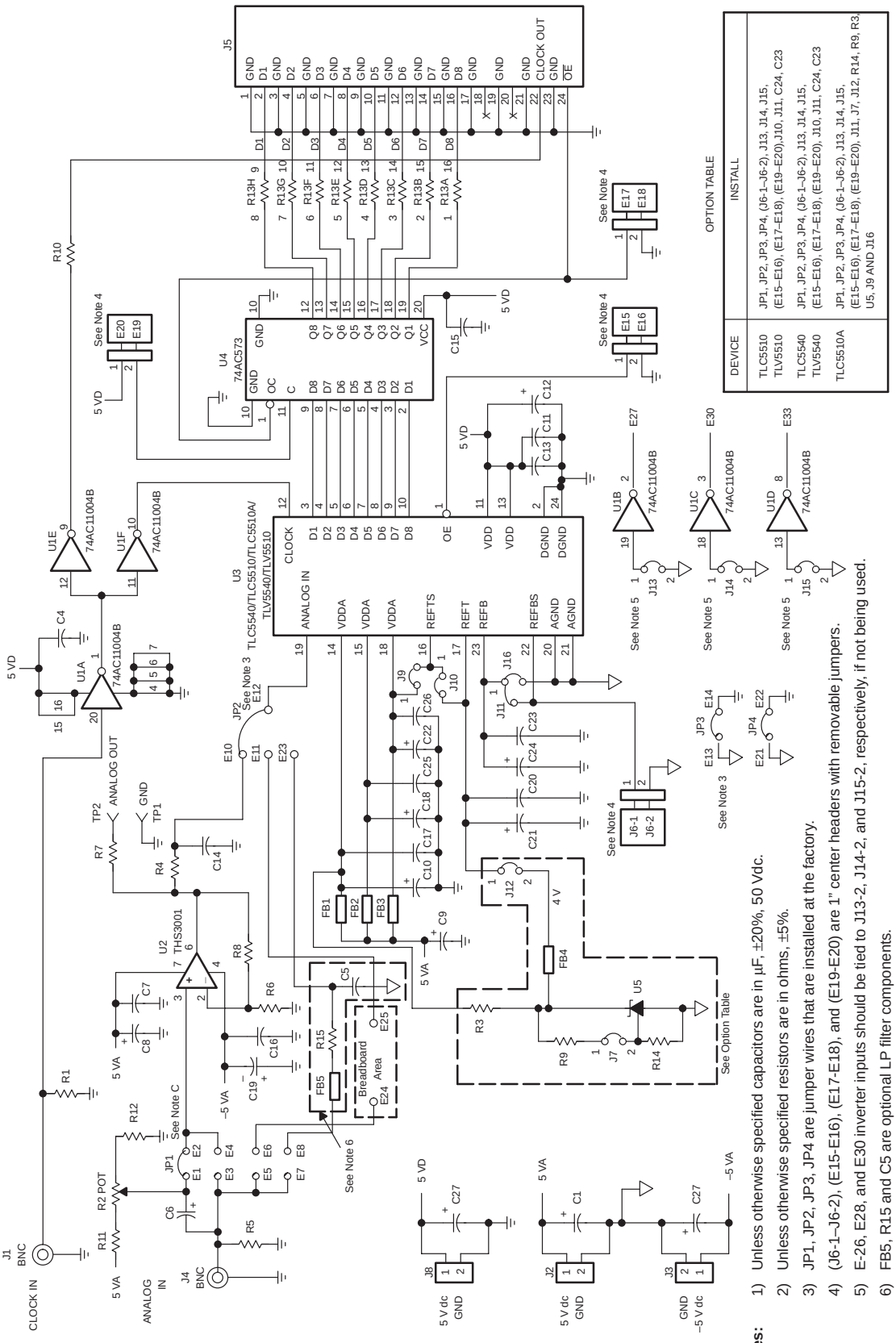
2.3 Clock Circuit

An external clock of up to 40 MHz is required for operation. The clock source is required to drive the 50-ohm BNC input J1. If the clock signal comes from a DSP or microcontroller, resistor R1 should be removed from the circuit. The clock is buffered by inverters (U1) and provides a true (noninverted) output to the TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510 and a true equivalent output at pin 22 of the output connector J5. This provides the user a buffered reference clock output for external circuitry.

2.4 Board Schematic

Figure 2–1 shows the EVM board schematic.

Figure 2–1. Board Schematic



Notes:

1) Unless otherwise specified capacitors are in µF, ±20%, 50 Vdc.
2) Unless otherwise specified resistors are in ohms, ±5%.
3) JP1, JP2, JP3, JP4 are jumper wires that are installed at the factory.
4) (J6-1–J6-2), (E15-E16), (E17-E18), and (E19-E20) are 1" center headers with removable jumpers.
5) E-26, E28, and E30 inverter inputs should be tied to J13-2, J14-2, and J15-2, respectively, if not being used.
6) FB5, R15 and C5 are optional LP filter components.

Chapter 3

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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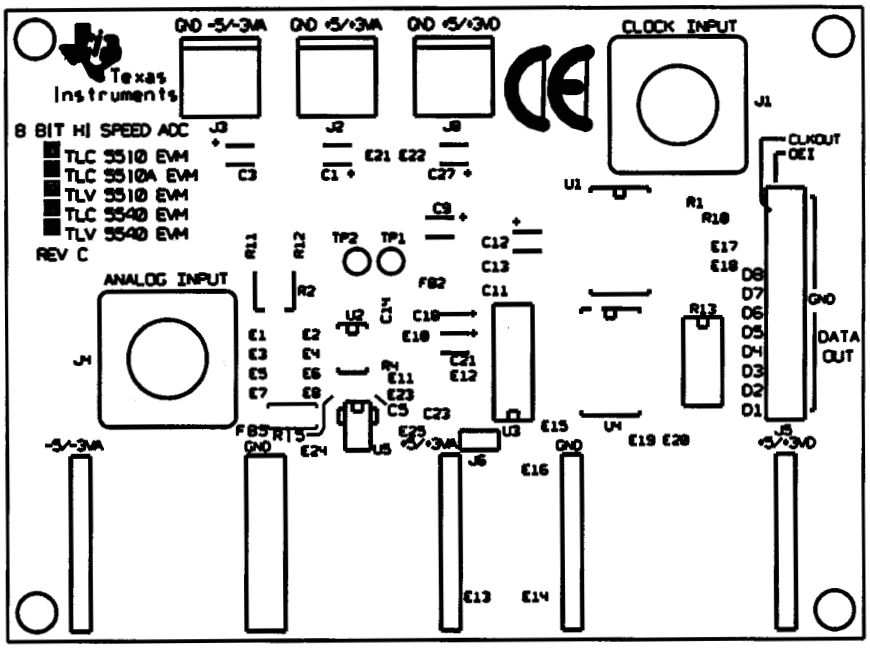
3.1 Board Layout

Figure 3–1 shows the EVM board layout.

Figure 3–1. EVM Board Layout



TI TLC 5540 EVM REV. C
SILKSCREEN TOP SIDE

3.2 Board Layers

Figures 3–2 through 3–5 show the EVM board layers.

Figure 3–2. EVM Board Layer 1

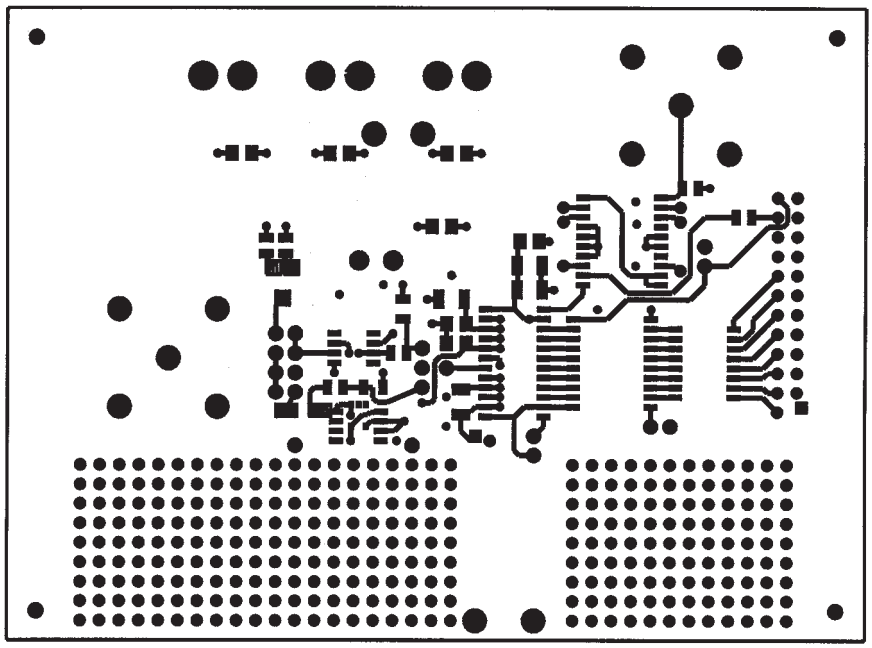


Figure 3–3. EVM Board Layer 2

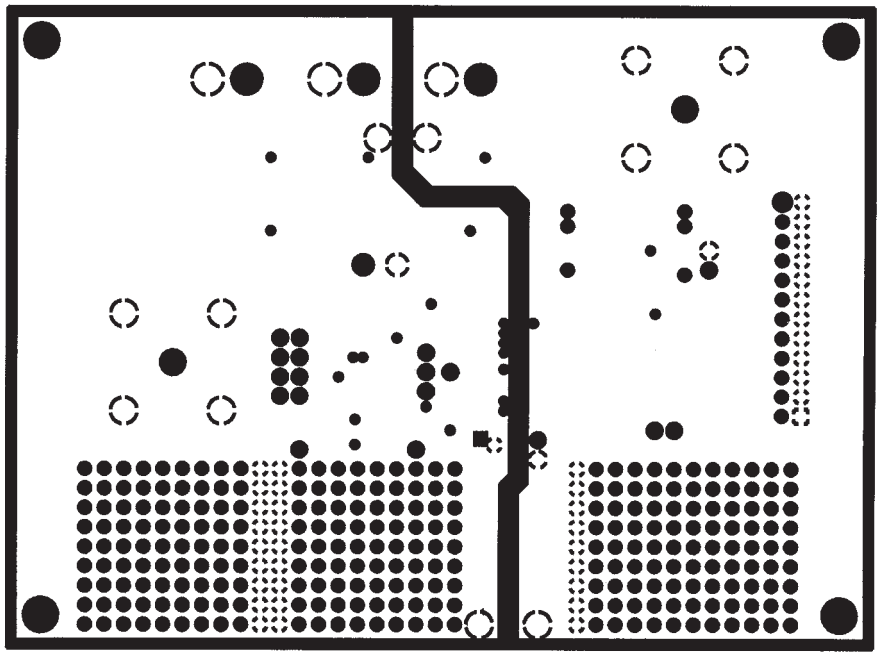


Figure 3–4. EVM Board Layer 3

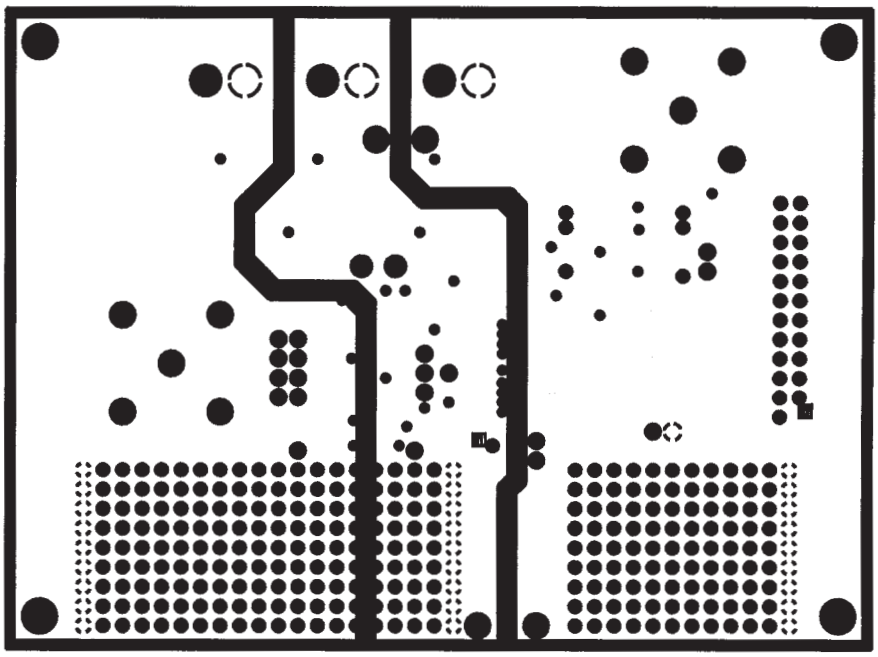
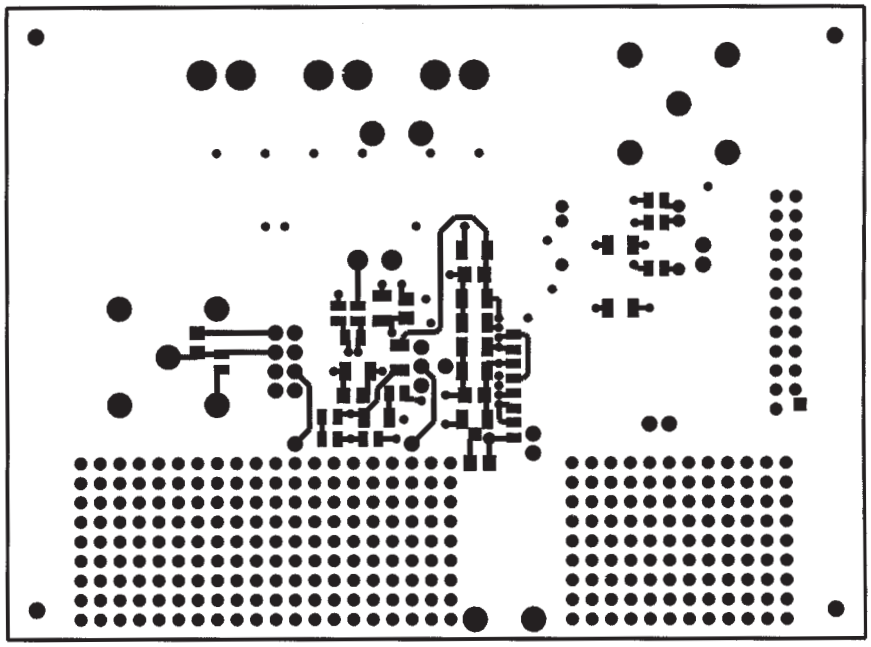


Figure 3–5. EVM Board Layer 4



3.3 Part Descriptions

Table 3–1 lists and describes the EVM parts. C2 and E9 are not used.

Table 3–1. Part Descriptions

Quantity	Reference	Description
11	C4, C7, C11 C13, C15, C16, C17, C20, C23, C25, C26	0.1 μF capacitor, 50 V, 10%, COG, SMD, size 1206
13	C1, C3, C6, C8–C10, C12, C18, C19, C21, C22, C24, C27	4.7 μF capacitor, tantalum electrolytic, SMD, size A
1	C5†	68 pF capacitor, 50 V, 5%, NPO, SMD, size 1210
1	C14	100 pF (TLC5540)/150 pF(TLC5510/TLC5510A) capacitor, 50 V, 5%, NPO, SMD, size 0805
3	FB1–FB5†	Ferrite bead, SMD, size 1206, Murata BLM31B601SPT
2	J1, J4	Connector, BNC, 50 Ω, vertical, PC mount
3	J2, J3, J8	Screw terminal, 2 pin, vertical
1	J5	Header, 2 × 12, 0.025 inch square pins, 0.1 inch centers
4	J6, (E15, E16), (E17, E18), (E19, E20)	Header, 1 × 2, 0.025 inch square pins, 0.1 inch centers
4	R1, R4, R5, R7	Resistor, 49.9 Ω, 1/8 W, 1 %, SMD, size 0805
1	R2	Potentiometer, 10 kΩ, multiturn SMD
1	R3	Resistor, 20 Ω, 1/4 W, SMD, size 1210
2	R6, R8	Resistor, 750 Ω, 1/10 W, 1 %, SMD, size 0805
1	R9	Resistor, 15K, 1/10 W, 1%, SMD, size 1210
1	R10	Resistor, 22 Ω, 1/10 W, 5%, SMD, size 0805
2	R11, R12	Resistor, 1 kΩ, 1/10 W, 5 %, SMD, size 0805
1	R13	Resistor pack, 22 Ω × 8, 1/8 W, 5%, SMD, SOIC-16
1	R14	Resistor, 24.9K, 1/10 W, 1%, SMD, size 1210
1	R15†	Resistor, 10 Ω, 1/10 W, 1%, SMD, size 1210
2	TP1, TP2	Test point terminal
4	P6, (P15, P16), (P17, P18), (P19, P20)	Jumper, for 0.025 inch, square pins, 0.1 inch centers
1	U1	IC, (SN)74AC11004DW inverter, SOIC-16
1	U2	IC, THS3001CD operational amplifier, SOIC-8
1	U3	IC, TLC5540INSLE/TLC5510INSLE/TLC5510AINSLE/ TLV5540INSLE/TLV5510INSLE ADC
1	U4	IC, SN74AC573DW octal transparent latch, SOIC-20
1	U5	IC, TL431AID or TLV431AIDBV5, SOIC–8, SOT–23
1	PCB1	PCB, TLC5540/TLC5510/TLC5510A/TLV5540/TLV5510

† C5, FB5 and R15 not on REV C PCB