MICRF505

868MHz and 915MHz ISM Band Transceiver

General Description

The MICRF505 is a true single chip, frequency shift keying (FSK) transceiver intended for use in half-duplex, bidirectional RF links. The multi-channeled FSK transceiver is intended for UHF radio equipment in compliance with the North American Federal Communications Commission (FCC) part 15.247 and 249, as well as the European Telecommunication Standard Institute (ETSI) specification, EN300 220.

The transmitter consists of a PLL frequency synthesizer and a power amplifier. The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual modulus prescaler, programmable frequency dividers, and a phase-detector. The loop-filter is external for flexibility and can be a simple passive circuit. The output power of the power amplifier can be programmed to seven levels. A lock-detect circuit detects when the PLL is in lock. In receive mode, the PLL synthesizer generates the local oscillator (LO) signal. The N, M , and A values that give the LO frequency are stored in the N0, M0, and A0 registers.

The receiver is a zero intermediate frequency (IF) type which makes channel filtering possible with low-power, integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel includes a pre-amplifier, a third order Sallen-Key RC low-pass filter that protects the following switched-capacitor filter from strong adjacent channel signals, and a limiter. The main channel filter is a switched-capacitor implementation of a six-pole elliptic low pass filter. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 100kHz, 150kHz, 230kHz, and 340kHz. The I and Q channel outputs are demodulated and produce a digital data output. The demodulator detects the relative phase of the I and the Q channel signal. If the I channel signal lags behind the Q channel, the FSK tone frequency is above the LO frequency (data ‘1’). If the I channel leads the Q channel, the FSK tone is below the LO frequency (data ‘0’). The output of the receiver is available on the DataIXO pin. A receive signal strength indicator (RSSI) circuit indicates the received signal level. All support documentation can be found on Micrel’s web site at www.micrel.com.

Features

- True single chip transceiver
- Digital bit synchronizer
- Received signal strength indicator (RSSI)
- RX and TX power management
- Power down function
- Reference crystal tuning capabilities
- Baseband shaping
- Three-wire programmable serial interface
- Register read back function

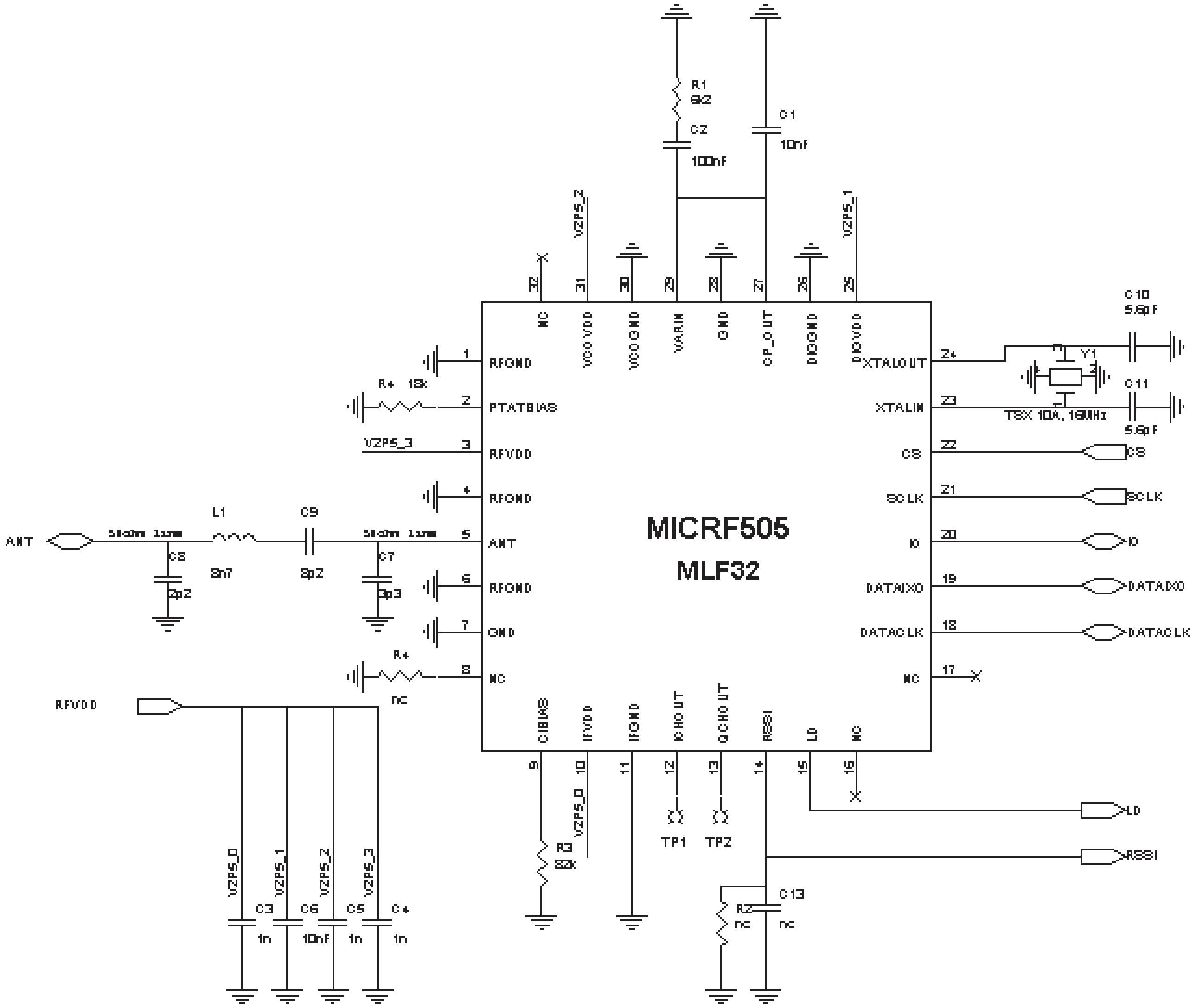
Applications

- Telemetry
- Remote metering
- Wireless controller
- Remote data repeater
- Remote control systems
- Wireless modem
- Wireless security system

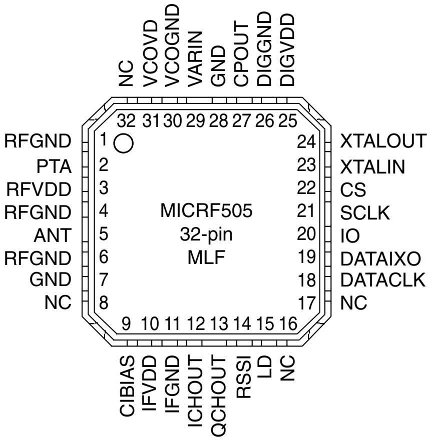
Ordering Information

Part Number	Junction Temp. Range	Package
MICRF505BML	–40°C to +85°C	32-Pin MLF™

Typical Application



Pin Configuration



32-Pin MLF™

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	RFGND		LNA and PA ground.
2	PTATBIAS	O	Connection for bias resistor.
3	RFVDD		LNA and PA power supply.
4	RFGND		LNA and PA ground.
5	ANT	I/O	Antenna In/Output
6	RFGND		LNA and PA ground.
7	RFGND		LNA and PA ground.
8	NC		No connect.
9	CIBIAS	O	Connection for bias resistor.
10	IFVDD		IF/mixer power supply.
11	IFGND		IF/mixer ground.
12	ICHOUT	O	Test pin.
13	QCHOUT	O	Test pin.
14	RSSI	O	Received signal strength indicator.
15	LD	O	PLL lock detect.
16	NC		No connect.
17	NC		No connect.
18	DATACLK	O	RX/TX data clock output.
19	DATAIXO	I/O	RX/TX data input/output.
20	IO	I/O	3-wire interface data in/output
21	SCLK	I	3-wire interface serial clock.
22	CS	I	3-wire interface chip select.
23	XTALIN	I	Crystal oscillator input.
24	XTALOUT	O	Crystal oscillator output.
25	DIGVDD		Digital power supply.
26	DIGGND		Digital ground.
27	CPOUT	O	PLL charge pump output.
28	GND		Substrate ground.
29	VARIN	I	VCO varactor input.
30	VCOGND		VCO ground.
31	VCOVDD		VCO power supply.
32	NC		No connect.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD})	+3.3V
Voltage on any pin (GND = 0V)	–0.3V to 2.7V
Lead Temperature (soldering, 4 sec.)	TBD°C
Storage Temperature (T_S)	–55°C to +150°C
ESD Rating[3]	**2kV**

Operating Ratings[2]

Supply Voltage (V_{IN})	+2.0V to +2.5V
RF Frequencies	850MHz to 950MHz
Data Rate (NRZ)	< 200kBaud
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance MLF™ (θ_{JA}) multi-layer board	41.7°C/W

Electrical Characteristics[4]

f_{RF} = 915MHz, Data-rate = 125kbps, Modulation type = closed-loop VCO modulation, V_{DD} = 2.5V; T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	RF Frequency Operating Range		**850**		**950**	MHz
	Power Supply		**2.0**		**2.5**	V
	Power Down Current			0.3		µA
	Standby Current			280		µA
VCO and PLL Section						
	Reference Frequency		**4**		**40**	MHz
	PLL Lock Time 3kHz bandwidth	915MHz to 915.5MHz		0.5		ms
		902MHz to 927MHz		1.7		ms
		20kHz bandwidth		0.3		ms
	Switch Time 3kHz loop bandwidth	Rx – Tx		0.6		ms
		Tx – Rx		0.6		ms
		Standby Rx		1.1		ms
		Standby Tx		1.2		ms
	Crystal Oscillator Start-Up Time	16MHz, 9pF load, 5.6pF loading capacitors		1.2		ms
	Charge Pump Current	VCP_{OUT} = 1.1V, CP_HI = 0		125		µA
		VCP_{OUT} = 1.1V, CP_HI = 1		500		µA
	Charge Pump Tolerance			20		%
Transmit Section						
	Output Power	R_{LOAD} = 50Ω, Pa2-0-111		10		dBm
		R_{LOAD} = 50Ω, Pa2-0-001		–8		dBm
	Output Power Tolerance	Over temperature range		2		dB
		Over power supply range		3		dB
	Tx Current Consumption	R_{LOAD} = 50Ω, Pa2-0-111		28		mA
		R_{LOAD} = 50Ω, Pa2-0-001		14		mA
	Tx Current Consumption Variation	10dBm		2.5		mA
	Binary FSK Frequency Separation[5]	bitrate = 200kbps	**20**		**500**	kHz
	Data Rate[5]	VCO modulation	**20**		**200**	kbps
	Occupid bandwidth	20kbps, β = 2, 20dBc				kHz
		125kbps, β = 2, 20dBc				kHz
		200kbps, β = 2, 20dBc				kHz
	2nd Harmonic			**–25**		dBm
	3rd Harmonic			**–15**		dBm
	Spurious Emission < 1GHz[5]				< –54	dBm
	Spurious Emission < 1GHz[5]				< –30	dBm

Symbol	Parameter	Condition	Min	Typ	Max	Units
Receive Section						
	Rx Current Consumption			13.5		mA
		LNA bypass		11.5		mA
		Switch cap filter bypass with LNA		11.5		mA
	Rx Current Consumption Variation	Over temperature		4		mA
	Receiver Sensitivity	2.4kbps, β = 16		–111		dBm
		4.8kbps, β = 16		–109		dBm
		19.2kbps, β = 4		–105		dBm
		38.4kbps, β = 4		–103		dBm
		76.8kbps, β = 2		–101		dBm
		125kbps, β = 2		–99		dBm
		200kbps, β = 2		–97		dBm
	Receiver Maximum Input Power	125kbps, 125kHz deviation		–12		dBm
		20kbps, 20kHz deviation		–20		dBm
	Receiver Sensitivity Tolerance	Over temperature		4		dB
		Over power supply range		1		dB
	Receiver Bandwidth		50		340	kHz
	Co-Channel Rejection					dB
	Adjacent Channel Rejection	200kHz spacing				
		500kHz spacing				
		1MHz spacing				
	Blocking	±1MHz		42		dB
		±2MHz		47		dB
		±5MHz		38		dB
		±10MHz		41		dB
	Noise Figure, Cascade			tbd		dB
	1dB Compression			–35		dB
	Input IP3	2 tones with 1MHz separation		–25		dBm
	Input IP2					dBm
	LO Leakage				–90	dBm
	Spurious Emission	< 1GHz			–54	dBm
		> 1GHz			–54	dBm
	Input Impedance[5]			~50		Ω
	Input Reflection (s11)[5]			–20	–15	dB
	RSSI Dynamic Range			50		dB
	RSSI Output Voltage	Pin = 100dBm		0.9		V
		Pin = 60dBm		1.85		V

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital Inputs/Outputs						
V_{IH}	Logic Input High		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Logic Input Low		0		$0.3V_{DD}$	V
	Clock/Data Frequency[5]				10	MHz
	Clock/Data Duty Cycle[5]		45		55	%

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.
5. Guaranteed by design.

Programming

General

The MICRF505 functions are enabled through a number of programming bits. The programming bits are organized as a set of addressable control registers, each register holding 8 bits.

There are 23 control registers in total in the MICRF505, and they have addresses ranging from 0 to 22. The user can read all the control registers. The user can write to the first 22 registers (0 to 21); the register with address 22 is a read-only register.

All control registers hold 8 bits and all 8 bits must be written to when accessing a control register, or they will be read. Some of the registers do not utilize all 8 bits. The value of an unused bit is "don't care."

The control register with address 0 is referred to as ControlRegister0, the control register with address 1 is ControlRegister1 and so on. A summary of the control registers is given in the table below. In addition to the unused bits (marked with "-") there are a number of fixed bits (marked with "0" or "1"). Always maintain these as shown in the table.

The control registers in MICRF505 are accessed through a 3-wire interface; clock, data and chip select. These lines are referred to as SCLK, IO, and CS, respectively. This 3-wire interface is dedicated to control register access and is referred to as the control interface. Received data (via RF) and data to transmit (via RF) are handled by the DataIXO and DataClk (if enabled) lines; this is referred to as the data interface.

The SCLK line is applied externally; access to the control registers are carried out at a rate determined by the user. The MICRF505 will ignore transitions on the SCLK line if the CS line is inactive. The MICRF505 can be put on a bus, sharing clock and data lines with other devices.

All control registers should be initiated (written to) following a power-on. During operation, however, writing to one register is sufficient to change the way the transceiver works.

Adr	Data							
A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	Load_en
0000001	Modulation1	Modulation0	‘0’	‘0’	RSSI_en	LD_en	PF_FC1	PF_FC0
0000010	CP_HI	‘0’	‘0’	‘0’	OUTS3	OUTS2	OUTS1	OUTS0
0000011	‘1’	‘1’	‘0’	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0
0000100	Mod_F2	Mod_F1	Mod_F0	Mod_I4	Mod_I3	Mod_I2	Mod_I1	Mod_I0
0000101	-	-	‘0’	‘1’	Mod_A3	Mod_A2	Mod_A1	Mod_A0
0000110	-	Mod_clkS2	Mod_clkS1	Mod_clkS0	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0
0001000	‘1’	ScClk_X2	ScClk5	ScClk4	ScClk3	ScClk2	ScClk1	ScClk0
0001001	‘0’	‘0’	‘1’	XCOtune4	XCOtune3	XCOtune2	XCOtune1	XCOtune0
0001010	-	-	A0_5	A0_4	A0_3	A0_2	A0_1	A0_0
0001011	-	-	-	-	N0_11	N0_10	N0_9	N0_8
0001100	N0_7	N0_6	N0_5	N0_4	N0_3	N0_2	N0_1	N0_0
0001101	-	-	-	-	M0_11	M0_10	M0_9	M0_8
0001110	M0_7	M0_6	M0_5	M0_4	M0_3	M0_2	M0_1	M0_0
0001111	-	-	A1_5	A1_4	A1_3	A1_2	A1_1	A1_0
0010000	-	-	-	-	N1_11	N1_10	N1_9	N1_8
0010001	N1_7	N1_6	N1_5	N1_4	N1_3	N1_2	N1_1	N1_0
0010010	-	-	-	-	M1_11	M1_10	M1_9	M1_8
0010011	M1_7	M1_6	M1_5	M1_4	M1_3	M1_2	M1_1	M1_0
0010100	‘1’	‘0’	‘1’	‘1’	‘0’	‘1’	‘0’	‘1’
0010101	-	-	-	-	FEEC_3	FEEC_2	FEEC_1	FEEC_0
0010110	FEE_7	FEE_6	FEE_5	FEE_4	FEE_3	FEE_2	FEE_1	FEE_0

Table 1. Control Registers in MICRF505

Names of programming bits, unused bits (“-”) and fixed bits (“1” or “0”) are shown. The control register with address 0 is referred to as ControlRegister0 etc.

Writing to the control registers in MICRF505

Writing: A number of octets are entered into MICRF505 followed by a load-signal to activate the new setting. Making these events is referred to as a “write sequence.” It is possible to update all, 1, or n control registers in a write sequence. The address to write to (or the first address to write to) can be any valid address (0-21). The IO line is always an input to the MICRF505 (output from user) when writing.

What to write:

- The address of the control register to write to (or if more than 1 control register should be written to, the address of the 1st control register to write to)
- A bit to enable reading or writing of the control registers. This bit is called the R/W bit.
- The values to write into the control register(s)

Field	**Comments**
Address:	A 7 bit field, ranging from 0 to 21. MSB is written first.
R/W bit:	A 1-bit field, = “0” for writing
Values:	A number of octetes (1-22 octetes). MSB in every octet is written first. The first octet is written to the control register with the specified address (="Adress"). The next octet (if there is one) is writtento the control register with address= "Adress + 1" and so on.

Table 2.

How to write:

Bring CS active to start a write sequence. The active state of the CS line is "high." Use the SCLK/IO serial interface to clock "Address" and "R/W bit and "Values" into the MICRF505. MICRF505 will sample the IO line at negative edges of SCLK. Make sure to change the state of the IO line before the negative edge. Refer to figures below.

Bring CS inactive to make an internal load-signal and complete the write-sequence. Note: There is an exception to this point. If the programming bit called "load_en" (bit0 in ControlRegister0) is "0", then no load pulse is generated.

The two different ways to "program the chip" are:

- Write to a number of control registers (0-22) when the registers have incremental addresses (write to 1, all, or n registers)
- Write to a number of control registers when the registers have non-incremental addresses

Writing to a Single Register

Writing to a control register with address "A6, A5, ... A0" is described here. During operation, writing to 1 register is sufficient to change the way the transceiver works. Typical example: Change from receive mode to power-down.

Field	Comments
Address:	7 bit = A6, A5, ... A0 (A6 = msb, A0 = lsb)
R/W bit:	"0" for writing
Values:	8 bits = D7, D6, ... D0 (D7 = msb, D0 = lsb)

Table 3. "Address" and "R/W bit" together make 1 octet. In addition, 1 octet with programming bits is entered. Totally, 2 octets are clocked into the MICRF505.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 2 octets
- Bring CS low

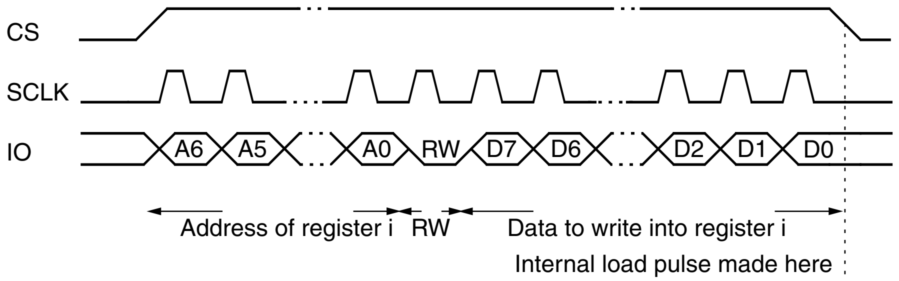


Figure 1.

In Figure 1, IO is changed at positive edges of SCLK. The MICRF505 samples the IO line at negative edges. The value of the R/W bit is always "0" for writing.

Writing to All Registers

After a power-on, all writable registers should be written. This is described here.

Writing to all registers can be done at any time. To get the simplest firmware, always write to all registers. The price to pay for the simplicity is increased write-time, which leads to increased time to change the way the MICRF505 works.

What to write

Field	Comments
Address:	'0000000' (address of the first register to write to, which is 0)
R/W bit:	"0" for writing
Values:	1st Octet: wanted values for ControlRegister0. 2nd octet: wanted values for ControlRegister1 and so on for all of the octets. So the 22nd octet wants values for ControlRegister21. Refer to the specific sections of this document for actual values.

Table 4. "Address" and "R/W bit" together make 1 octet. In addition, 22 octets with programming bits are entered. Totally, 23 octets are clocked into the MICRF505.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 23 octets
- Bring CS low

Refer to the figure in the next section, "Writing to n registers having incremental addresses".

Writing to n registers having incremental addresses

In addition to entering all bytes, it is also possible to enter a set of n bytes, starting from address i = "A6, A5, ... A0." Typical example: Clock in a new set of frequency dividers (i.e. change the RF frequency). "Incremental addresses": Registers to be written are located in i, i+1, i+2 ...

What to write

Field	Comments
Address:	7 bit = A6, A5, ... A0 (A6 = msb, A0 = lsb) (address of first byte to write to)
R/W bit:	"0" for writing
Values:	n* 8 bits = D7, D6, ... D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i") D7, D6, ... D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i+1") ... D7, D6, ... D0 (D7 = msb, D0 = lsb) (written to control reg. with address "i+n-1 ")

Table 5. "Address" and "R/W bit" Together Make 1 Octet.
In addition, n octets with programming bits are entered. Totally, 1 + n octets are clocked into the MICRF505.

How to write:

- Bring CS high
- Use SCLK and IO to clock in the 1 + n octets
- Bring CS low

In Figure 1, n = 2 (write to 2 registers in the MICRF505). In the figure, IO is changed at positive edges of SCLK. The MICRF505 samples the IO line at negative edges. The value of the R/W bit is always "0" for writing.

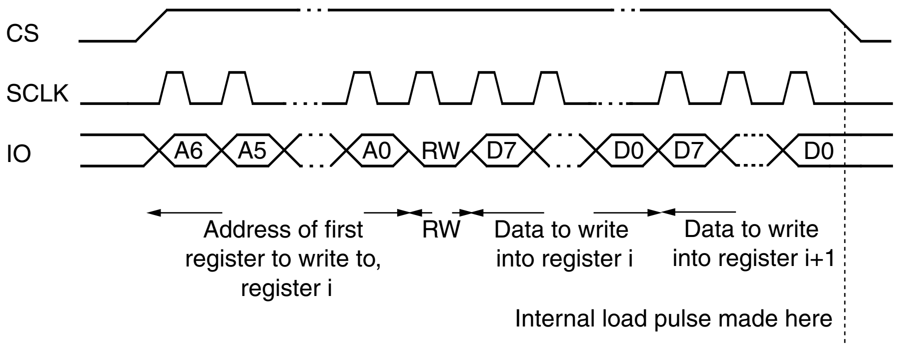

CS
SCLK
IO
A6
A5
A0
RW
D7
D0
D7
D0
Address of first register to write to, register i
RW
Data to write into register i
Data to write into register i+1
Internal load pulse made here

Figure 2.

Writing to n Registers having Non-Incremental Addresses

Registers with non-incremental addresses can be written to in one write-sequence as well. Example of non-incremental addresses: “0,1,3”. However, this requires more overhead, and the user should consider the possibility to make a “continuous” update, for example, by writing to “0,1,2,3” (writing the present value of “2” into “2”). The simplest firmware is achieved by always writing to all registers. Refer to previous sections.

This write-sequence is divided into several sub-parts:

- Disable the generation of load-signals by clearing bit “load_en” (bit0 in ControlRegister0)
- Repeat for each group of registers having incremental addresses:
  - Bring CS active
  - Enter first address for this group, R/W bit and values
  - Bring CS inactive
  - Finally, enable and make a load-signal by setting “load_en”

Refer to the previous sections for how to write to 1 or n (with incremental addresses) registers in the MICRF505.

Reading from the control registers in MICRF505

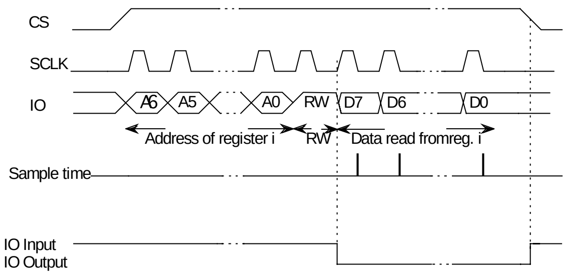
The “read-sequence” is:

1. Enter address and R/W bit
2. Change direction of IO line
3. Read out a number of octets and change IO direction back again.

It is possible to read all, 1 or n registers. The address to read from (or the first address to read from) can be any valid address (0-22). Reading is not destructive, i.e. values are not changed. The IO line is output from the MICRF505 (input to user) for a part of the read-sequence. Refer to procedure description below.

A read-sequence is described for reading n registers, where n is a number 1-23.

Reading n registers from MICRF505



In the figure, 1 register is read. The address is A6, A5, ... A0. A6=msb. The data read out is D7, D6, ... D0. The value of the R/W bit is always “1” for reading.

SCLK and IO together form a serial interface. SCLK is applied externally for reading as well as for writing.

- Bring CS active
- Enter address to read from (or the first address to read from) (7 bits) and
- The R/W bit = 1 to enable reading
- Make the IO line an input to the user (set pin in tristate)
- Read n octets. The first rising edge of SCLK will set the IO as an output from the MICRF505. MICRF will change the IO line at positive edges. The user should read the IO line at the negative edges.
- Bring CS inactive. This will make the IO line an input to the MICRF505 again
- Make the IO line an output from the user again.

Programming interface timing

Figure 4 and Table 6 shows the timing specification for the 3-wire serial programming interface.

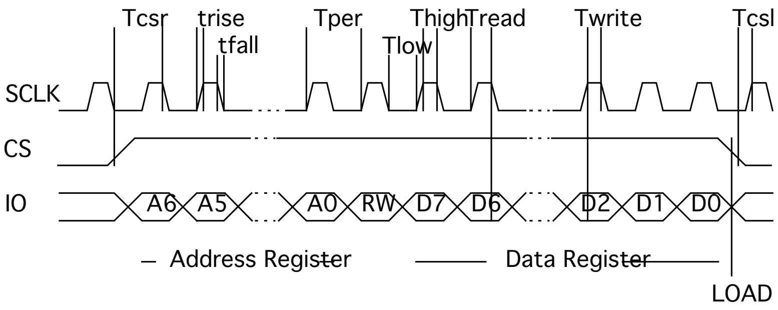


Figure 4.

Symbol	Parameter	Values			Units
		Min.	Typ.	Max.	
Tper	Min. period of SCLK	50			ns
Thigh	Min. high time of SCLK	20			ns
Tlow	Min. low time of SLCK	20			ns
tfall	Max. time of falling edge of SLCK			1	µs
trise	Max. time of rising edge of SLCK			1	µs
Tcsr	Min. delay from rising edge of CS to falling edge of SCLK	0			ns
Tcsf	Min. delay from falling edge of CS to rising edge of SCLK	5			ns
Twrite	Min. delay from valid IO to falling edge of SCLK during a write operation	0			ns
Tread	Min. delay from rising edge of SCLK to valid IO during a read operation (assuming load capacitance of IO is 25 pF)	75			ns

Table 6. Timing Specification for the 3-Wire Programming Interface

Programming summary

- Use CS, SCLK, and IO to get access to the control registers in MICRF505.
- SCLK is user-controlled.
- Write to the MICRF505 at positive edges (MICRF 505 reads at negative edges).
- Read from the MICRF505 at negative edges (MICRF505 writes at positive edges).
- After power-on: Write to the complete set of control registers
- Address field is 7 bits long. Enter msb first
- R/W bit is 1 bit long (“1” for read, “0” for write)
- Address and R/W bit together make 1 octet
- All control registers are 8 bits long. Enter/read msb in every octet first
- Always write 8 bits to/read 8 bits from a control register. This is the case for registers with less than 8 used programming bits as well.
- Writing: Bring CS high, write address and R/W bit followed by the new values to fill into the addressed control register(s) and bring CS low for loading, i.e. activation of the new control register values (“load_en” = 1).
- Reading: Bring CS high, write address and R/W bit, set IO as an input, read present contents of the addressed control register(s), bring CS low and set IO as an output.

Frequency Synthesizer

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0001010	-	-	A0_5	A0_4	A0_3	A0_2	A0_1	A0_0
0001011	-	-	-	-	N0_11	N0_10	N0_9	N0_8
0001100	N0_7	N0_6	N0_5	N0_4	N0_3	N0_2	N0_1	N0_0
0001101	-	-	-	-	M0_11	M0_10	M0_9	M0_8
0001110	M0_7	M0_6	M0_5	M0_4	M0_3	M0_2	M0_1	M0_0
0001111	-	-	A1_5	A1_4	A1_3	A1_2	A1_1	A1_0
0010000	-	-	-	-	N1_11	N1_10	N1_9	N1_8
0010001	N1_7	N1_6	N1_5	N1_4	N1_3	N1_2	N1_1	N1_0
0010010	-	-	-	-	M1_11	M1_10	M1_9	M1_8
0010011	M1_7	M1_6	M1_5	M1_4	M1_3	M1_2	M1_1	M1_0

The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual modulus prescaler, programmable frequency dividers and a phase-detector. The loop-filter is external for flexibility and can be a simple passive circuit. The lengths of the N and M and A registers are 12, 12 and 6 bits respectively. The M, N and A values can be calculated from the formula:

$$f_{PhD} = \frac{f_{XCO}}{M} = \frac{f_{VCO/2}}{16 \times N + A} = \frac{f_{RF}}{16 \times N + A}$$

where PhD is the phase detector comparison frequency.

PhD: Phase detector comparison frequency

fxco: Crystal oscillator frequency

fvco: Voltage controlled oscillator frequency

There are two sets of each of the divide factors (i.e. A0 and A1). If modulation by using the dividers is selected (that is Modulation1=1, Modulation0=0), the two sets should be programmed to give two RF frequencies, separated by two times the specified frequency deviation. For all other modulation methods, and also in receive mode, the 0-set will be used.

Crystal Oscillator (XCO)

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0001001	‘0’	‘0’	‘1’	XCOtune4	XCOtune3	XCOtune2	XCOtune1	XCOtune0

The crystal oscillator is a very critical block. As the crystal oscillator is a reference for the RF output frequency and also for the LO frequency in the receiver, very good phase and frequency stability is required. The schematic of the crystal oscillator’s external components for 16MHz are shown in Figure 2.

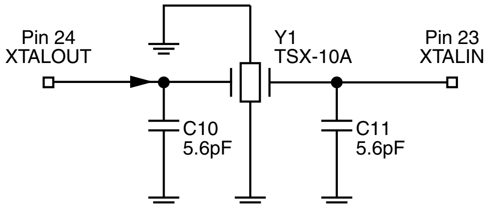


Figure 5. Crystal Oscillator Circuit

The crystal should be connected between pins XoscIn and XoscOut (pin 23 and 24). In addition, loading capacitors for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The load capacitance seen between the crystal terminals should be equal to C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{10}} + \frac{1}{C_{11}}} + C_{parasitic}$$

The parasitic capacitance is the pin input capacitance and PCB stray capacitance. Typically the total parasitic capacitance is around 6pF. For instance, for a 9pF load crystal the recommended values of the external load capacitors are 5.6pF.

It is also possible to tune the crystal oscillator internally by switching in internal capacitance using 5 tune bits XCOtune4 - XCOtune0. When XCOtune4 - XCOtune0 = 0 no internal capacitors are connected to the crystal pins. When XCOtune4 - XCOtune0 = 1 all of the internal capacitors are connected to the crystal pins. Figure 3 shows the tuning range for two different capacitor values, these are 1.5pF and no capacitors. The crystal used is a TN4-26011 from Toyocom. Specification: Package TSX-10A, Nominal frequency 16.000000 MHz, frequency tolerance ±10ppm, frequency stability ±9ppm, load capacitance 9pF, pulling sensitivity 15ppm/pF.

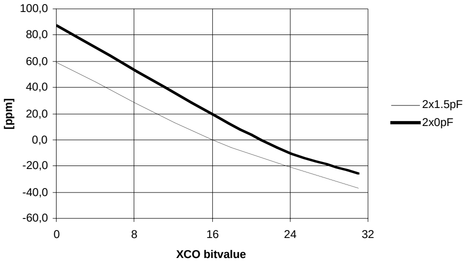


Figure 6. XCO Tuning

The start up time is given in Table 7. As can be seen, more capacitance will slow down the start up time.

The start-up time of a crystal oscillator is typically around a millisecond. Therefore, to save current consumption, the XCO is turned on before any other circuit block. During start-up the XCO amplitude will eventually reach a sufficient level to trigger the M-counter. After counting 2 M-counter output pulses the rest of the circuit will be turned on. The current consumption during the prestart period is approximately 280µA.

XCO Bitvalue	Start-up Time (ms)
0	590
1	590
2	700
4	700
8	810
16	1140
31	2050

Table 7. Typical values with C_{EXT}= 1.5pF

If an external reference shall be used instead of a crystal, the signal shall be applied to pin 24, XtalOut. Due to internal DC setting in the XCO, an AC coupling is recommended to be used between the external reference and the XtalOut-pin.

VCO

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000011	'1'	'1'	'0'	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0

The VCO has no external components. It has three bit to set the bias current and two bit to set the VCO frequency. These five bit are set by the RF frequency, as follows:

RF freq.	VCO_IB2	VCO_IB1	VCO_IB0	VCO_freq1	VCO_freq0
850MHz	1	1	1	0	0
868MHz	0	1	1	0	1
915MHz	0	0	1	1	0
950MHz	0	0	0	1	1

Table 8. VCO Bit Setting

The bias bit will optimize the phase noise, and the frequency bit will control a capacitor bank in the VCO. The tuning range, the RF frequency versus varactor voltage, is dependent on the VCO frequency setting, and can be shown in Figure 4. When the tuning voltage is in the range from 0.9V to 1.4V, the VCO gain is at its maximum, approximately 65 to 70MHz/V. It is recommended that the varactor voltage stays in this range.

The input capacitance at the varactor pin must be taken into considerations when designing the PLL loop filter. This is most critical when designing a loop filter with high bandwidth, which gives relatively small component values. The input capacitance is approximately 6pF.

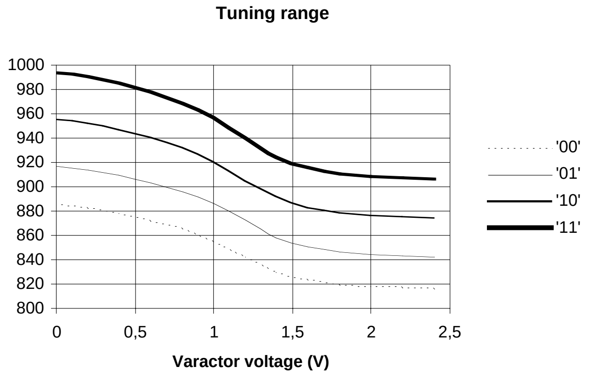


Figure 7. RF Frequency vs. Varactor Voltage and VCO Frequency bit (V_{DD} = 2.25V)

Charge Pump

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000011	CP_HI	‘0’	‘0’	‘0’	OUTS3	OUTS2	OUTS1	OUTS0

The charge pump current can be set to either 125µA or 500µA by CP_HI (‘1’ D 500µA). This will affect the loop filter component values, see “PLL Filter” section. In most cases, the lowest current is best suited. For applications using a high phase detector frequency and a high PLL bandwidth, the 500µA can be a better choice.

PLL Filter

The design of the PLL filter will strongly affect the performance of the frequency synthesizer. The PLL filter is kept externally for flexibility. Input parameters when designing the loop filter for the MICRF505 are mainly the modulation method and the bit rate. These choices will also affect the switching time and phase noise.

The frequency modulation can be done in two different ways with the MICRF505, either by VCO modulation or by modulation with the internal dividers (see chapter Frequency modulation for further details). In the first case, the PLL bandwidth needs to be adequately low not to cancel the modulation. In the second case, using the dividers, the PLL needs to lock on a new carrier frequency for every new data bit. Now the PLL bandwidth needs to be adequately high. It may be necessary to use a third order filter to suppress the phase detector frequency, as this is not suppressed as much as when doing modulation on the VCO.

A schematic for a second and third order loop filter is shown in Figure 5. For a second order filter, C3 is not connected and R2 is 0 Ω.

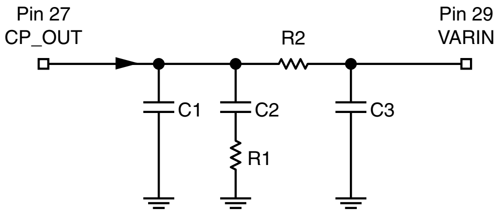


Figure 8. Second and Third Order Loop Filter

Table 9 shows three different loop filters, the two first for VCO modulation and the last one for modulation using the internal dividers. The component values are calculated with RF frequency = 915MHz, VCO gain = 67MHz/V and charge pump current = 125µA. Other settings are shown in the table. The varactor pin capacitance (pin 29) of 6pF does not influence on the component values for the two filters with lowest bandwidth. For the 12kHz bandwidth filter, a third order loop filter is calculated. The third pole is set by R2×C3. Here C3 is chosen to be 6pF, the same as the varactor input pin capacitance (pin 29). C3 can therefore be skipped.

	Baud Rate (kbaud/sec)	PLL BW (kHz)	Phase Margin (°)	Phase Detector Freq. (kHz)	C1	C2	R1	R2	C3
VCO	>20	0.8	56	500	56nF	560nF	1.2kΩ	0	NC
VCO	>125	3	56	500	3.9nF	560nF	4.7kΩ	0	NC
Internal	>10	12	65	300	56nF	560pF	27kΩ	220kΩ	NC

Table 9. Loop Filter Components Values

Lock Detect

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	Modulation1	Modulation0	"0"	"0"	RSSI_en	LD_en	PF_FC1	PF_FC0

A lock detector can be enabled by setting LD_en = 1. When pin LD is high, it indicates that the PLL is in lock.

Modes of Operation

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	Load_en

Mode1	Mode0	State	Comments
0	0	Power down	Keeps register configuration
0	1	Standby	Only crystal oscillator running
1	0	Receive	Full receive
1	1	Transmit	Full transmit ex PA stage

Transceiver Sync/Non-Synchronous Mode

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	Load_en
0000110	–	Mod_clkS2	Mod_clkS1	Mod_clkS0	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0

Sync_en	State	Comments
0	Rx: Bit synchronization off	Transparent reception of data
0	Tx: DataClk pin off	Transparent transmission of data
1	Rx: Bit synchronization on	Bit-clock is generated by transceiver
1	Tx: DataClk pin on	Bit-clock is generated by transceiver

When Sync_en = 1, it will enable the bit synchronizer in receive mode. The bit synchronizer clock needs to be programmed, see chapter Bit synchronizer. The synchronized clock will be set out on pin DataClk.

In transmit mode, when Sync_en = 1, the clock signal on pin DataClk is a programmed bit rate clock. Now the transceiver controls the actual bit rate. The data to be transmitted will be sampled on rising edge of DataClk. The micro controller can therefore use the negative edge to change the data to be transmitted. The clock used for this purpose, BitRate-clock, is programmed in the same way as the modulator clock and the bit synchronizer clock:

$$f_{BITRATE\_CLK} = \frac{f_{XCO}}{Refclk\_K \times 2^{\left(7-BITRATE\_clkS\right)}}$$

where:

fBITRATE_CLK: The clock frequency used to control the bit rate, should be equal to the bit rate (a bit rate of 20 kbit/sec requires a clock frequency of 20kHz)

fxco: Crystal oscillator frequency

Refclk_K: 6 bit divider, values between 1 and 63

BitRate_clkS: Bit rate setting, values between 0 and 6

Data Interface

The MICRF505 interface can be divided in to two separate interfaces, a "programming interface" and a "Data interface". The "programming interface" has a three wire serial programmable interface and is described in chapter Programming.

The "data interface" can be programmed to sync-/non-synchronous mode. In synchronous mode the MICRF505 is defined as "Master" and provides a data clock that allows users to utilize low cost micro controller reference frequency.

The data interface is defined in such a way that all user actions should take place on falling edge and is illustrated Figure 6 and 7. The two figures illustrate the relationship between DATACLK and DATAIXO in receive mode and transmit mode.

MICRF505 will present data on rising edge and the "USER" sample data on falling edge in receive mode.

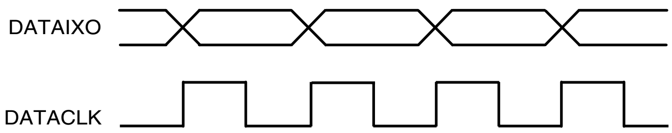


Figure 9. Data interface in Receive Mode

The User presents data on falling edge and MICRF505 samples on rising edge in transmit mode.

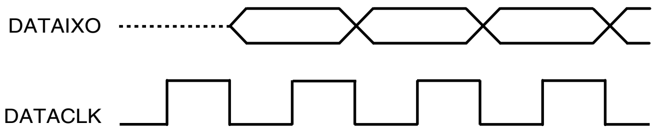


Figure 10. Data interface in Transmit Mode

When entering transmit mode it is important to keep DATAIXO in tri-state from the time Tx-mode is entered until user starts sending data. The data is provided directly to the modulation circuit and violation of this may/will cause abnormal behavior. Depending on the chosen FSK modulation some sort of encoding might be needed. The different modulation types and encoding is described in chapter Frequency modulation.

Receiver

The receiver is a zero intermediate frequency (IF) type in order to make channel filtering possible with low-power integrated low-pass filters. The receiver consists of a low noise amplifier (LNA) that drives a quadrature mixer pair. The mixer outputs feed two identical signal channels in phase quadrature. Each channel include a pre-amplifier, a third order Sallen-Key RC lowpass filter that protects the following switched-capacitior filter from strong adjacent channel signals and finally a limiter. The main channel filter is a switched-capacitor implementation of a six-pole elliptic lowpass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the Sallen-Key RC filter can be programmed to four different frequencies: 100kHz, 150kHz, 230kHz and 340kHz. The demodulator demodulates the I and Q channel outputs and produces a digital data output. It detects the relative phase of the I and the Q channel signal. If the I channel signal lags the Q channel, the FSK tone frequency lies above the LO frequency (data '1'). If the I channel leads the Q channel, the FSK tone lies below the LO frequency (data '0'). The output of the receiver is available on the DataIXO pin. A RSSI circuit (receive signal strength indicator) indicates the received signal level.

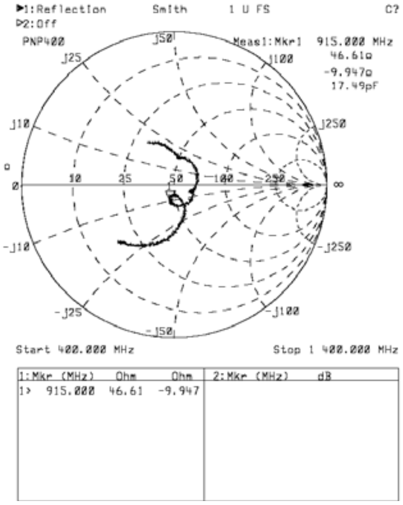
Front End

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000011	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	Load_en

A low noise amplifier in RF receivers is used to boost the incoming signal prior to the frequency conversion process. This is important in order to prevent mixer noise from dominating the overall front-end noise performance. The LNA is a two-stage amplifier and has a nominal gain of approximately 23dB at 900MHz. The front end has a gain of about 33dB to 35dB. The gain varies by 1-1.5dB over a 2.0V to 2.5V variation in power supply.

The LNA can be bypassed by setting bit LNA_by to '1'. This can be useful for very strong input signal levels. The front-end gain with the LNA bypassed is about 9-10dB. The mixers have a gain of about 10dB at 900MHz. The differential outputs of the mixers can be made available at pins IchOut and QchOut. The output impedance of each mixer is about 8kΩ.

The input impedance is close to 50kΩ as shown in Figure 8, giving an input reflection of about -20dB. The receiver does not require any matching network.



1:Mkr (MHz)	Ohm	Ohm	2:Mkr (MHz)	dB
1> 915.000	46.61	-9.947		

Figure 11. LNA Input Impedance

Sallen-Key Filters

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	Modulation1	Modulation0	"0"	"0"	RSSI_en	LD_en	PF_FC1	PF_FC0

Each channel includes a pre-amplifier and a prefilter, which is a three-pole Sallen-Key lowpass filter. It protects the following switched-capacitor filter from strong adjacent channel signals, and it also works as an anti-aliasing filter. The preamplifier has a gain of 22-23dB. The maximum output voltage swing is about 1.4Vpp for a 2.25V power supply. In addition, the IF amplifier also performs offset cancellation. Gain varies by less than 0.5dB over a 2.0 - 2.5V variation in power supply. The third order Sallen-Key low pass filter is programmable to four different cut-off frequencies according to the table below:

PF_FC1	PF_FC0	Cut-off Freq. (kHz)
0	0	100
0	1	150
1	0	230
1	1	340

Switched Capacitor Filter

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	‘1’	ScClk_X2	ScClk5	ScClk4	ScClk3	ScClk2	ScClk1	ScClk0

The main channel filter is a switched-capacitor implementation of a six-pole elliptic low pass filter. The elliptic filter minimizes the total capacitance required for a given selectivity and dynamic range. The cut-off frequency of the switched-capacitor filter is adjustable by changing the clock frequency.

The clock frequency is designed to be 20 times the cut-off frequency. The clock frequency is derived from the reference crystal oscillator. A programmable 6-bit divider divides the frequency of the crystal oscillator. To generate the correct non-overlapping clock-phases needed by the filter this frequency is then divided by 4. The cut-off frequency of the filter is given by:

$$f_{cut} = \frac{f_{XCO}}{80 \cdot \mathrm{ScClk}}$$

when ScClk_X2=0 and

$$f_{cut} = \frac{f_{XCO}}{40 \cdot \mathrm{ScClk}}$$

when ScClk_X2=1 where:

f_{cut}: Filter cutoff frequency

f_{xco}: Crystal oscillator frequency

ScCLK: Switched capacitor filter clock, bits ScClk5-0

For instance, for a crystal frequency of 32MHz and if the 6 bit divider divides the input frequency by 5 the cut-off frequency of the SC filter is 32MHz/(80 × 5) = 80kHz

1st order RC low pass filters are connected to the output of the SC filter to filter the clock frequency.

The lowest cutoff frequency in the pre- and the main channel filter must be set so that the received signal is passed with no attenuation, that is frequency deviation plus modulation. If there are any frequency offset between the transmitter and the receiver, this must also be taken into consideration. A formula for the receiver bandwidth can be summarized as follows;

$$f_{BW} = +f_{OFFSET} + f_{DEV} + \mathrm{Baudrate} / 2$$

where

f_{BW}: Needed receiver bandwidth, fcut above should not be smaller than f_{BW} (Hz)

f_{offset}: Total frequency offset between receiver and transmitter [Hz]

f_{DEV}: Single-sided frequency deviation, see chapter Modulator on how to calculate (Hz)

Baudrate: The baud rate given in bit/sec

RSSI

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	Modulation1	Modulation0	"0"	"0"	RSSI_en	LD_en	PF_FC1	PF_FC0

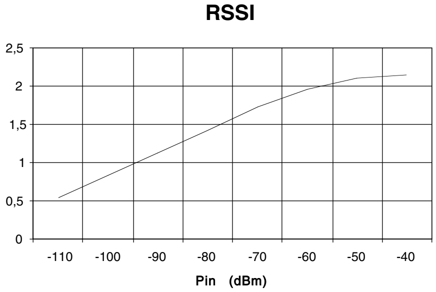


Figure 12. RSSI Voltage

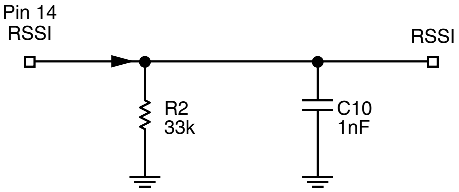


Figure 13. RSSI Network

A typical plot of the RSSI voltage as function of input power is shown in Figure 9. The RSSI has a dynamic range of about 50dB from about -110dBm to -60dBm input power.

The RSSI can be used as a signal presence indicator. When a RF signal is received, the RSSI output increases. This could be used to wake up circuitry that is normally in a sleep mode configuration to conserve battery life.

Another application for which the RSSI could be used is to determine if transmit power can be reduced in a system. If the RSSI detects a strong signal, it could tell the transmitter to reduce the transmit power to reduce current consumption.

FEE

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	—	—	—	—	FEEC_3	FEEC_2	FEEC_1	FEEC_0
0000001	FEE_7	FEE_6	FEE_5	FEE_4	FEE_3	FEE_2	FEE_1	FEE_0

The Frequency Error Estimator (FEE) uses information from the demodulator to calculate the frequency offset between its receive frequency and the transmitter frequency. The output of the FEE can be used to tune the XCO frequency, both for production calibration and for compensation for crystal temperature drift and aging.

The input to the FEE circuit are the up and down pulses from the demodulator. Every time a '1' is updated, an UP-pulse is coming out of the demodulator, and the same with the DN-pulse every time the '0' is updated. The expected no. of pulses for every received symbol are 2 times the(modulation index (Δ).

The FEE can operate in three different modes; counting only UP-pulses, only DN-pulses or counting UP+DN pulses. The no. of received symbols to be counted are either 8, 16, 32 or 64. This is set by the FEEC_0..FEEC_3 control bit, as follows:

FEEC_1	FEEC_0	FEE Mode
0	0	Off
0	1	Counting UP pulses
1	0	Counting DN pulses
1	1	Counting UP and DN pulses. UP increments the counter, DN decrements it.
FEEC_3	**FEEC_2**	**No. of symbols used for the measurement**
0	0	8
0	1	16
1	0	32
1	1	64

Table 10. FEEC Control Bit

The result of the measurement is the FEE value, this can be read from register with address 0010110b. Negative values are stored as a binary no between 00000000 and 11111111. To calculate the negative value, a two's complement of this value must be performed. Only FEE modes where DN-pulses are counted (10 and 11) will give a negative value.

When the FEE value has been read, the frequency offset can be calculated as follows:

Mode UP: $\text{Foffset} = R/(2P)\times(\text{FEE} -\Delta\text{Fp}$

Mode DN: $\text{Foffset} = R/(2P)\times(\text{FEE} +\Delta\text{Fp}$

Mode UP+DN: $\text{Foffset} = R/(4P)\times(\text{FEE}$

where FEE is the value stored in the FEE register, (Fp is the single sided frequency deviation, P is the no. of symbols/data bit counted and R is the symbol/data rate. A positive Foffset means that the received signal has a higher frequency than the receiver frequency. To compensate for this, the receivers XCO frequency should be increased (see ANNEX A) on how to tune the XCO frequency based on the FEE value).

It is recommended to use Mode UP+DN for two reasons, you do not need to know the actual frequency deviation and this mode gives the best accuracy.

Bit Synchronizer

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000110	—	ModclkS2	ModclkS1	ModclkS0	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0

A bit synchronizer can be enabled in receive mode by selecting the synchronous mode (Sync_en=1). The DataClk-pin will output a clock with twice the frequency of the bit rate (a bit rate of 20 kbit/sec gives a DataClk of 20 kHz). A received symbol/bit on DataIXO will be output on rising edge of DataClk. The micro controller should therefore sample the symbol/bit on falling edge of DataClk.

The bit synchronizer uses a clock which needs to be programmed according to the bit rate. The clock frequency should be 16 times the actual bit rate (a bit rate of 20 kbit/sec needs a bit synchronizer clock with frequency of 320 kHz). The clock frequency is set by the following formula:

$$f_{BITSYNC\_CLK} = \frac{f_{XCO}}{\mathrm{Refclk\_K} \times 2^{(7-BITSYNC\_clkS)}}$$

where

$f_{BITSYNC\_CLK}$: The bit synchronizer clock frequency (16 times higher than the bit rate)

f_{XCO}: Crystal oscillator frequency

Refclk_K: 6 bit divider, values between 1 and 63

BitSync_clkS: Bit synchronizer setting, values between 0 and 7

Refclk_K is also used to derive the modulator clock and the bit rate clock.

At the beginning of a received data package, the bit synchronizer clock frequency is not synchronized to the bit rate. When these two are maximum offset to each other, it takes 22 bit/symbols before synchronization is achieved.

Transmitter

Power Amplifier

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000000	LNA_by	PA2	PA1	PA0	Sync_en	Mode1	Mode0	Load_en
0000001	Modulation1	Modulation0	"0"	"0"	RSSI_en	LD_en	PF_FC1	PF_FC0

The maximum output power is approximately 10dBm for a 50Ω load. For maximum output power the load seen by the PA must be resistive. Higher output power can be obtained by decreasing the load impedance. However, this will be in conflict with obtaining impedance match in the LNA. The output power is programmable in seven steps, with approximately 3dB between each step. This is controlled by bits PA2 - PA0. PA2 - PA0 = 1 give the maximum output power.

The power amplifier can be turned off in by settingPA2 - PA0 = 0.

For all other combinations the PA is on and has a maximum power when PA2 - PA0 = 1. The PA has 7 power levels in this case.

The output power vary about 3dB over power supply 2.0V to 2.5V and about 2dB over temperature –40°C to +85°C. The 2nd and 3rd harmonic of the PA are as follows:

2nd harmonic: <-25dBm

3rd harmonic: <-15dBm

To reduce the emission of harmonics, a LC filter can be added between the ANT pin and the antenna as shown in Figure 11.

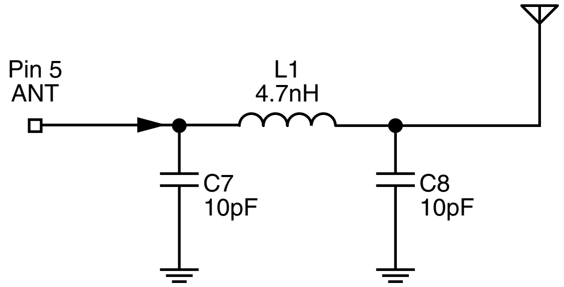


Figure 14. LC Filter

This filter is designed for the 915MHz band with 50Ohm terminations. The component values may have to be tuned to compensate for layout parasitics. This filter may also increase the receiver selectivity.

Frequency Modulation

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000001	Modulation1	Modulation0	‘0’	PA_LDc_en	RSSI_en	LD_en	PF_FC1	PF_FC0

Modulation1	Modulation0	Modulation Type
0	0	Closed loop modulation using modulator
0	1	Not in use
1	0	FSK applied using two sets of dividers
1	1	Not in use

Table 11. Modulation Bit Setting

When Modulation1 and Modulation0 is 00, the modulator needs to be programmed properly, see “Modulator” section. The modulation signal will now be applied directly on the phase locked VCO. It is therefore important that the PLL bandwidth is not too high, as this will remove the modulation. See “PLL Filter” section on how to calculate the PLL components. When using the modulator the modulation signal is applied to the VCO and therefore some sort of encoding is needed.

The level of encoding is determined by the PLL loop filter bandwidth and data rate. Two of the most common encoding techniques are Manchester encoding and 3B4B. Other encoding schemes may also be used.

Manchester encoding is when one bit is encoded in to a two-bit word and is shown in Table 10. When using Manchester encoding the maximum overhead is 100%. When selecting PLL loop filter it is important to note that the min baud rate is equal to:

$$f_{baud\_min} = \frac{baud/s}{4}$$

f_{baud_min}: The minimum frequency of the baud rate (Hz)
baud/s: Elements per second (encoded data)

Data	Word
“0”	“10”
“1”	“01”

Table 12. Manchester Encoding

Another much more efficient encoding type is 3B4B where three data bits are encoded into a four-bit word. The reason for encoding is to minimize the dc component in the modulated data. To have minimum dc component each four bit word should include two elements of “1” and two elements of “0”. Following this guidance only 6 out of 8 word complies and two encoded words needs special precaution. Whenever 000 and 111 data appear, the user must set/clear a flag that indicate if last encoded word was “Word A” and select the respective encoded word shown in Table 11.

Data	Word A	Word B
000	1011	0100
001	1100	
010	0011	
011	1010	
100	0101	
101	1001	
110	0110	
111	1101	0010

Table 13. 3B4B Enconding

Data bits	Encoded words	Comments
000 000 000 000 000	1011 0100 1011 0100 1011	A Flag indicates if “Word A” has been used
111 111 010 110 000	1101 0010 0011 0110 1011	A Flag indicates if “Word A” has been used

Table 14. Example of 3B4B encoding

When Modulation1 Modulation0 is 10, two sets of divider values need to be programmed. The formula for calculating the M,N and A values is given in chapter Frequency synthesizer. The divider values stored in the M0-, N0- and A0-registers will be used when transmitting a ‘0’ and the M1-, N1- and A1-registers will be used to transmit a ‘1’. The difference between the two carrier frequencies corresponds to the double sided frequency modulation. Opposite from the modulation with the modulator, the PLL shall now lock on a new frequency for every change in the transmitted data. The PLL bandwidth therefore needs to be relatively high, higher bit rate requires a higher PLL bandwidth and vice versa.

The data to be transmitted shall be applied to pin DataIXO (see chapter Transceiver sync-/non-synchronous mode on how to use the pin DataClk). The DataIXO pin is set as input in transmit mode and output in receive mode. When set as input, a weak voltage divider will set the level to Vdd/2, when it is not pulled up or down by the controller. When using the modulator, it is important that the DataIXO is kept tristated until the transmission shall begin (when PLL is in lock and the PA is turned on). When DataIXO is tristated, the PLL will lock on the LO frequency (used in receive mode). When DataIXO is set either high or low, the RF frequency will be shifted up or down, centered around the LO-frequency. This is only important when using the modulator, for the other modulation method, if DataIXO is tristated, the M0-, N0 and A0 registers will be used.

Modulator

A6..A0	D7	D6	D5	D4	D3	D2	D1	D0
0000100	Mod_F2	Mod_F1	Mod_F0	Mod_I4	Mod_I3	Mod_I2	Mod_I1	Mod_I0
0000101	—	—	“0”	“1”	Mod_A3	Mod_A2	Mod_A1	Mod_A0
0000110	—	Mod_clkS2	Mod_clkS1	Mod_clkS0	BitSync_clkS2	BitSync_clkS1	BitSync_clkS0	BitRate_clkS2
0000111	BitRate_clkS1	BitRate_clkS0	RefClk_K5	RefClk_K4	RefClk_K3	RefClk_K2	RefClk_K1	RefClk_K0

The modulator will create a waveform with programmable amplitude and frequency. This waveform is fed into a modulation varactor in the VCO which will create the desired frequency modulation. The frequency spectrum can be narrowed by increasing the rise- and fall times of the waveform.

The modulator waveform is created by charging and discharging a capacitor. A modulator clock controls the timing, as shown in Figure 13. For every rise- and fall edge, 4 clock periods are being used. The charging current during these 4 clock periods are not equal, this is to reduce the high-frequency components in the waveform, which in turn will narrow the frequency spectrum.

The frequency deviation can be set in three different ways, as will be explained below. A formula for setting the desired deviation is given at the end of this chapter.

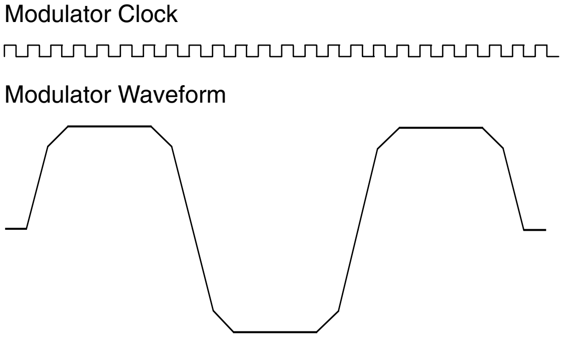


Figure 15. Modulator Waveform and Clock

Modulator Clock

The modulator clock frequency is set by:

$$f_{Mod\_clk} = \frac{f_{XCO}}{Refclk\_K \times 2^{(7\times Mod\_clkS)}}$$

where f_{MOD_CLK} is the modulator clock shown in Figure 13, f_{XCO} is the crystal oscillator frequency, Refclk_K is a 6 bit number and Mod_clkS is a 3 bit number. Mod_clkS can be set to a value between 0 and 7. The modulator clock frequency should be set according to the bit rate and shaping.

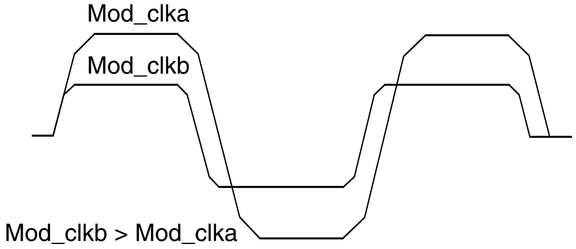


Figure 16. Two Different Modulator Clock Settings

A f_{MOD_CLK} of 8 times the bit rate (as in Figure 14) corresponds to a signal filtered in a gaussian filter with a Bandwidth(Period-product (BT) of 1. When BT is increased, the waveform will be less filtered. Minimum BT is 1 (Mod_clk is 8 times the bitrate). Figure 14 shows two waveforms with BT=1 and BT=2, i.e. the Mod_clk is 8 and 16 times higher than the bit rate. When changing the BT factor, the charge- and discharge times will also be changed, and therefore the frequency deviation, as shown in Figure 15.

Modulator Current

The current used during the rise- and fall times can be programmed with the Mod_I4..Mod_I0 bit, the last one being LSB. Figure 15 shows two waveforms generated with two different currents, where Mod_Ia > Mod_Ib. Higher current will give a higher frequency deviation and vice versa. The effect of modulator clock and MOD_1 is illustrated by

$$f_{DEVIATION} \alpha \frac{MOD\_1}{f_{MOD\_CLK}}$$

To avoid saturation in the modulator it it important not to exceed maximum Mod_I. Max Mod_I for a given fMOD_clk is given by:

$$MOD\_Imax = INT(f\_MOD\_CLK \cdot 28e-6)-1$$

where min() returns the value of the smallest argument and int() returns the integer part of the argument.

where int(x): integer and and f_MOD_CLK: Modulater clk frequency.

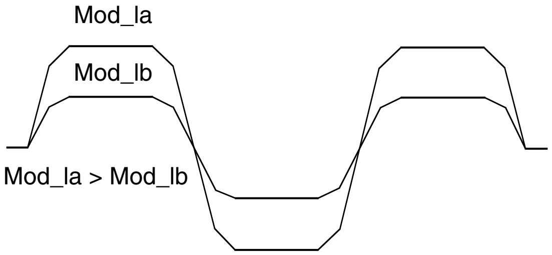


Figure 17. Two Different Modulator Current Settings

Modulator Attenuator

A third way to set the deviation is by programming the modulator attenuator, Mod_A2..Mod_A0, the last being LSB. The purposes of the attenuator is to allow small deviations when the bit rate is small and/or the BT is small (these settings will give a relatively slow modulator clock, and therefore long rise- and fall times, which in turn results in large frequency deviations). In addition, the attenuator will improve the resolution in the modulator.

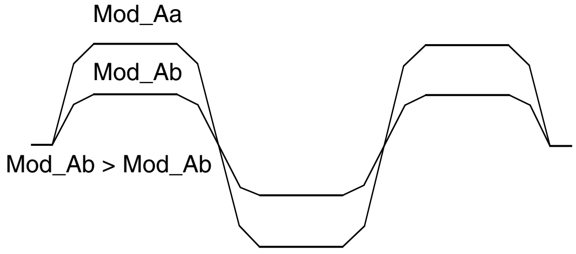


Figure 18. Two different modulator attenuator settings

The attenuation is given by:

$$V_{MOD2} \alpha \frac{1}{1+MOD\_A}$$

where V_{MOD2} and V_{MOD1} is the modulator amplitude after and before the attenuator, respectively. Figure 16 shows two waveforms with different attenuator setting; Mod_Aa < Mod_Ab. If Mod_A is increased, the frequency deviation is lowered and vice versa.

Modulator Filter

To reduce the high-frequency components in the generated waveform, a filter with programmable cut-off frequency can be enabled. This is done using Mod_F2..Mod_F0, the last one being LSB. The Mod_F should be set according to the formula:

$$MOD\_F = \frac{150 \times 10^3}{BitRate}$$

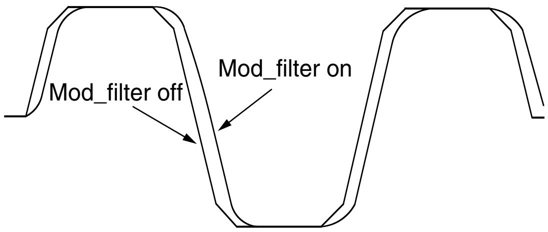


Figure 19. Modulator Waveform with and Without Filtering

Mod_F=0 disables the modulator filter and Mod_F=7 gives most filtering. Figure 18 shows a waveform with and without the filter.

Calculation of the Frequency Deviation

The parameters influencing the frequency deviation can be summarized in the following equations:

$$f_{MOD\_CLK} = \frac{f_{XCO}}{Refclk\_K \times 2^{(7 \times Mod\_clkS)}}$$

$$f_{DEV} = \frac{MOD\_I}{f_{MOD\_CLK}} \cdot \frac{1}{1+MOD\_A} \cdot \left(-44.28 \cdot 10^{9} 72 \cdot f_{RF}\right)$$

where :

f_{DEV}:	Single sided frequency deviation [Hz]
f_{XCO}:	Crystal oscillator frequency [Hz]
f_{RF}:	Center frequency [Hz]
Refclk_K:	6 bit divider, values between 1 and 63
Mod_clkS:	Modulator clock setting, values between 0 and 7
f_{MOD_CLK}:	Modulator clock frequency, derived from the crystal frequency, Refclk_K and Mod_clkS
Mod_I:	Modulator current setting, values between 0 and 31
Mod_A:	Modulator attenuator setting, values between 0 and 15

The modulator filter will not influence on the frequency deviation as long as the programmed cut-off frequency is above the actual bit rate.

The frequency deviation must be programmed so that the modulation index (2 x single sided frequency deviation/ Baudrate [bps]) always is greater than or equal to 2 including the total frequency offset between the receiver and the transmitter:

$$f_{DEV} = \text{Baudrate} + f_{OFFSET}$$

The calculated f_{DEV} should be used to calculate the needed receiver bandwidth, see chapter Switched capacitor filter.

Using the XCO-tune Bits

The RF chip has a built-in mechanism for tuning the frequency of the crystal oscillator and is often used in combination with the Frequency Error Estimator (FEE). The XCO tuning is designed to eliminate or reduce initial frequency tolerance of the crystal and/or the frequency stability over temperature.

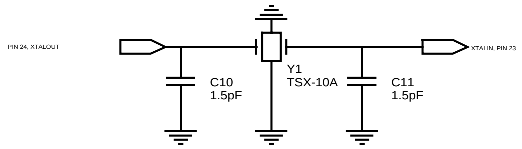


Figure 20: Crystal oscillator’s external components

If the value in XCO_tune is increased (adding capacitance), the frequency will decrease.

The XCO uses two external capacitors. The value of these will strongly affect the tuning range. With a 16.0 MHz crystal (TN4-26011 from Toyocom), and external capacitor values of 1.5 pF, the tuning range will be (almost) equally divided between Òincrease frequencyÓ and Òdecrease frequencyÓ. That is, XCO_tune values greater than approx 16 will decrease frequency, and XCO_tune values less than approx 16 will increase frequency.

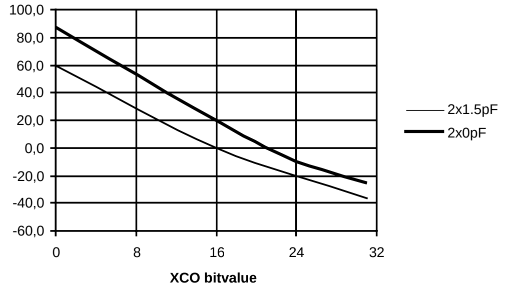


Figure. 21 XCO Tuning

A procedure for using the XCOtuning feature in combination with the FEE is given below. The MICRF505 measures the frequency offset between the demodulated signal and the Lo and tune the XCO so the Lo frequency is equal to received carrier frequency.

A procedure like this can be called during production (storing the calibrated XCO_tune value), at regular intervals or implemented in the communication protocol when the frequency has changed.

The FEE can count “UP”-pulses and/or “DOWN”-pulses (pulses out of the demodulator when a logic “1” or logic “0”, resp., is received). The FEE can count pulses for n bits, where n = 8, 16, 32 or 64.

Example: In FEE, count up+dwn pulses, counting 8 bits:

A perfect case ==> FEE = 0

If FEE > 0: LO is too low, increase LO by decreasing XCO_tune value

v.v. for FEE <0

FEE field holds a a number in the range -128 , ... , 127

However, it keeps counting above/below the range, that is:

If FEE=-128 and still counting dwn-pulses:

1) => -129 = +127

2) 126

3) 125

...

To avoid this situation, always make sure max count is between limits. Suggestion: Count for 8 (or 16) bits only.

Procedure description

In the procedure below, UP+DWN pulses are counted, and only the sign of the FEE is used. The value of n is 8 or 16.

Assumption:

A transmitter is sending a 1010... pattern at the correct frequency and bitrate

The wanted receiver frequency is the mid-point between the “0” and “1” frequencies

Input:

Nothing

Output:

The best XCO_tune value

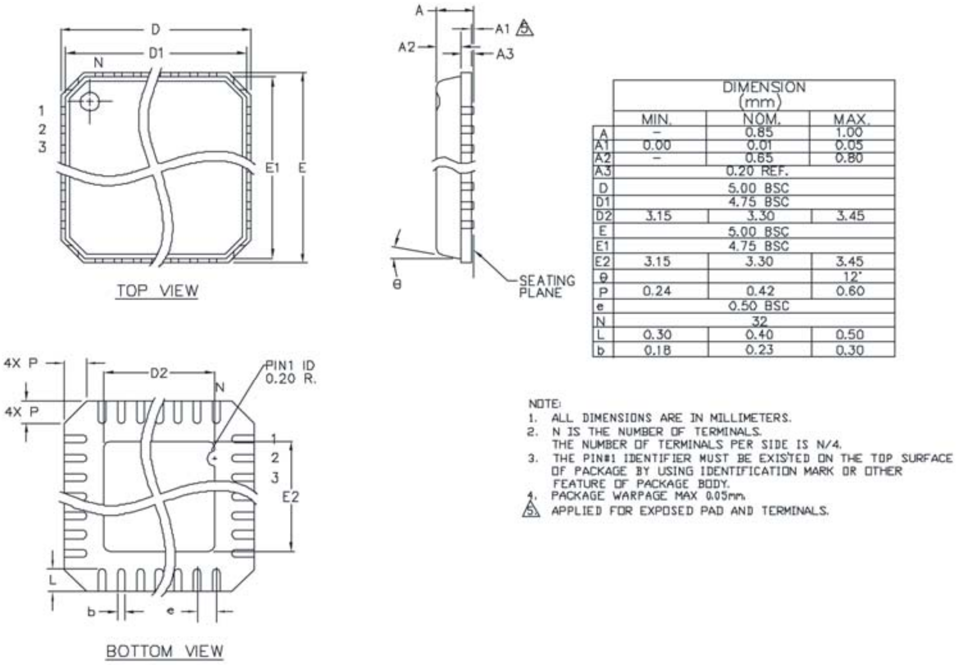
(giving the lowest IFEEI)

Local variables:

XCO_Present (5-bit) holds present value in XCO_tune bits
XCO_Step (4-bit) holds Increment/decrement of XCO_tune bits
XCO_Sign (1 bit) holds POS or NEG (increment/decrement) increasing LO is done by reducing the XCO_tune value

XCO TUNE PROCEDURE

```
INIT:
        XCO_Present =   0
        XCO_Step    =  32
        XCO_Sign    = NEG

        Control_Word =
        Default RX, clocks match transmitter

LOOP:
        XCO_Step = XCO_Step/2

        XCO_Sign == POS?
           Yes —> XCO_Present -= XCO_Step // increase LO
           No  —> XCO_Present += XCO_Step // decrease LO

        XCO_tune bits = XCO_Present

        Program RFChip

        Delay > n bits

        Read FEE

        FEE > 0?
          Yes —> XCO_Sign = POS
          No  —> XCO_Sign = NEG // negative or == 0

       XCO_Step > 1?
           Yes —> Branch to LOOP
           No  —>
             XCO_Sign == POS?
                Yes —> XCO_Present -= 1
            Branch to FIN
       FIN:    RETURN, return-value = XCO_Present
```



	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	–	0.85	1.00
A1	0.00	0.01	0.05
A2	–	0.65	0.80
A3	0.20 REF.		
D	5.00 BSC		
D1	4.75 BSC		
D2	3.15	3.30	3.45
E	5.00 BSC		
E1	4.75 BSC		
E2	3.15	3.30	3.45
θ			12°
P	0.24	0.42	0.60
e	0.50 BSC		
N	32		
L	0.30	0.40	0.50
b	0.18	0.23	0.30

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS.
   THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.
5. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin MLF (B)

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