General Description

The MIC5800/5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bank of Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. MIC5800 contains four latched drivers; MIC5801 contains eight latched drivers.

Data input rates are greatly improved in these devices. With a 5V supply, they typically operate at better than 5MHz. With a 12V supply, significantly higher speeds are obtained. The outputs are compatible with standard TTL, PMOS, NMOS, and CMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500mA and will sustain at least 50V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

Features

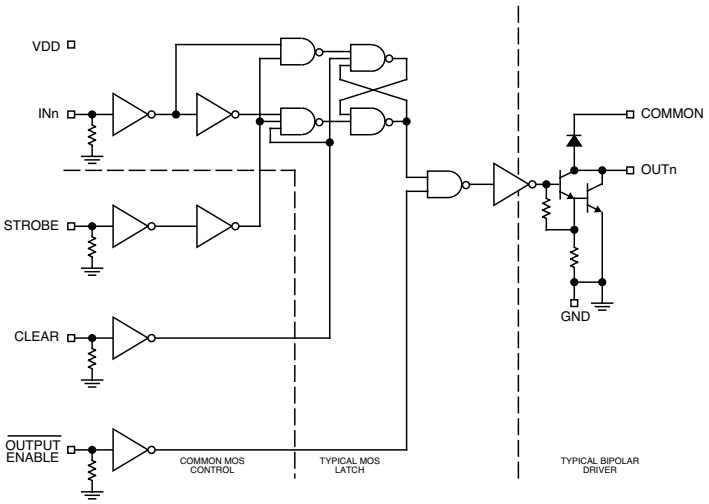
- 4.4MHz Minimum Data Input Rate
- High-Voltage, Current Sink Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

Ordering Information

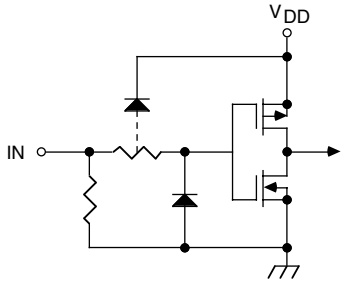
Standard	Pb-Free	Temperature Range	Package
MIC5800N	MIC5800YN	– 40°C to + 85°C	14–Pin Plastic DIP
MIC5800M	MIC5800YM	– 40°C to + 85°C	14–Pin SOIC
MIC5801BN	MIC5801YN	– 40°C to +85°C	22–Pin Plastic DIP
5962-87640		– 55°C to +125°C	22–Pin CERDIP
MIC5801BV	MIC5801YV	– 40°C to + 85°C	28–Pin PLCC
MIC5801BWM	MIC5801YWM	– 40°C to +85°C	24–Pin SOIC

Standard Military Drawing for MIC5801AJBQ

Functional Diagram



Typical Input



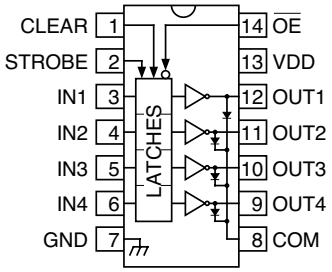
Absolute Maximum Ratings: (Notes 1–6)

at +25°C Free-Air Temperature

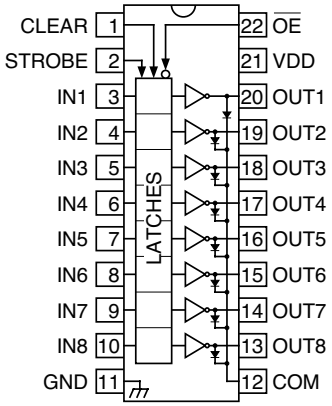
Output Voltage, V_{CE}	50V
Supply Voltage, V_{DD}	15V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Continuous Collector Current, I_C	500mA
Package Power Dissipation:	
MIC5800 Plastic DIP (Note 1)	2.1W
MIC5801 Plastic DIP (Note 2)	2.5W
MIC5800 SOIC (Note 3)	1.0W
MIC5801 PLCC (Note 4)	2.25W
MIC5801 CERDIP (Note 5)	3.1W
MIC5801 Wide SOIC (Note 6)	1.4 Watt
Operating Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_S	–65°C to +125°C

Note 1: Derate at 16.7 mW/°C above T_A = +25°C
Note 2: Derate at 20 mW/°C above T_A = +25°C
Note 3: Derate at 8.5 mW/°C above T_A = +25°C
Note 4: Derate at 18.2 mW/°C above T_A = +25°C
Note 5: Derate at 25 mW/°C above T_A = +25°C
Note 6: Derate at 11 mW/°C above T_A = +25°C
Note 7: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

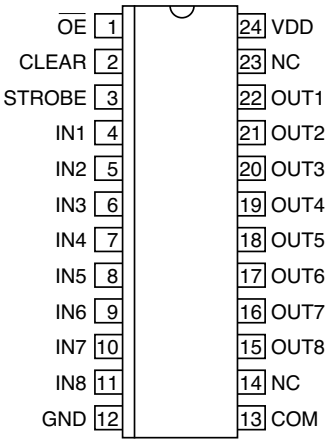
Pin Configuration



MIC5800BN, BM

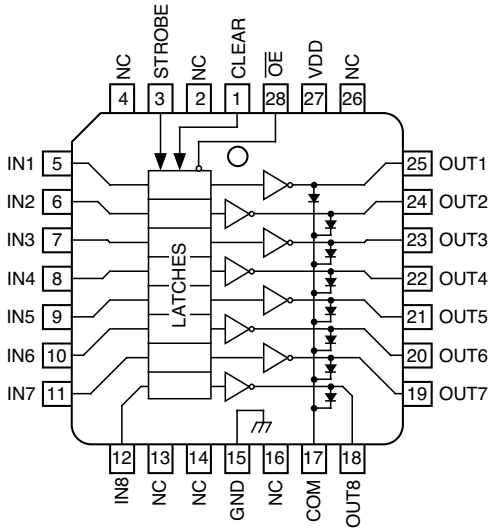


MIC5801BN, AJBQ



MIC5801BWM

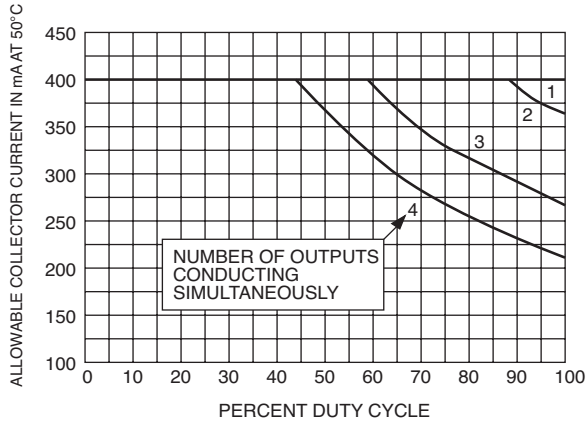
Pin Configurations (continued)



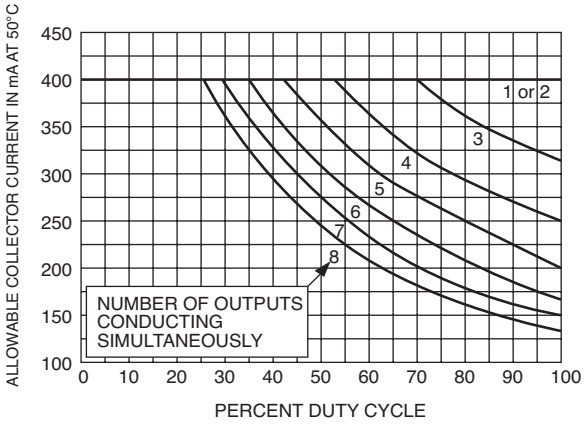
MIC5801BV

Allowable Output Current As A Function of Duty Cycle

MIC5800BN, BM



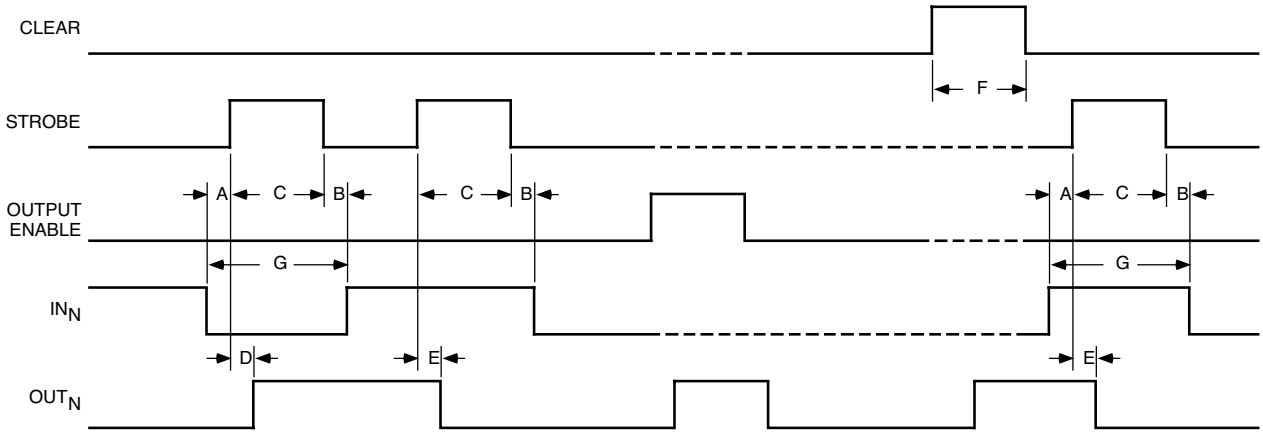
MIC5801BN, AJBQ



Electrical Characteristics (Note 1): at T_A = +25°C, V_{DD} = 5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C			50	µA
		V_{CE} = 50 V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA		0.9	1.1	V
		I_C = 200 mA		1.1	1.3	
		I_C = 350 mA, V_{DD} = 7.0 V		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5			
		V_{DD} = 10 V	8.5			
		V_{DD} = 5.0 V (See Note)	3.5			
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200		kΩ
		V_{DD} = 10 V	50	300		
		V_{DD} = 5.0 V	50	600		
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open		1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open		0.9	1.7	
		V_{DD} = 5.0 V, Outputs Open		0.7	1.0	
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V			200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V		50	100	
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C			50	µA
		V_R = 50 V, T_A = +70°C			100	
Clamp Diode Forward Voltage	V_F	I_F = 350 mA		1.7	2.0	V

NOTE : Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
NOTE 1: Specification for packaged product only.



Timing Conditions

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) 50ns
B. Minimum data active time after strobe disabled (data hold time) 50ns
C. Minimum strobe pulse width 125ns
D. Typical time between strobe activation and output on to off transition 500ns
E. Typical time between strobe activation and output off to on transition 500ns
F. Minimum clear pulse width 300ns
G. Minimum data pulse width 225ns

Truth Table

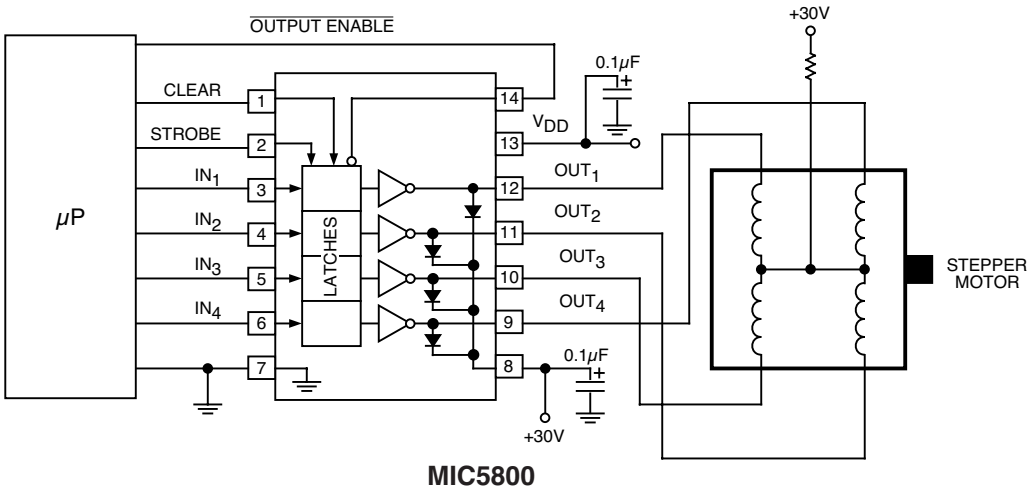
IN_N	Strobe	Clear	Output Enable	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t-1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

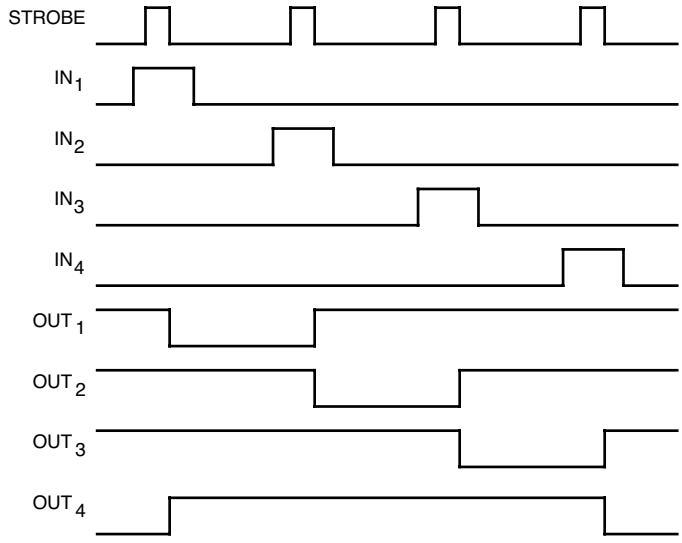
Typical Application

Unipolar Stepper-Motor Drive

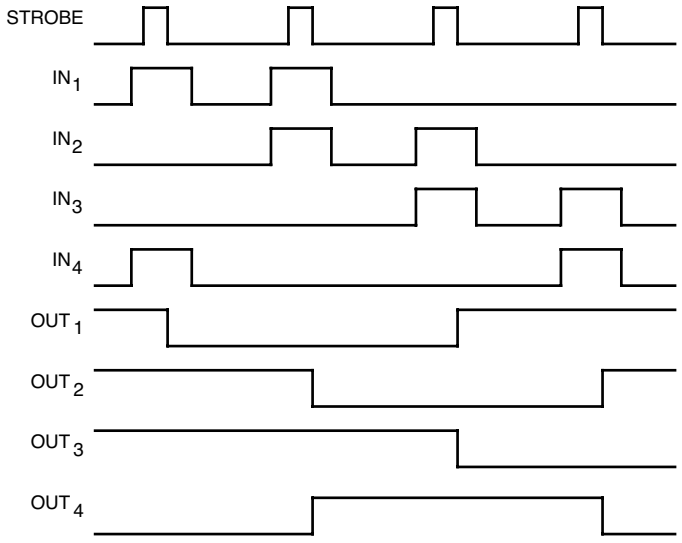


MIC5800

UNIPOLAR WAVE DRIVE



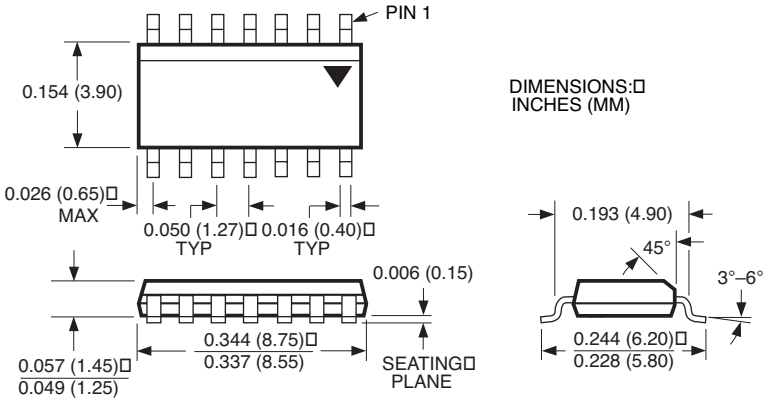
UNIPOLAR 2-PHASE DRIVE



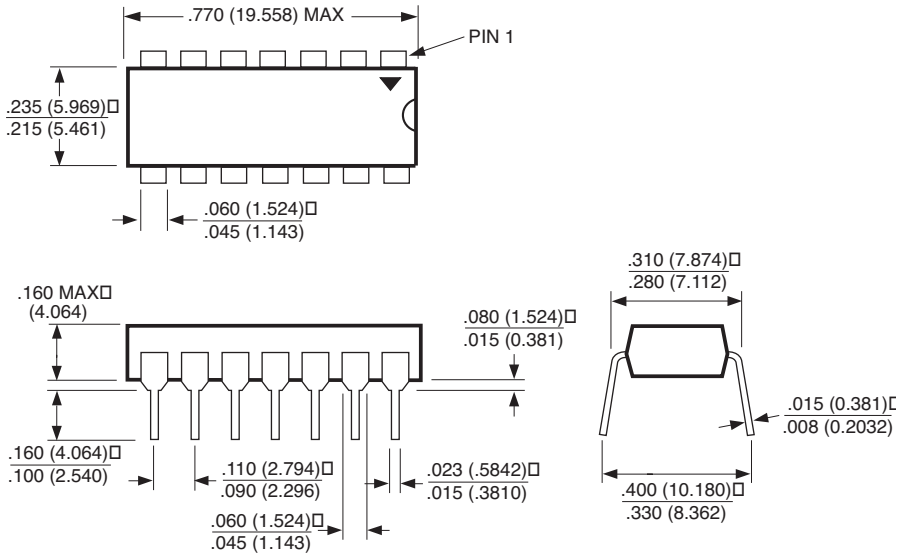
Note:

Lamp inrush current
is approximately 10
lamp operating current.

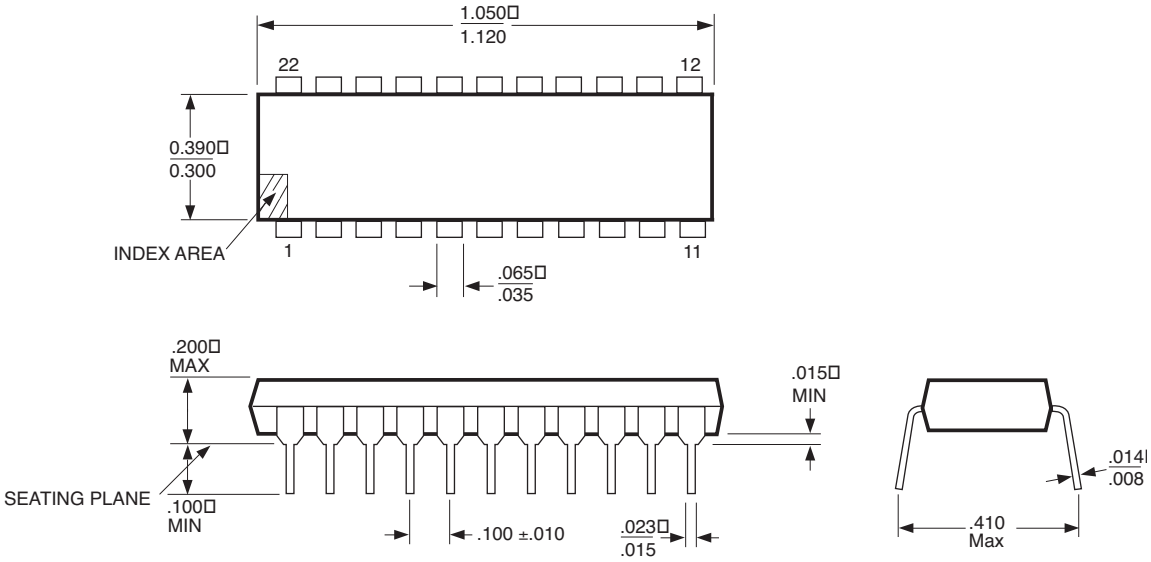
Package Information



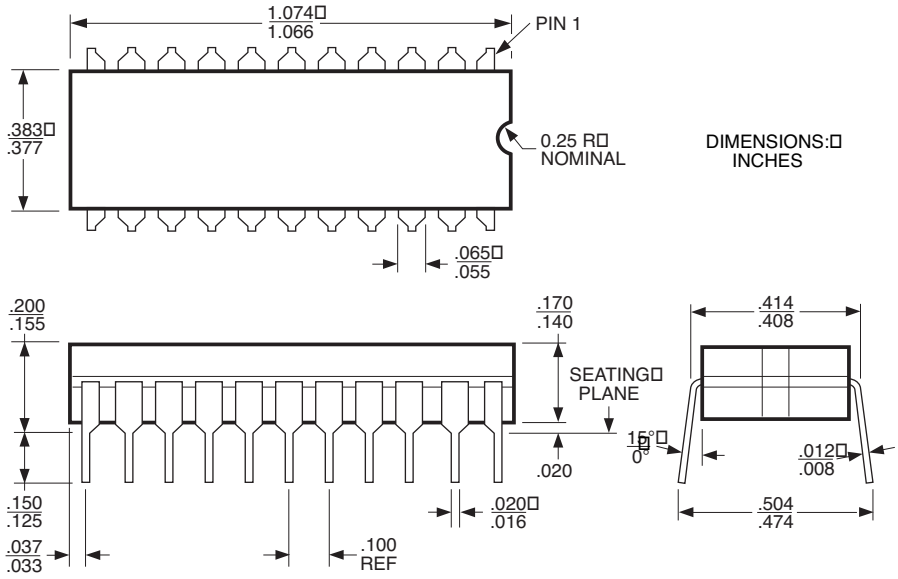
14-Pin SOIC (M)



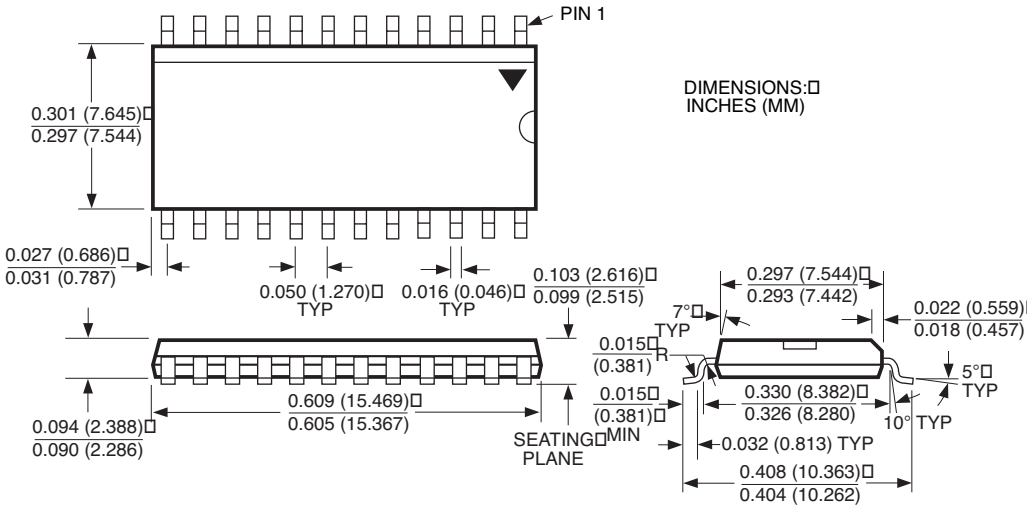
14-Pin Plastic DIP (N)



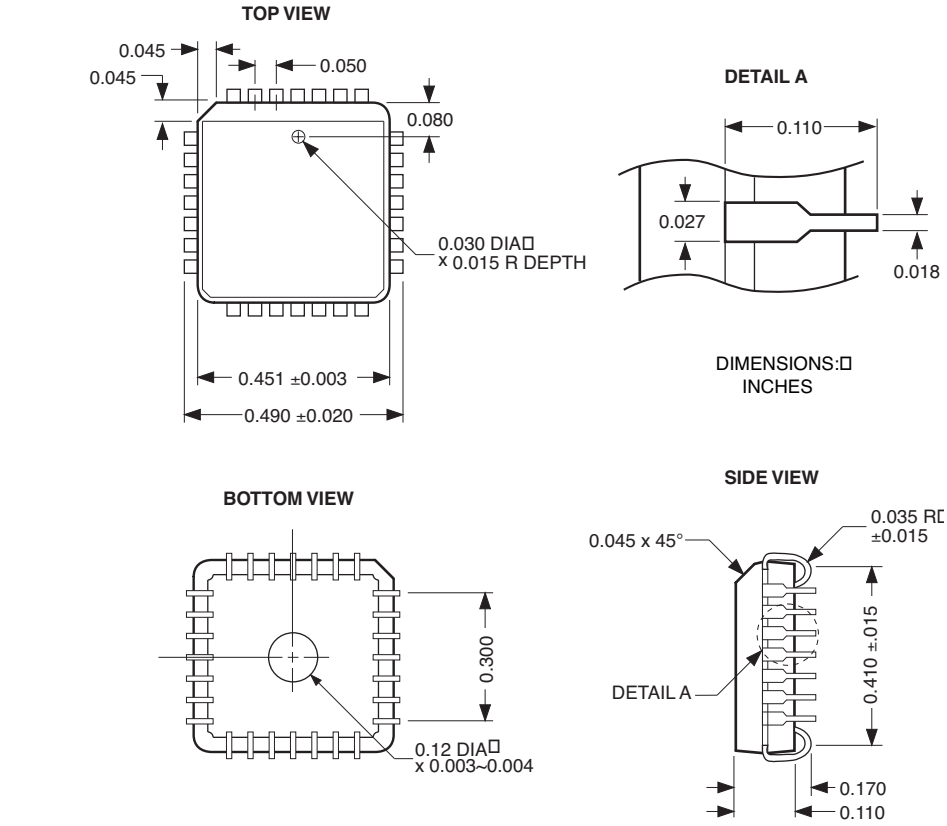
22-Pin Plastic DIP (N)



22-Pin Ceramic DIP (J)



24-Pin SOIC (M)



28-Pin PLCC (V)

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