Preliminary Specification

PRODUCT NAME: RGS15128128FH029
PRODUCT NO.: 9919001000
PART NUMBER: PFO19001

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2007. 08. 10	

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 262K and 65K full colors
- Panel matrix : 128*3*128
- Driver IC : SSD1355
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.625 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8/16-bit 6800-series Parallel Interface, 8/16-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x (RxGxB) x 128 (H)	dot
2	Dot Size	0.0435 (W) x 0.1855 (H)	mm^2
3	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm^2
4	Aperture Rate	57	%
5	Active Area	26.279 (W) x 26.284 (H)	mm^2
6	Panel Size	33.5 (W) x 33.5 (H)	mm^2
7	Panel Thickness	1.625 ± 0.1	mm
8	Module Size	33.5 (W) x 46.33 (H) x 1.625 (D)	mm^3
9	Diagonal A/A size	1.46	inch
10	Module Weight	TBD	gram

5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	10	20	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	9,000	-	Hrs	110 cd/m^2, 50% checkerboard	Note (1)
Life Time	10,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (2)
Life Time	13,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = TBD, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 110cd/m^2 :

- Master contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/128

(2) Setting of 100cd/m^2 :

- Master contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/128

(3) Setting of 80cd/m^2 :

- Master contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/128

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)		TBD	TBD	TBD	V
V_{CI}	Low voltage power supply (for driver IC)		2.4	2.8	3.5	V
V_{DDIO}	Logic I/O operating voltage		1.6	1.8	V_{CI}	V
V_{OH}	High logic output level	Iout=100uA	0.9*V_{DDIO}		V_{DDIO}	V
V_{OL}	Low logic output level	Iout=100uA	0		0.1*V_{DDIO}	V
V_{IH}	High logic input level		0.8*V_{DDIO}		V_{DDIO}	V
V_{IL}	Low logic output level		0		0.2*V_{DDIO}	V
I_{CC}	Operating current for V_{CC} (No panel attached)	Contrast=FF		1.65	1.9	mA
I_{DDIO}	Operating current for V_{DDIO} (No panel attached)	Contrast=FF		0.5	10	uA
I_{CI}	Operating current for V_{CI} (No panel attached)	Contrast=FF		670	750	uA
I_{SEG}	Segment output current (No panel attached)	Contrast=FF		230	250	uA
		Contrast=7F		120		uA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		TBD	TBD	mA	All pixels on (1)
Standby mode current		TBD	TBD	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		TBD	TBD	mW	All pixels on (1)
Standby mode power consumption		TBD	TBD	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m^2	Display Average
Standby mode Luminance		TBD		cd/m^2	
CIEx(White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy(White)	0.28	0.32	0.36		
CIEx (Red)	TBD	TBD	TBD		
CIEy (Red)	TBD	TBD	TBD		
CIEx (Green)	TBD	TBD	TBD		
CIEy (Green)	TBD	TBD	TBD		
CIEx (Blue)	TBD	TBD	TBD		
CIEy (Blue)	TBD	TBD	TBD		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

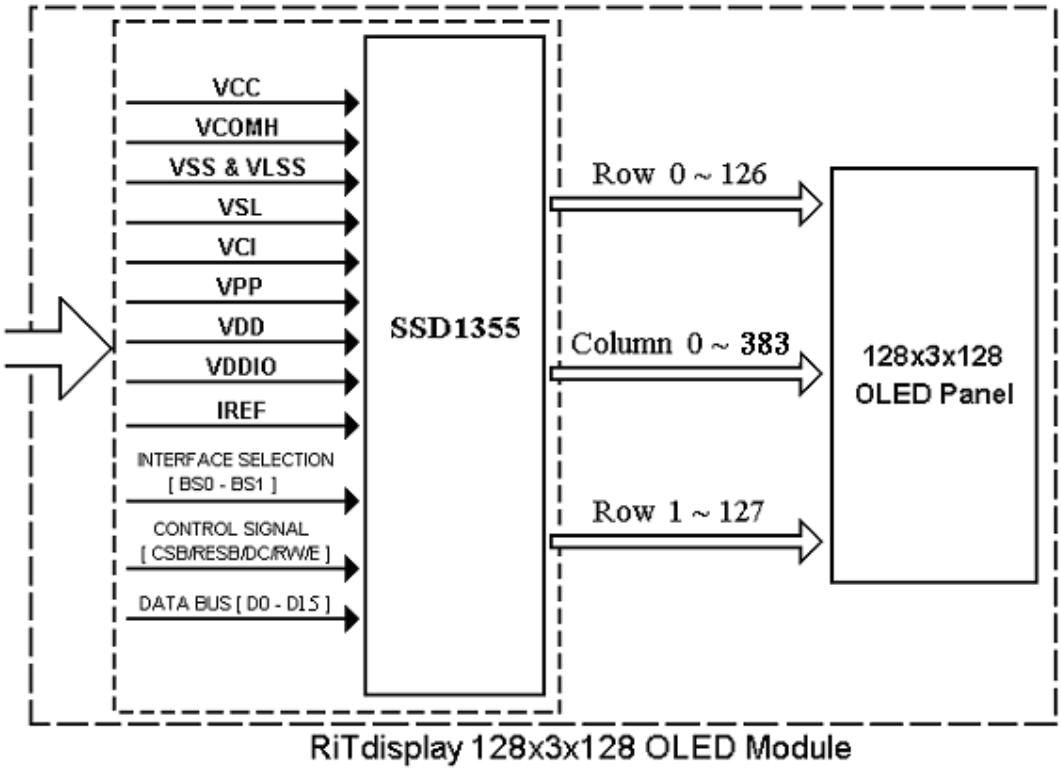
- Driving Voltage : TBD
- Master contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/128

(2) Standby mode condition :

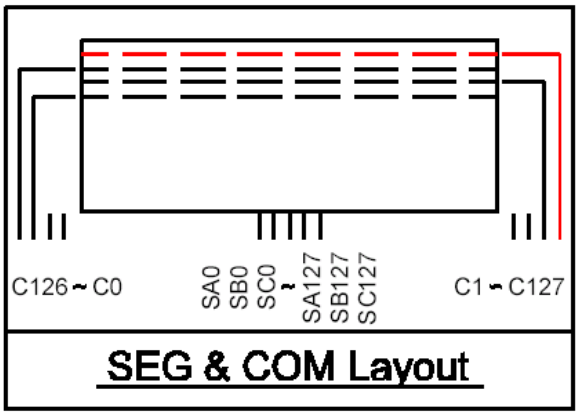
- Driving Voltage : TBD
- Master contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	NC	No connection.
2	VLSS	Analog system ground pin.
3	VCC	Power supply for panel driving voltage.
4	VSL	This is segment voltage reference pin.
5	VCI	Low voltage power supply.
6	VDDIO	Power supply for interface logic level.It should be match with the MCU interface voltage level and must be connected to external source
7	BS0	Interface selection
8	BS1	
9	CS#	This pad is the chip select input. Low active.
10	RES#	This is a reset signal input. Low active.
11	D/C#	D/C="H": Data. D/C="L": Command.
12	R/W#	When connected to an 8080 MPU. When WR ="L": Write signal input. When connected to a 6800 Series MPU. When WR ="H": Read. When WR ="L": Write.
13	E/RD#	When connected to an 8080 MPU. When RD ="L": Read signal input. When connected to a 6800 Series MPU. Enable clock input of the 6800 series MPU.
14	VPP	Connect to VDD.
15	VDD	Power supply input for logic.
16	D0	16bit / 8 bit Data bus I/O.
17	D1	
18	D2	
19	D3	
20	D4	
21	D5	
22	D6	
23	D7	
24	D8	
25	D9	
26	D10	
27	D11	
28	D12	
29	D13	
30	D14	
31	D15	
32	VSS	Ground pin.
33	IREF	A resistor should be connected between this pin and VSS.

34	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pad and VSS.
35	VCC	Power supply for panel driving voltage.
36	VLSS	Analog system ground pin.
37	NC	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x160x18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

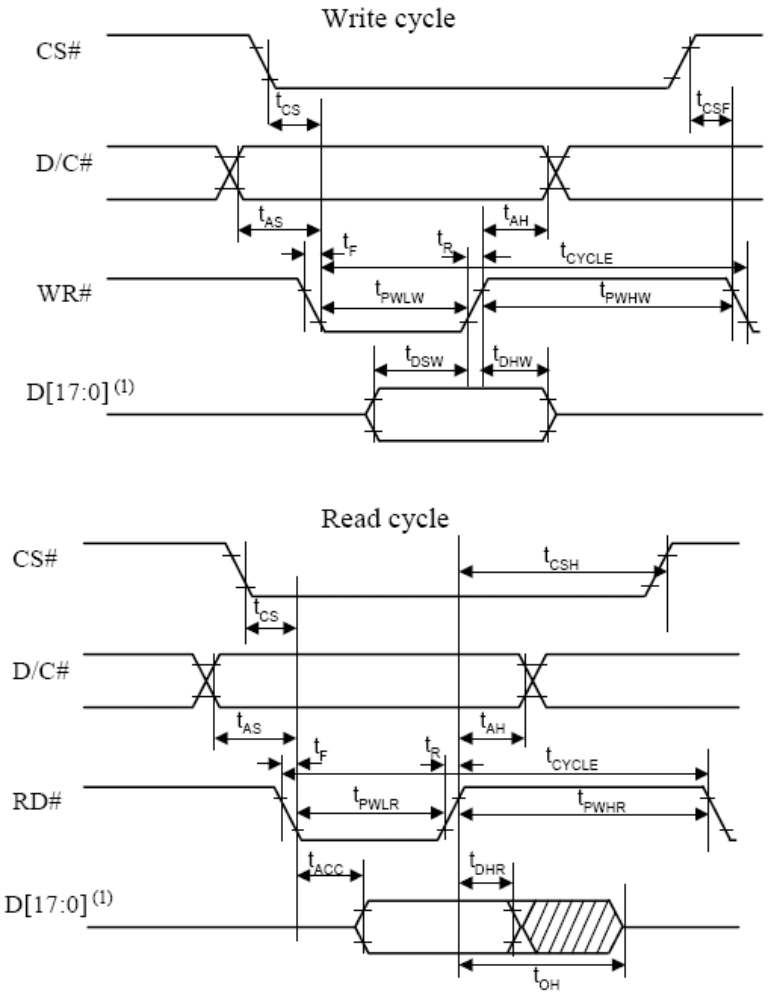
Segment Address	Normal	0			1			2	.....	.....	126	127			
	Remapped	127			126			125	.....	.....	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	
Normal	Remapped														Common output
0	159	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	158	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM1
2	157	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM2
3	156	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM3
4	155	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM4
5	154	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM5
6	153	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6	COM6
7	152								.....	.....	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
155	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6	:
156	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM156
157	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM157
158	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM158
159	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM159

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

7.5 INTERFACE TIMING CHART

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



8080-series MPU parallel interface characteristics

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

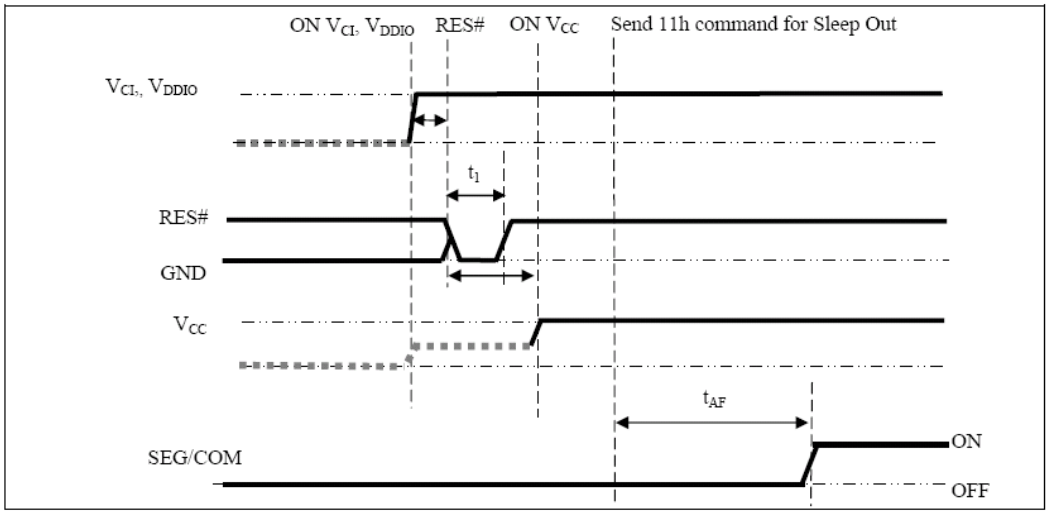
***Power ON sequence**:*

1.Power ON VCI, VDDIO.

2. After VCI, VDDIO become stable, set wait time at least 1ms (t_0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) and then HIGH (logic high).

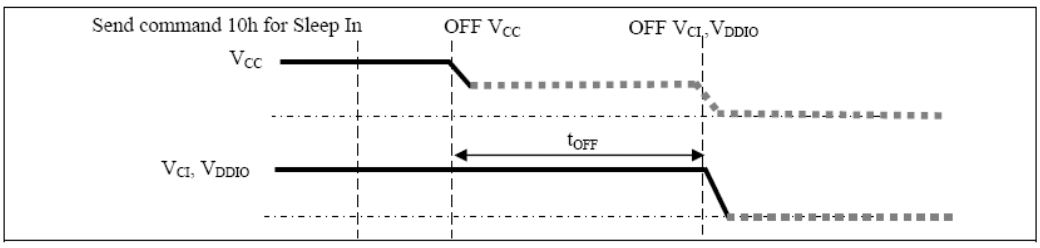
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON VCC.(1)

4. After VCC become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms (t_{AF}).



Power OFF sequence:

1. Send command 10h for sleep In.
2. Power OFF VCC. (1), (2)
3. Wait for t_{OFF}. Power OFF VCI,VDDIO. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI,VDDIO and VCC,VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2) VCC should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT

TBD

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1355

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

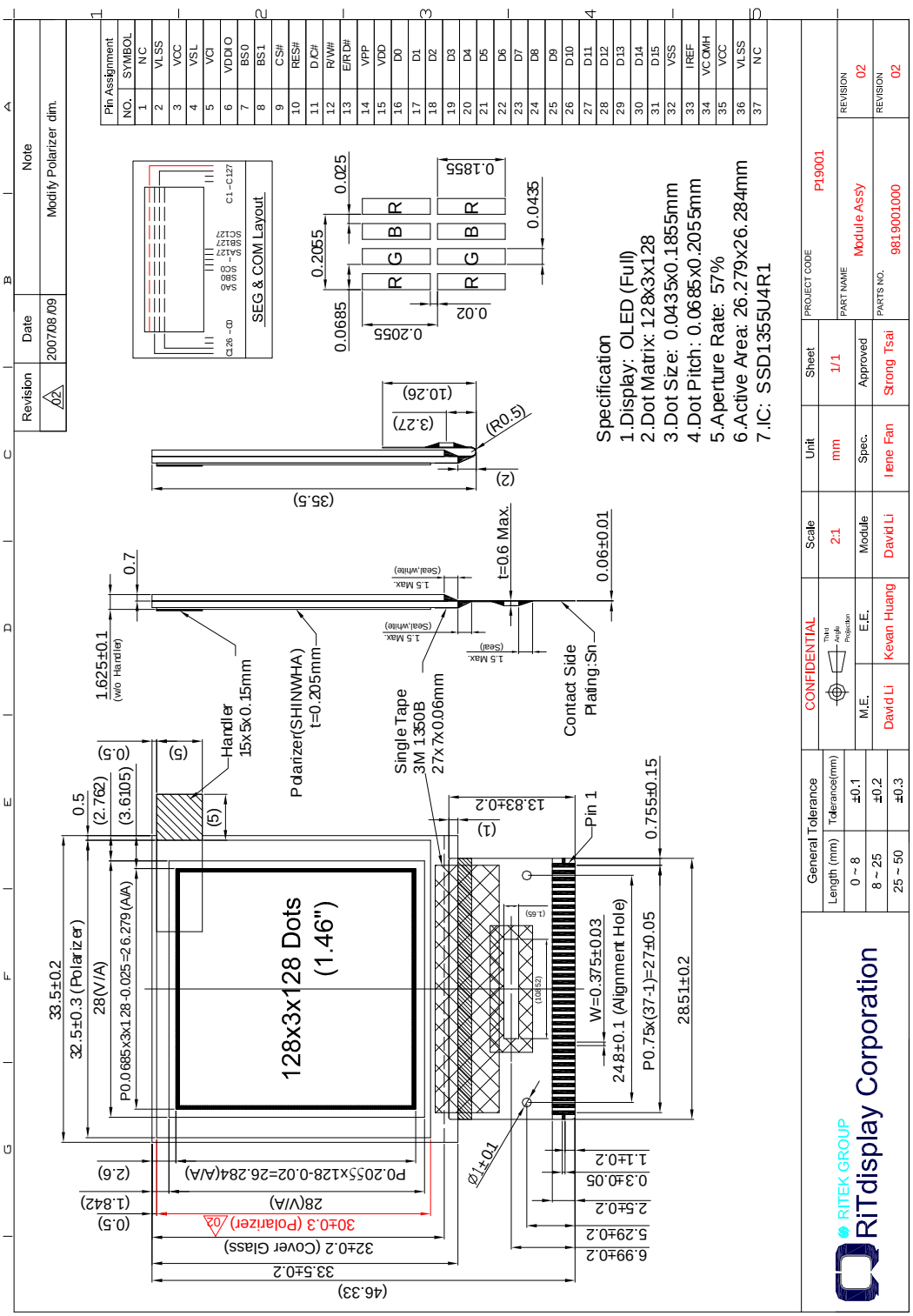
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

TBD

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

1. The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

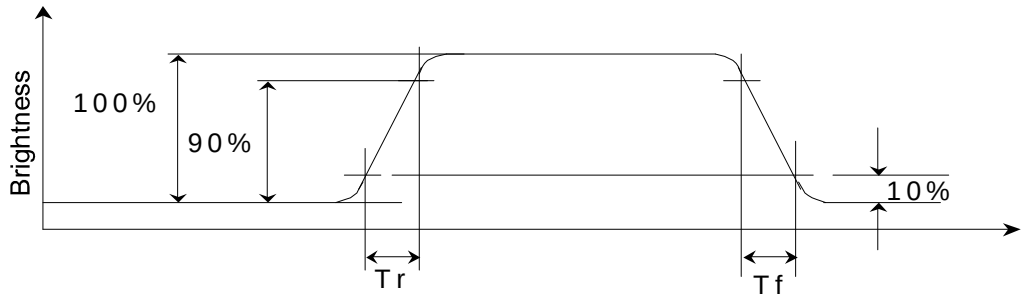
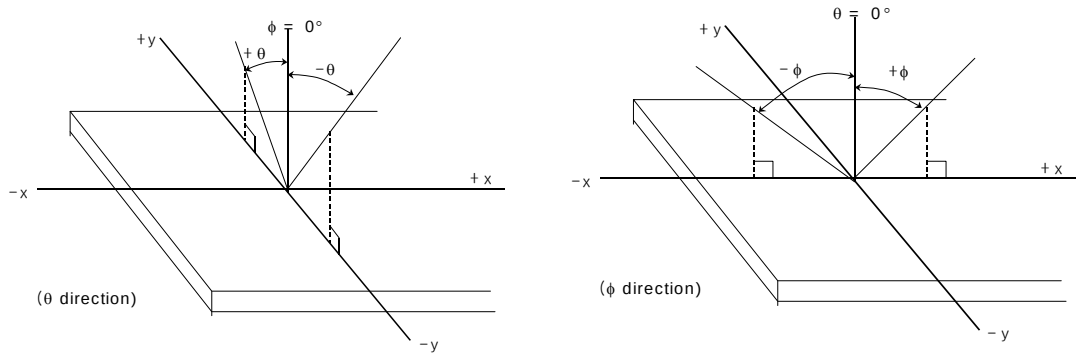


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



Vertical angles

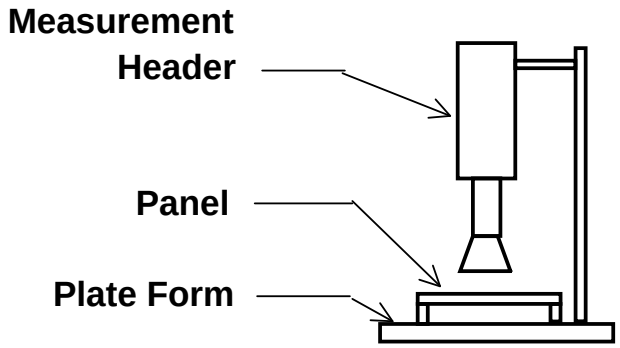
Horizontal angles

Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

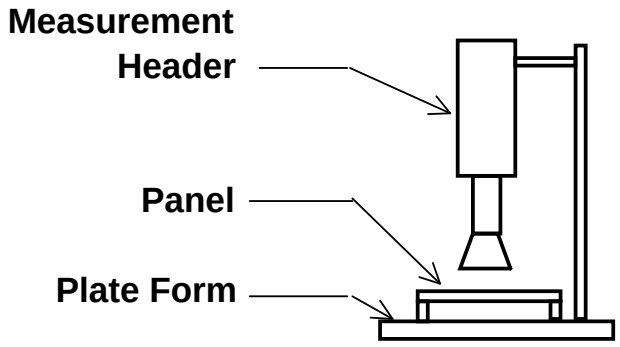
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

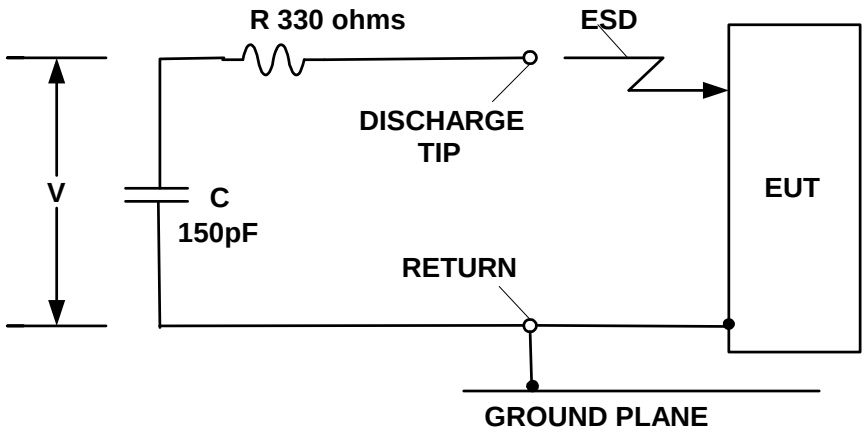
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.