TIBPAL16L8-25C, TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16L8-30M, TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT THE PAL® CIRCUITS

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High-Performance Operation: Propagation Delay

C Suffix . . . 25 ns Max M Suffix . . . 30 ns Max

- Functionally Equivalent, but Faster Than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A
- Power-Up Clear on Registered Devices (All Register Outputs Are Set High, but Voltage Levels at the Output Pins Go Low)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

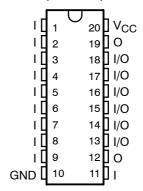
DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

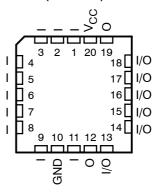
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

TIBPAL16L8'
C SUFFIX ... J OR N PACKAGE
M SUFFIX ... J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)





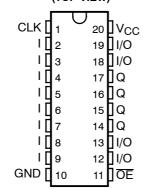
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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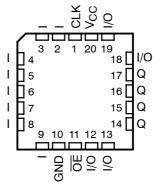


TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT TM PAL® CIRCUITS SRPS059A FEBRUARY 1984 - REVISED DECEMBER 2010

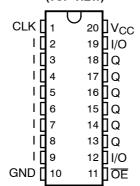
TIBPAL16R4'
C SUFFIX ... J OR N PACKAGE
M SUFFIX ... J OR W PACKAGE
(TOP VIEW)



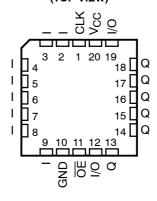
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



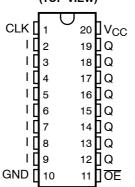
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



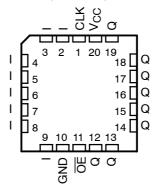
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



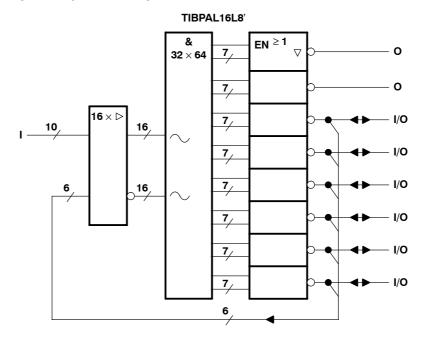
TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)

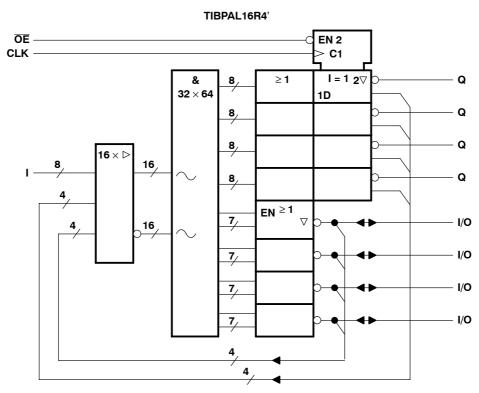


TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



functional block diagrams (positive logic)



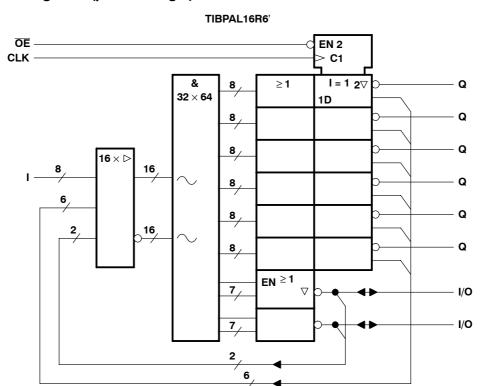


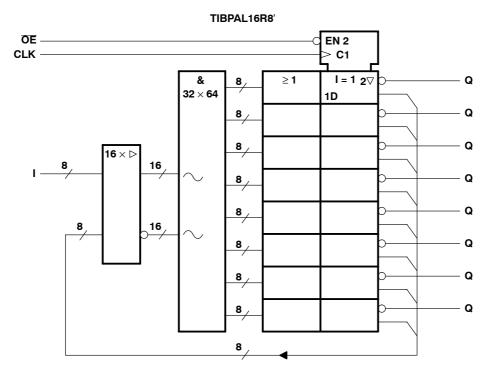
denotes fused inputs



SRPS059A FEBRUARY 1984 - REVISED DECEMBER 2010

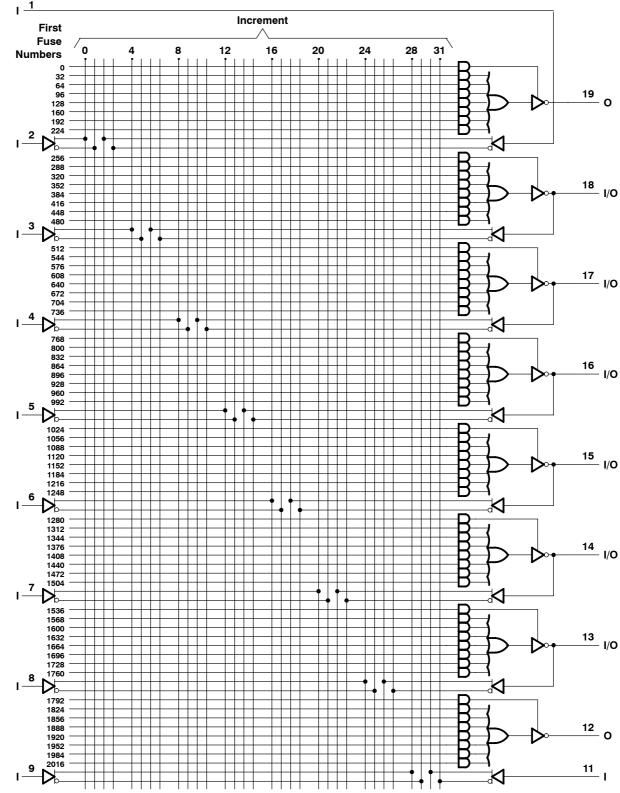
functional block diagrams (positive logic)





outline denotes fused inputs



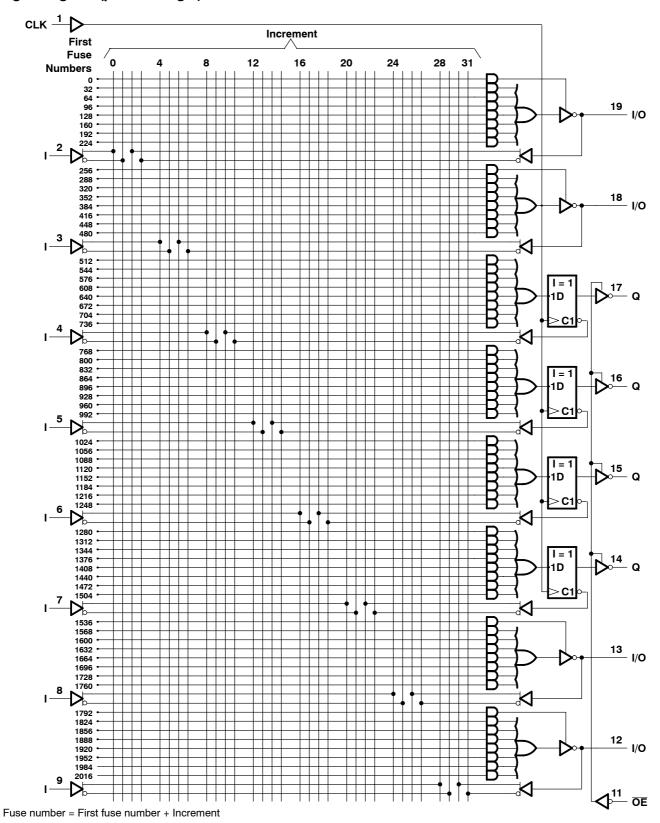




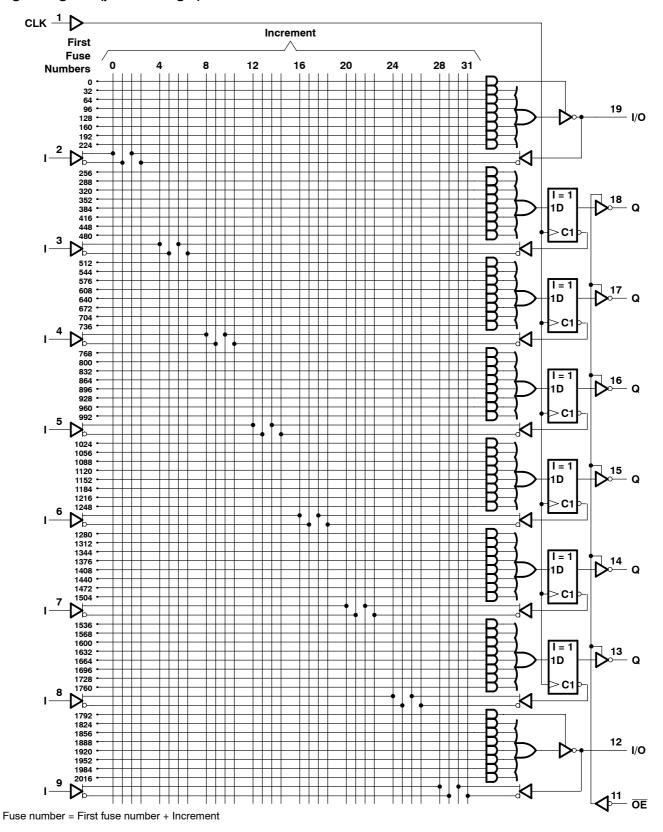


TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT ™ PAL® CIRCUITS

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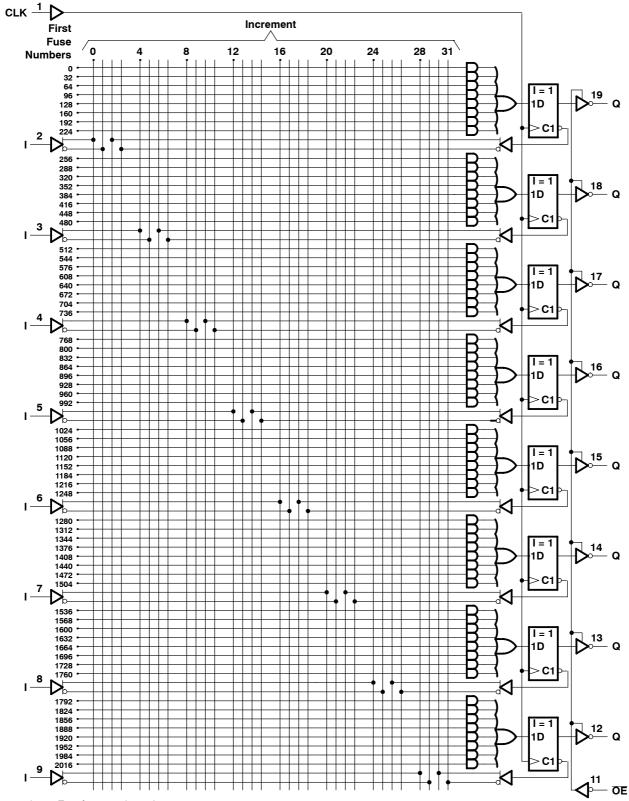


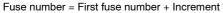




TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE *IMPACT* ™ *PAL*® CIRCUITS

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TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT TM PAL® CIRCUITS SRPS059A FEBRUARY 1984 - REVISED DECEMBER 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range, T _{sta}	. −65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

	pply voltage		4.75			
V _{IH} Higl			4.75	5	5.25	٧
	h-level input voltage		2		5.5	V
V _{IL} Low	v-level input voltage				8.0	V
I _{OH} Higl	h-level output current				-3.2	mA
I _{OL} Low	v-level output current				24	mA
f _{clock} Clo	ck frequency		0		30	MHz
4 Dul	and distribution along (and Nata O)	High	10			
t _w Puls	se duration, clock (see Note 2)	Low	15			ns
t _{su} Set	up time, input or feedback before clock↑		20			ns
t _h Hole	d time, input or feedback after clock↑		0			ns
T _A Ope	erating free-air temperature		0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, fclock. The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT ™ PAL® CIRCUITS

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electrical characteristics over recommended operating free-air temperature range

F	PARAMETER		TEST CONDITION	IS	MIN	TYP [†]	MAX	UNIT
V _{IK}		$V_{CC} = 4.75 V$,	I _I = -18 mA				-1.5	V
V _{OH}		$V_{CC} = 4.75 V$,	$I_{OH} = -3.2 \text{ mA}$		2.4	3.3		V
V _{OL}		$V_{CC} = 4.75 V$,	$I_{OL} = 24 \text{ mA}$			0.35	0.5	V
	Outputs	., 5.05.)/	V 07V				20	•
l _{ozh}	I/O ports	$V_{CC} = 5.25 \text{ V},$	$V_0 = 2.7 \text{ V}$				100	μΑ
	Outputs	., 5.05.),	V 0.4V				-20	•
l _{OZL}	I/O ports	$V_{CC} = 5.25 \text{ V},$	$V_O = 0.4 V$				-250	μΑ
II		$V_{CC} = 5.25 \text{ V},$	V _I = 5.5 V				0.1	mA
I _{IH}		V _{CC} = 5.25 V,	V _I = 2.7 V				20	μΑ
I _{IL}		$V_{CC} = 5.25 \text{ V},$	$V_{I} = 0.4 V$				-0.25	mA
l _O [‡]		V _{CC} = 5.25 V,	V _O = 2.25 V		-30		-125	mA
I _{CC}		V _{CC} = 5.25 V,	$V_I = 0$,	Outputs open		75	100	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 $^{\circ}$ C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
f _{max}				30			MHz
t _{pd}	I, I/O	O, I/O			15	25	ns
t _{pd}	CLK↑	Q	R1 = 500Ω ,		10	15	ns
t _{en}	OE↓	Q	R2 = 500Ω ,		15	20	ns
t _{dis}	OE↑	Q	See Figure 3		10	20	ns
t _{en}	I, I/O	O, I/O			14	25	ns
t _{dis}	I, I/O	O, I/O			13	25	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.



[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS}.

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE IMPACT TM PAL® CIRCUITS SRPS059A FEBRUARY 1984 - REVISED DECEMBER 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range, T _{sto}	-65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage		2		5.5	V
V _{IL}	Low-level input voltage				8.0	V
I _{OH}	High-level output current				-2	mA
I _{OL}	Low-level output current				12	mA
f _{clock}	Clock frequency		0		25	MHz
	Dulas duration alask (ass Nata 0)	High	15			
t _w	Pulse duration, clock (see Note 2)	Low	20			ns
t _{su}	Setup time, input or feedback before clock↑		25			ns
t _h	Hold time, input or feedback after clock↑		0			ns
T _A	Operating free-air temperature		-55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, fclock. The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE *IMPACT* ™ *PAL*® CIRCUITS

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electrical characteristics over recommended operating free-air temperature range

P	ARAMETER		TEST CONDITION	IS	MIN	TYP†	MAX	UNIT
V _{IK}		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA				-1.5	V
V _{OH}		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$		2.4	3.2		V
V _{OL}		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA			0.25	0.4	V
	Outputs	V 55V	V 07V				20	
l _{OZH}	I/O ports	V _{CC} = 5.5 V	$V_0 = 2.7 \text{ V}$				100	μΑ
	Outputs	V 55V	V 0.4V				-20	
I _{OZL}	I/O ports	$V_{CC} = 5.5 \text{ V},$	$V_O = 0.4 V$				-250	μΑ
	Pin 1, 11	V 55V	V 55V				0.2	A
I _I	All others	V _{CC} = 5.5 V,	$V_{l} = 5.5 V$				0.1	mA
	Pin 1, 11						50	
I _{IH}	I/O ports	V _{CC} = 5.5 V,	$V_{I} = 2.7 V$				100	μΑ
	All others						20	
	I/O ports	V 55V	V 04V				-0.25	4
I _{IL}	All others	$V_{CC} = 5.5 \text{ V},$	$V_I = 0.4 V$				-0.2	mA
los‡		V _{CC} = 5.5 V,	V _O = 0.5 V		-30		-250	mA
I _{CC}		V _{CC} = 5.5 V,	$V_I = 0$,	Outputs open		75	105	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}				25			MHz
t _{pd}	I, I/O	O, I/O			15	30	ns
t _{pd}	CLK↑	Q	R1 = 390 Ω,		10	20	ns
t _{en}	OE↓	Q	R2 = 750 Ω ,		15	25	ns
t _{dis}	OE↑	Q	See Figure 4		10	25	ns
t _{en}	I, I/O	O, I/O			14	30	ns
t _{dis}	I, I/O	O, I/O			13	30	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25°C.



[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.

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programming information

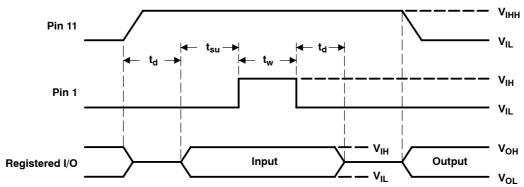
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644–5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.



NOTE 3: $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns V}_{IHH} = 10.25 \text{ V to } 10.75 \text{ V}$

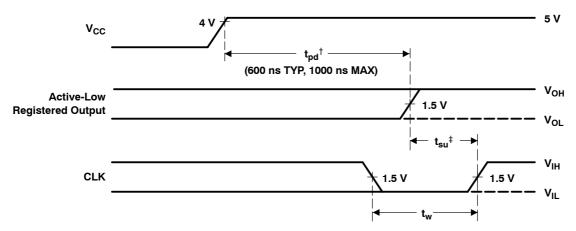
Figure 1. Preload Waveforms

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M .OW-POWER HIGH-PERFORMANCÉ *IMPACT* ™ *PAL*® CIRCUITS

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power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



[†] This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

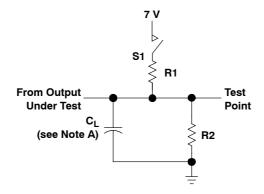
Figure 2. Power-Up Reset Waveforms



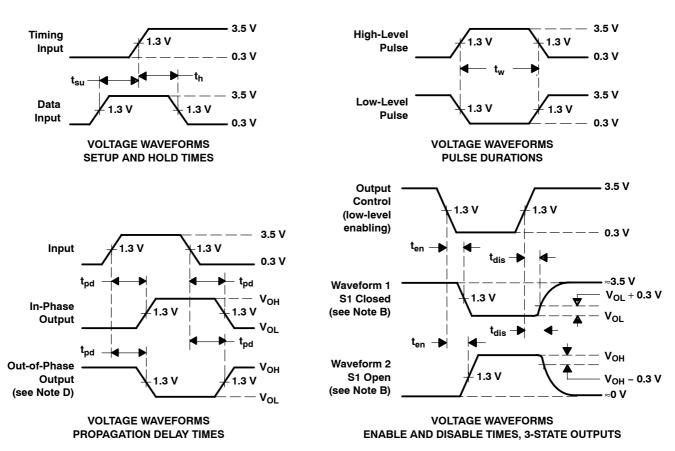
[‡] This is the setup time for input or feedback.

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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



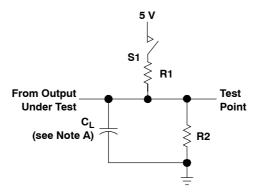
- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_{r} = $t_{f} \leq 2$ ns, duty cycle = 50%
 - D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
 - E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

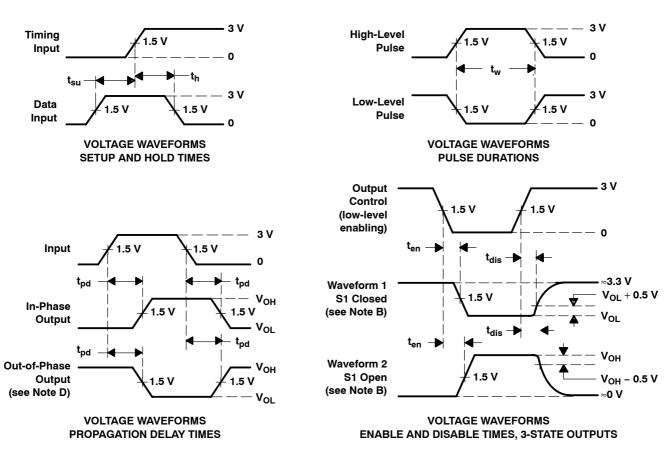


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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: PRR \leq 10 MHz, $t_r = t_f \leq$ 2 ns, duty cycle = 50%
 - D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 - E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms



25-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-85155052A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8515505RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8515505SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-85155062A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8515506RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8515506SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-85155072A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8515507RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8515507SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-85155082A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8515508RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-8515508SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
JM38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16L8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	
TIBPAL16L8-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
TIBPAL16L8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TIBPAL16L8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TIBPAL16L8-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16L8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16L8-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
TIBPAL16R4-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	





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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TIBPAL16R4-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	
TIBPAL16R4-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TIBPAL16R4-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TIBPAL16R4-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16R4-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16R4-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
TIBPAL16R6-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	
TIBPAL16R6-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TIBPAL16R6-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TIBPAL16R6-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16R6-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16R6-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
TIBPAL16R8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	
TIBPAL16R8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TIBPAL16R8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TIBPAL16R8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
TIBPAL16R8-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

25-Jan-2012

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



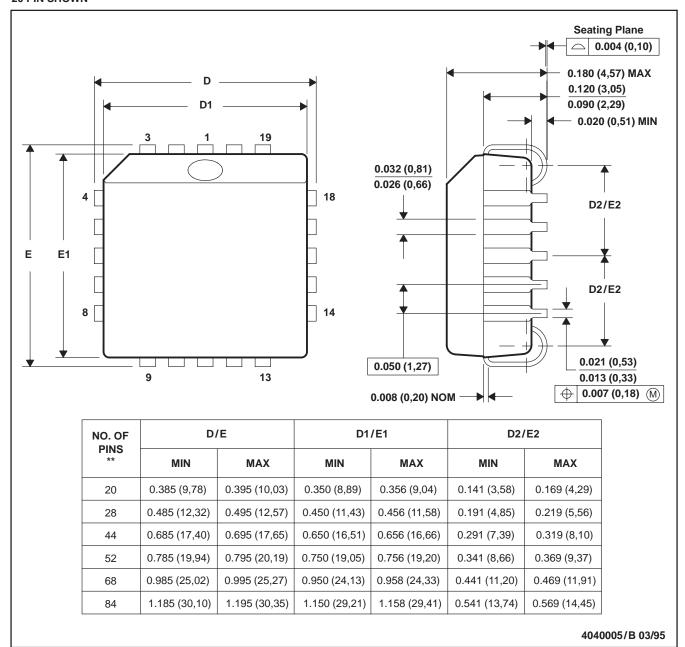
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-018

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