

STRUCTURE Silicon Monolithic Integrated Circuit
TYPE 1ch Series Regulator Driver IC
PRODUCT SERIES **BD3509MUV**
FEATURES

- High Accuracy Voltage Regulator(0.65±1%)
- Non Rush Current on Start up (NRCS)
- Built in Super low ON resistance (28mΩ typ) Nch Power MOSFET
- Built in Power Good Function
- Maximum Output Current, 4A

○ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply Voltage 1	V _{CC}	+6.0 ^{*1}	V
Supply Voltage 2	V _{IN}	+6.0 ^{*1}	V
Supply Voltage 3	V _{DD}	+6.0 ^{*1}	V
Enable Input Voltage	V _{EN}	-0.3~+6.0	V
PGOOD Input Voltage	V _{PGOOD}	+6.0	V
Output Current	I _O	4.0 ^{*1}	A
Power dissipation 1	Pd1	0.34 ^{*2}	W
Power dissipation 2	Pd2	0.70 ^{*3}	W
Power dissipation 3	Pd3	1.21 ^{*4}	W
Power dissipation 4	Pd4	3.56 ^{*5}	W
Operating temperature range	Topr	-10~+100	°C
Storage temperature range	Tstg	-55~+150	°C
Junction Temperature	Tjmax	+150	°C

^{*1} Should not exceed Pd.

^{*2} Reduced by 2.7mW/°C for each increase in Ta ≥ 25°C (no heat sink)

^{*3} Reduced by 5.6mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:No substrate surface copper foil area.

^{*4} Reduced by 9.7mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:4layer, substrate surface copper foil area 10.29mm².

^{*5} Reduced by 28.5mW for each increase in Ta of 1°C over 25°C. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB.)
:4layer, substrate surface copper foil area 5505mm².

○OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage 1	V _{CC}	4.3	5.5	V
Supply Voltage 2	V _{IN}	0.7	V _{CC} -1 ^{*6}	V
Supply Voltage 3	V _{DD}	2.7	5.5	V
Output Voltage	V _O	0.65	2.7	V
Enable Input Voltage	V _{EN}	0	5.5	V
PGOOD Input Voltage	V _{PGOOD}	0	5.5	V
Capacitor in NRCS pin	C _{NRCS}	0.001	1	uF

^{*6} Order of V_{CC} and V_{IN} does not matter

★ This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

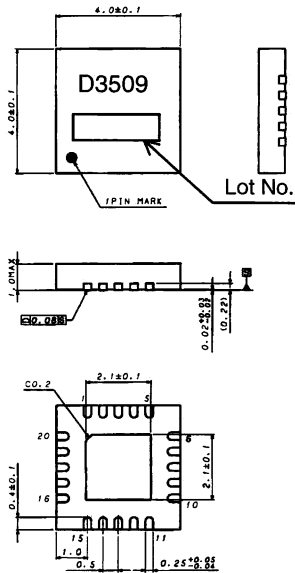
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○ELECTRICAL CHARACTERISTICS

 (Unless otherwise specified, Ta=25°C V_{CC}=5V V_{DD}=3.3V V_{EN}=3V V_{IN}=1.5V R1=3.9kΩ R2=3.6kΩ)

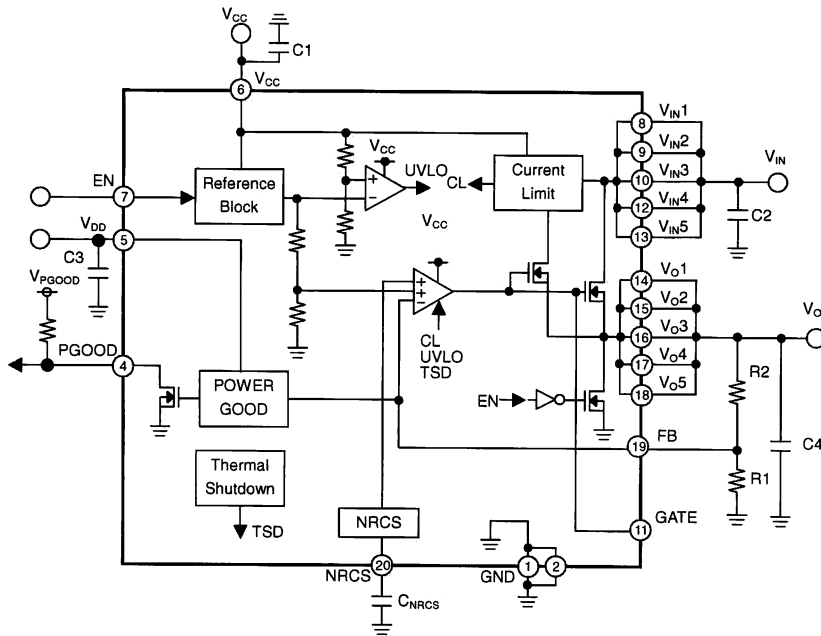
PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Bias current	I _{CC}	-	1.2	2.0	mA	
Shut-Down Mode Current	I _{ST}	-	0	10	uA	V _{EN} =0V
Maximum Output Current	I _O	4.0	-	-	A	
Feed Back Voltage 1	V _{FB1}	0.643	0.650	0.657	V	
Feed Back Voltage 2	V _{FB2}	0.637	0.650	0.663	V	I _O =0 to 4A Tj=-10 to 100°C
Line Regulation 1	REG.1	-	0.1	0.5	%/V	V _{CC} =4.3V to 5.5V
Line Regulation 2	REG.2	-	0.1	0.5	%/V	V _{IN} =1.2V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I _O =0 to 4A
Dropout Voltage	dV _O	-	28	50	mV	I _O =1A, V _{IN} =1.25V Tj=-10 to 100°C
Standby Discharge Current	I _{DEN}	1	-	-	mA	V _{EN} =0V, V _O =1V
[Enable]						
High level Enable Input Voltage	EN _{HIGH}	2	-	-	V	
Low level Enable Input Voltage	EN _{LOW}	0	-	0.8	V	
Enable pin Input Current	I _{EN}	-	7	10	uA	V _{EN} =3V
[Voltage Feed Back]						
Feed Back terminal Bias Current	I _{FB}	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	I _{NRCS}	14	20	26	uA	V _{NRCS} =0.5V
NRCS Standby Voltage	V _{STB}	-	0	50	mV	V _{EN} =0V
[UVLO]						
VCC UVLO	V _{CCUVLO}	3.5	3.8	4.1	V	V _{CC} :Sweep-up
VCC UVLO Hysteresis	V _{CCHYS}	100	160	220	mV	V _{CC} :Sweep-down
[AMP]						
Gate Source Current	I _{GSO}	6	10	14	mA	V _{FB} =0, V _{GATE} =2.5V
Gate Sink Current	I _{GSI}	11	18	25	mA	V _{FB} =V _{CC} , V _{GATE} =2.5V
[PGOOD]						
Threshold Voltage	V _{THPG}	0.565	0.585	0.605	V	FB voltage
Ron	R _{PG}	-	0.1	0.3	kΩ	

○ PHYSICAL DIMENSION



(Unit:mm)
Package name : VQFN020V4040

○ BLOCK DIAGRAM



○ Pin number Pin name

PIN No.	Pin name
1	GND
2	GND
3	N.C*
4	PGOOD
5	V _{DD}
6	V _{CC}
7	EN
8	V _{IN1}
9	V _{IN2}
10	V _{IN3}
11	GATE
12	V _{IN4}
13	V _{IN5}
14	V _{O1}
15	V _{O2}
16	V _{O3}
17	V _{O4}
18	V _{O5}
19	FB
20	NRCS
-	FIN

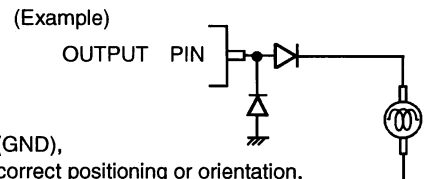
* Please short N.C to the GND

○ NOTES FOR USE

- (1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.
- (2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.
- (3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.
- (4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.
- (5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.
- (6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	15

- (7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.
- (8) Output Voltage Setting (R1, R2)
Output voltage is adjusted with resistor R1 and R2. output voltage is calculated as $V_{FB} \times (R1+R2)/R1$. Total 10kohm resistor (R1+R2) is recommended so that the output voltage is not affected by the FB bias current (Typ. 100nA).
- (9) Output Capacitor (C4)
Mount an output capacitor between V_{O1} to V_{O5} and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 150uF polymer capacitor is recommended. However, the stability depends on the characteristics of temperature and load. And if several kinds of capacitors are utilized in parallel, the output voltage may oscillate due to lack of phase margin. Please confirm operation across a variety of temperature and load conditions.
- (10) Input Capacitor (C1, C2, C3)
The input capacitor reduces the output impedance of the voltage supply source connected in the V_{CC} and V_{IN} . If the output impedance of this power supply increases, the input voltage (V_{CC}, V_{IN}, V_{DD}) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 10uF capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.
- (11) NRCS (Non Rush Current on Start-up) Setting (C_{NRCS})
The NRCS function is built in this IC to prevent rush current from going through the load (V_{IN} to V_O) for start-up. The constant current comes from the NRCS pin when EN is high or UVLO function is deactivated. Temporary reference voltage is made proportional to time due to current charge the NRCS pin capacitor and make output voltage start up proportional to this reference voltage. To obtain a stable NRCS delay time, a capacitor (X5R or X7R) with susceptibility to temperature is recommended.
- (12) Input Terminal ($V_{CC}, V_{IN}, V_{DD}, EN$)
The EN, V_{IN} , V_{DD} and V_{CC} are isolated. The UVLO protects incorrect operation when the voltage level of V_{CC} are low. The output becomes high when V_{CC} and EN reach the individual threshold level independent of the start-up pin order. When V_{IN} is the last on power-on sequence, the output voltage may over shoot.
- (13) Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.
- (14) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.
- (15) Short-circuits between pins and mounting errors
Do not short-circuit between output pin (V_O) and supply pin (V_{CC}, V_{IN}, V_{DD}) or ground (GND), or between supply pin (V_{CC}, V_{IN}, V_{DD}) and ground (GND). Mounting errors, such as incorrect positioning or orientation, destroy the device.



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