Data Sheet | February 11, 2005 | FN7049.1

Differential Line Receiver

The EL2142 is a very high bandwidth amplifier designed to extract the difference signal from noisy environments, and is thus primarily targeted for applications such as receiving signals from twisted pair lines, or any application where common mode noise injection is likely to occur.

The EL2142 is stable for a gain of one, and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (V_{REF}), which has a -3dB bandwidth of over 100MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The output can deliver a minimum of ±50mA and is short circuit protected to withstand a temporary overload condition.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL2142CS	8-pin SOIC	-	MDP0027
EL2142CS-T7	8-pin SOIC	7”	MDP0027
EL2142CS-T13	8-pin SOIC	13”	MDP0027
EL2142CSZ (See Note)	8-pin SOIC (Pb-free)	-	MDP0027
EL2142CSZ-T7 (See Note)	8-pin SOIC (Pb-free)	7”	MDP0027
EL2142CSZ-T13 (See Note)	8-pin SOIC (Pb-free)	13”	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

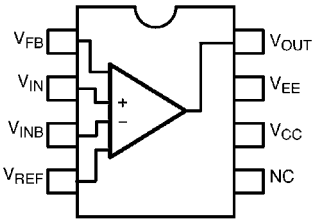
- Differential input range ±2.3V
- 150MHz 3dB bandwidth
- 400V/µs slewrate
- ±5V supplies or single supply
- 50mA minimum output current
- Output swing (100Ω load) to within 1.5V of supplies
- Low power-11mA typical supply current
- Pb-free available (RoHS compliant)

Applications

- Twisted pair receiver
- Differential line receiver
- VGA over twisted pair
- ADSL/HDSL receiver
- Differential to single ended amplification.
- Reception of analog signals in a noisy environment.

Pinout

EL2142
(8-PIN SOIC)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_{CC}–V_{EE}) 12.6V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +150°C
Recommended Operating Temperature . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_{CC} = +5V, V_{EE} = -5V, T_{EE} = 25°C, V_{IN}= 0V, R_L = 100, unless otherwise specified

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{SUPPLY}	Supply Operating Range (V_{CC}-V_{EE})	±3.0	±5.0	±6.3	V
I_S	Power Supply Current (no load)		11	14	mA
V_{OS}	Input Referred Offset Voltage	-25	10	40	mV
I_{IN}	Input Bias Current (V_{IN}, V_{IN}B, V_{REF})	-20	6	20	µA
Z_{IN}	Differential Input Resistance		400		kΩ
C_{IN}	Differential Input Capacitance		1		pF
V_{DIFF}	Differential Input Range	±2.0	±2.3		V
A_{VOL}	Open Loop Voltage Gain		75		dB
V_{IN}	Input Common Mode Voltage Range	-2.6		+4.0	V
V_{OUT}	Output Voltage Swing (50Ω load to GND)	±2.9	±3.1		V
I_{OUT}(min)	Minimum Output Current	50	60		mA
V_N	Input Referred Voltage Noise		36		nV/√Hz
V_{REF}	Output Voltage Control Range	-2.5		+3.3	V
PSRR	Power Supply Rejection Ratio	60	70		dB
CMRR2	Input Common Mode Rejection Ratio (V_{IN}= ±2V)	60	70		dB
CMRR1	Input Common Mode Rejection Ratio (full V_{IN} range)	50	60		dB

AC Electrical Specifications

V_{CC} = +5V, V_{EE} = -5V, T_A = 25C, V_{IN} = 0V, R_{LOAD} = 100, unless otherwise specified

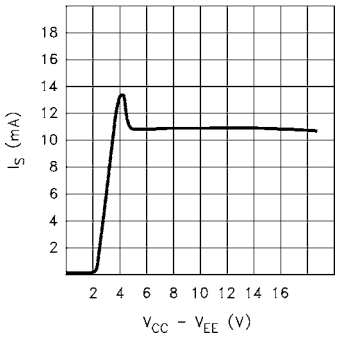
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
BW(-3dB)	-3dB Bandwidth (Gain =1)		150		MHz
SR	Slewrate		400		V/µs
T_{STL}	Settling time to 1%		15		ns
GBWP	Gain bandwidth product		200		MHz
V_{REF}BW(-3dB)	V_{REF} -3dB Bandwidth		130		MHz
V_{REF}SR	V_{REF} Slewrate		100		V/µsec
dG	Differential gain at 3.58MHz		0.2		%
dθ	Differential phase at 3.58MHz		0.2		°

Pin Descriptions

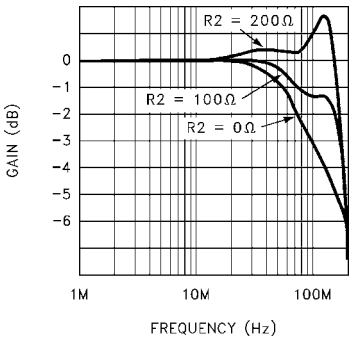
PIN NUMBER	PIN NAME	FUNCTION
1	V_{FB}	Feedback input
2	V_{IN}	Non-inverting input
3	V_{INB}	Inverting input
4	V_{REF}	Sets output voltage level to V_{REF} when $V_{IN}=V_{INB}$
5	NC	
6	V_{CC}	Positive supply voltage
7	V_{EE}	Negative supply voltage
8	V_{OUT}	Output voltage

Typical Performance Curves

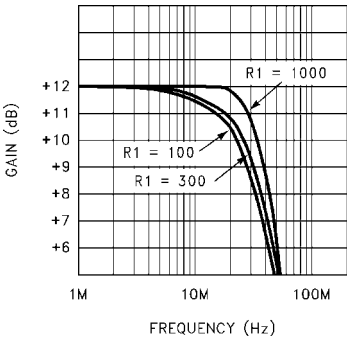
I_S vs Supply Voltage



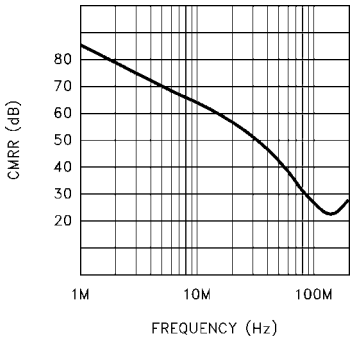
Frequency Response (Gain = 1)



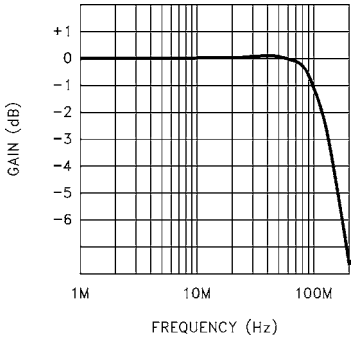
Frequency Response vs Resistor R1 (Gain = 4)



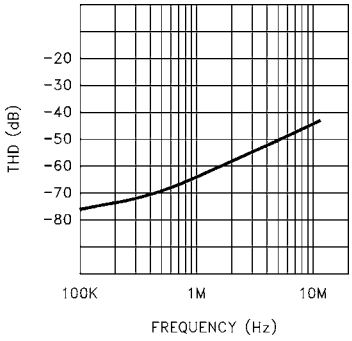
CMRR vs Frequency



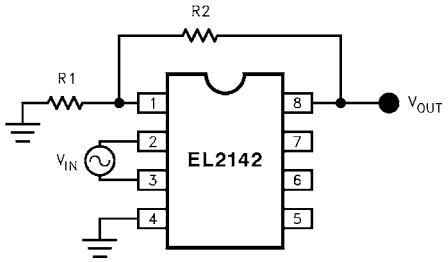
V_{REF} Frequency Response



Distortion vs Frequency (Gain = 3, R_{LOAD} = 100Ω) V_{IN} = $2V_{PK-PK}$



Applications Information



Gain Equation

V_{OUT} = ((R2+R1)/R1) x (V_{IN}-V_{INB}+V_{REF}) when R1 tied to GND

V_{OUT} = ((R2+R1)/R1) x (V_{IN}-V_{INB}) when R1 tied to V_{REF}

Choice of Feedback Resistor

For a gain of one, V_{OUT} may be shorted back to V_{FB}, but 100Ω-200Ω improves the bandwidth. For gains greater than one, there is little to be gained from choosing resistor R1 value below 200Ω, for it would only result in increased power dissipation and potential signal distortion. Above 200Ω, the bandwidth response will develop some peaking (for a gain of one), but substantially higher R1 values may be used for higher voltage gains, such as up to 1kΩ at a gain of four before peaking will develop.

Capacitance Considerations

As with many high bandwidth amplifiers, the EL2142 prefers not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} is kept below 10pF if the user does not want gain peaking to develop. The V_{FB} node forms a potential pole in the feedback loop, so capacitance should be minimized on this node for maximum bandwidth.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Typical Applications Circuits

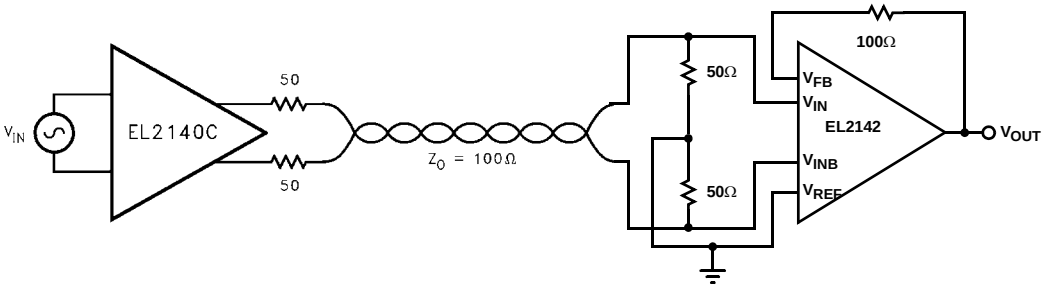


FIGURE 1. TYPICAL TWISTED PAIR APPLICATION

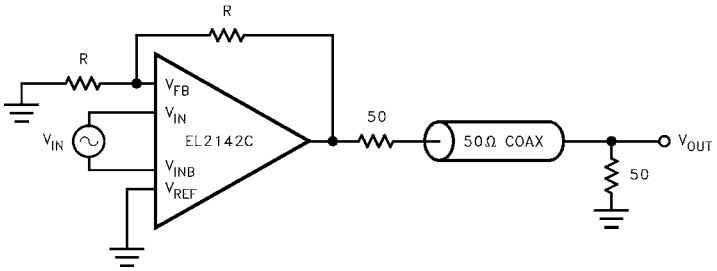


FIGURE 2. COAXIAL CABLE DRIVER PAIR APPLICATION

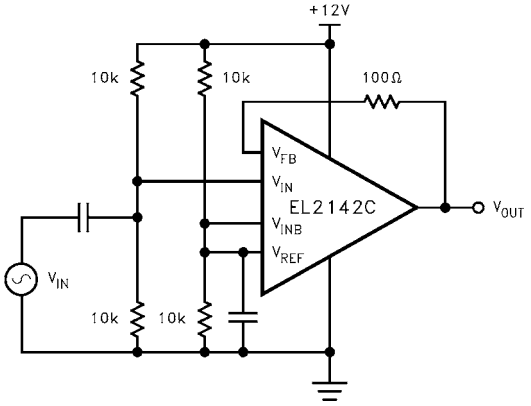


FIGURE 3. SINGLE SUPPLY RECEIVER

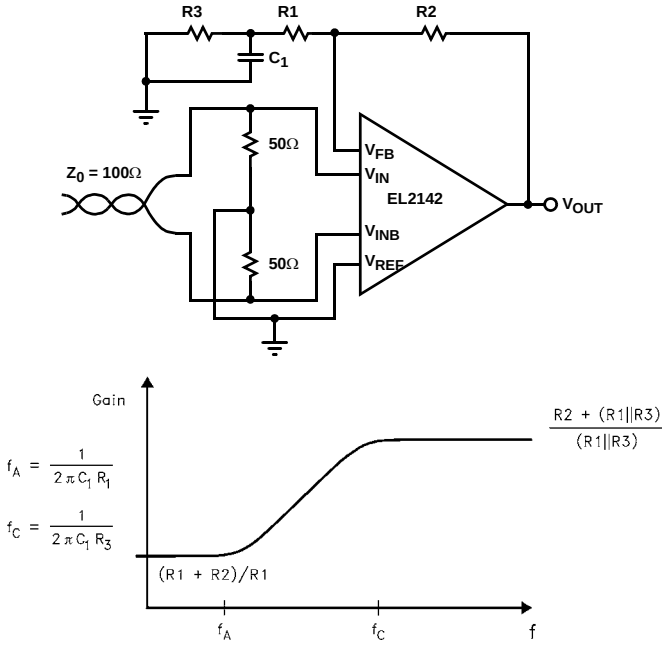


FIGURE 4. COMPENSATED LINE RECEIVER

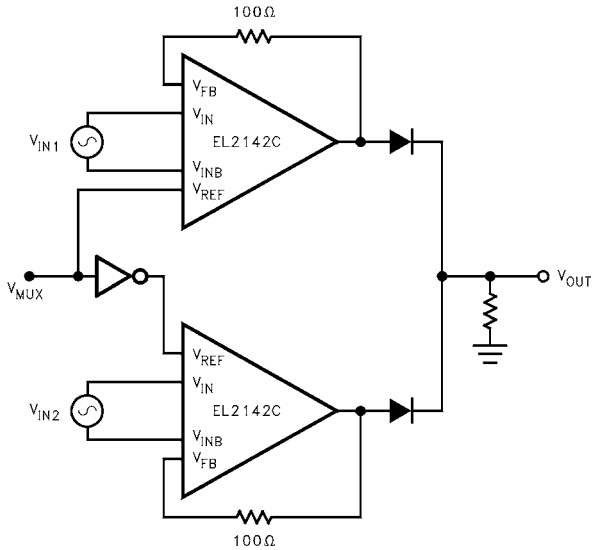
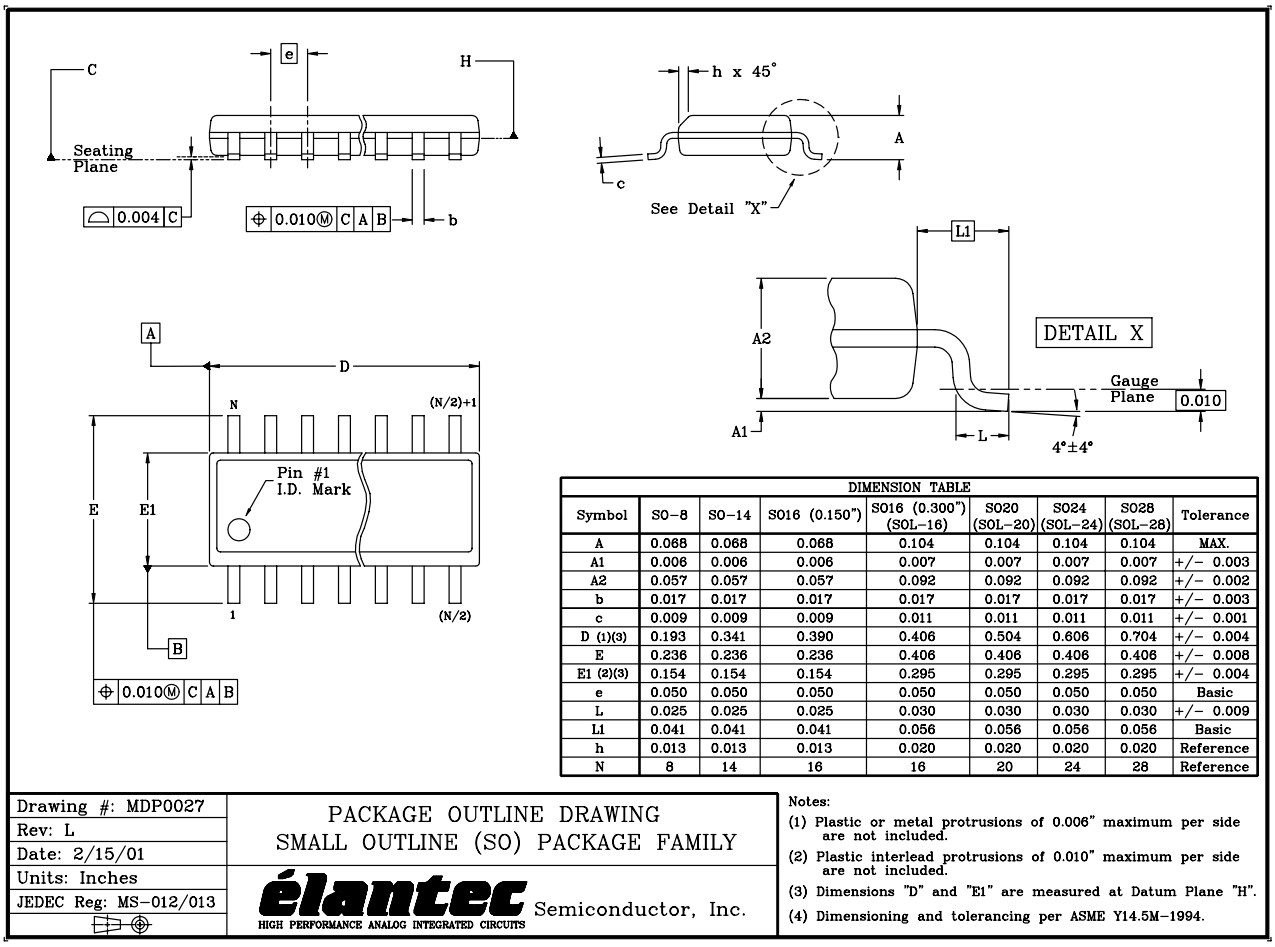


FIGURE 5. TWO CHANNEL MULTIPLEXER

SOIC Package Outline Drawing



DIMENSION TABLE								
Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>