- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow Power Consumption:
  - Active Mode: 270 μA at 1 MHz, 2.2 V
  - Standby Mode: 0.7 μA
  - Off Mode (RAM Retention): 0.1 μA
- Ultrafast Wake-Up From Standby Mode in Less Than 1 μs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Hardware Multiplier
- Basic Clock Module Configurations:
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%
  - Internal Very Low Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - High-Frequency (HF) Crystal up to 16 MHz
  - Resonator
  - External Digital Clock Source
  - External Resistor
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Three Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- Universal Serial Communication Interface
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Bootstrap Loader in Flash Devices
- On-Chip Emulation Module
- Family Members Include
  MSP430F2330
  8KB + 256B Flash Memory
  1KB RAM
  MSP430F2350
  16KB + 256B Flash Memory
  2KB RAM
  MSP430F2370
  32KB + 256B Flash Memory
  2KB RAM
- Available in 40-Pin QFN Package and 49-Pin Die-Sized BGA Package
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430F23x0 series is an ultralow-power microcontroller with two built-in 16-bit timers, one universal serial communication interface (USCI), a versatile analog comparator, and 32 I/O pins.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS[†]

T_A	PACKAGED DEVICES[‡]	
	PLASTIC 49-PIN DSBGA (YFF)	PLASTIC 40-PIN QFN (RHA)
–40°C to 85°C	MSP430F2330IYFF MSP430F2350IYFF MSP430F2370IYFF	MSP430F2330IRHA MSP430F2350IRHA MSP430F2370IRHA
–40°C to 105°C	– – –	MSP430F2330TRHA MSP430F2350TRHA MSP430F2370TRHA

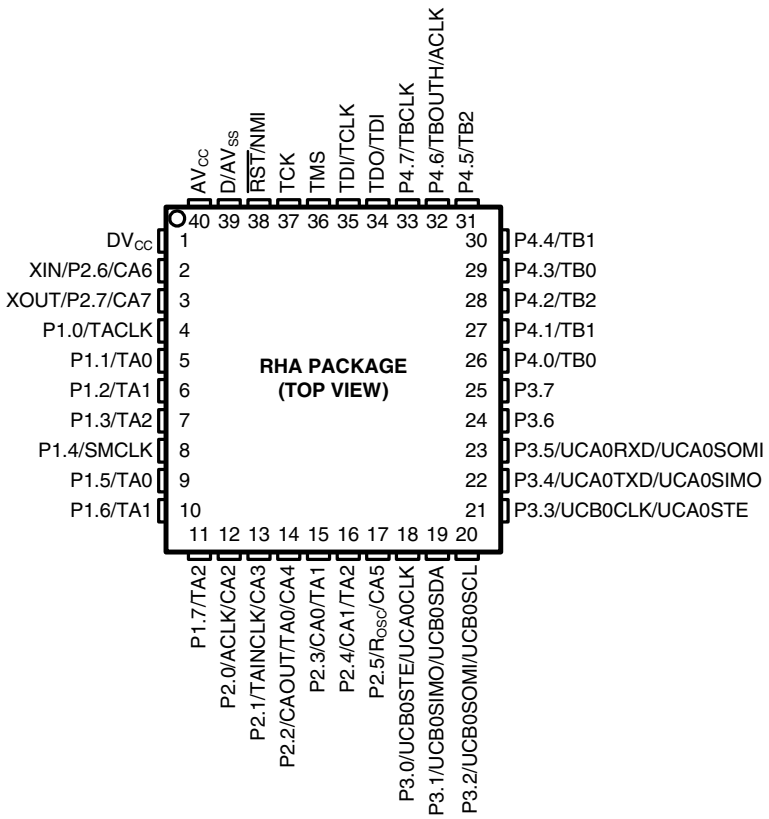
[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVELOPMENT TOOL SUPPORT

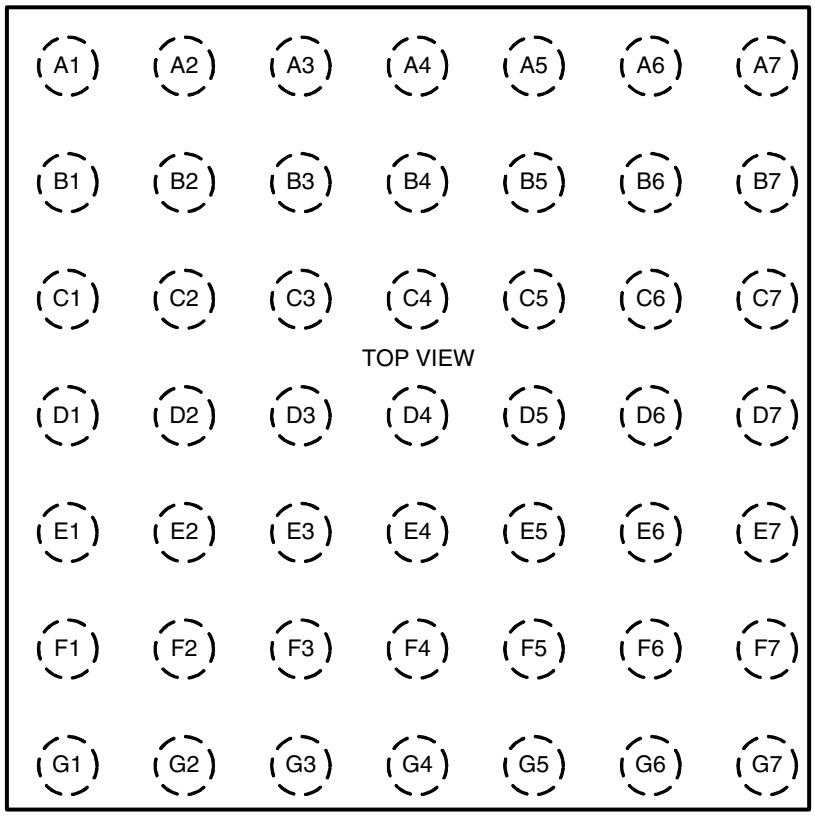
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface With Target Board
  - MSP-FET430U23X0 (RHA package)
- Production Programmer
  - MSP-GANG430

pin designation, MSP430F23x0IRHA and MSP430F23x0TRHA



pin designation, MSP430F23x0IYFF



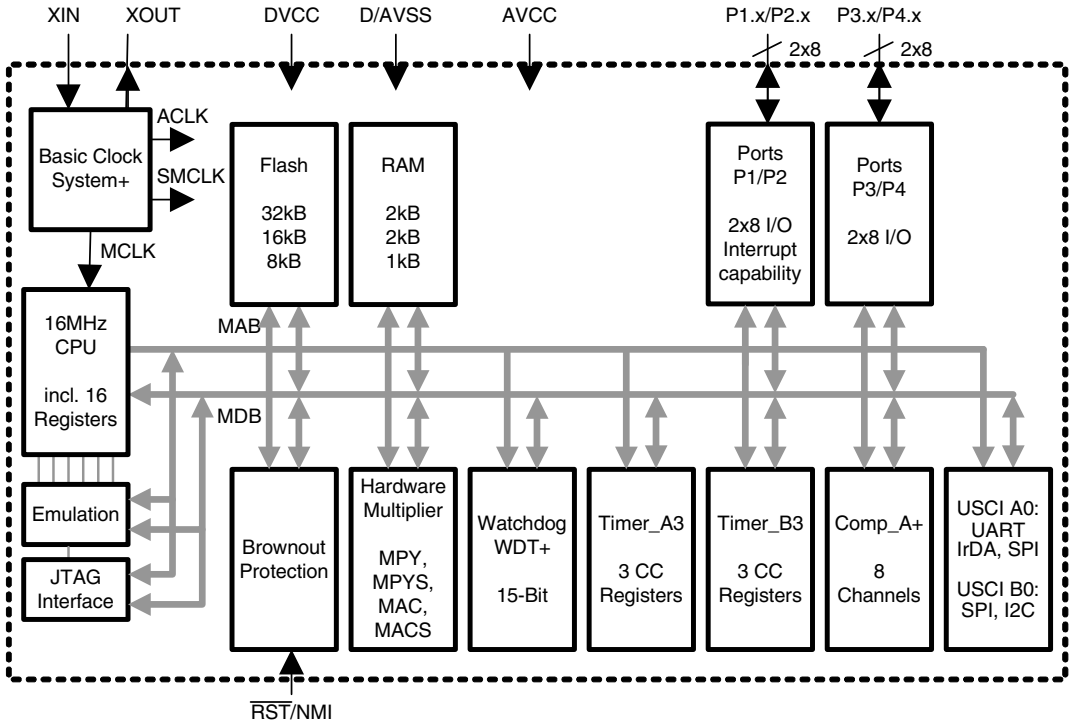
Package Dimensions

The package dimensions for this YFF package are shown in the following table. See the package drawing at the end of this data sheet for more details.

YFF Package Dimensions

PACKAGED DEVICES	D	E
MSP430F2370IYFF	3.20 ± 0.05 mm	3.20 ± 0.05 mm

functional block diagram



Terminal Functions

TERMINAL				DESCRIPTION
NAME	DS-BGA	QFN	I/O	
DV_{CC}	B3	1		Digital supply voltage, positive terminal. Supplies all digital parts.
XIN/P2.6/CA6	A2	2	I/O	Input terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input
XOUT/P2.7/CA7	A3	3	I/O	Output terminal of crystal oscillator/general-purpose digital I/O pin/Comparator_A input
P1.0/TACLK	B4	4	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	C4	5	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	A5	6	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	B5	7	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	A6	8	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	B6	9	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	A7	10	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	B7	11	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK/CA2	C5	12	I/O	General-purpose digital I/O pin/ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	C7	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK/Comparator_A input
P2.2/CAOUT/TA0/CA4	C6	14	I/O	General-purpose digital I/O pin/Comparator_A output/Timer_A, capture: CCI0B input/Comparator_A input
P2.3/CA0/TA1	D7	15	I/O	General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out1 output
P2.4/CA1/TA2	D6	16	I/O	General-purpose digital I/O pin/Comparator_A input/Timer_A, compare: Out2 output
P2.5/R_{OSC}/CA5	E7	17	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input
P3.0/UCB0STE/UCA0CLK	E6	18	I/O	General-purpose digital I/O pin/USCIB0 slave transmit enable/USCIA clock input/output
P3.1/UCB0SIMO/UCB0SDA	F7	19	I/O	General-purpose digital I/O pin/USCIB0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/UCB0SCL	F6	20	I/O	General-purpose digital I/O pin/USCIB0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	G7	21	I/O	General-purpose digital I/O/USCIB0 clock input/output, USCIA0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	G6	22	I/O	General-purpose digital I/O pin/USCIA0 transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/UCA0SOMI	G5	23	I/O	General-purpose digital I/O pin/USCIA0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6	F5	24	I/O	General-purpose digital I/O pin
P3.7	G4	25	I/O	General-purpose digital I/O pin
P4.0/TB0	F4	26	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A input, compare: Out0 output
P4.1/TB1	G3	27	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A input, compare: Out1 output
P4.2/TB2	G2	28	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A input, compare: Out2 output
P4.3/TB0	F3	29	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0B input, compare: Out0 output
P4.4/TB1	G1	30	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1B input, compare: Out1 output
P4.5/TB2	F1	31	I/O	General-purpose digital I/O pin/Timer_B, compare: Out2 output
P4.6/TBOUTH/ACLK	F2	32	I/O	General-purpose digital I/O pin/switch all PWM digital outputs to high impedance – Timer_B3: TB0 to TB2/ACLK output
P4.7/TBCLK	E2	33	I/O	General-purpose digital I/O pin/input clock TBCLK – Timer_B3
TDO/TDI	E1	34	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	D1	35	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	D2	36	I	Test mode select. TMS is used as an input port for device programming and test.

Terminal Functions (Continued)

TERMINAL				DESCRIPTION
NAME	BGA	QFN	I/O	
TCK	C1	37	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{RST}$/NMI	C2	38	I	Reset input, nonmaskable interrupt input port.
D/AV_{SS}	B1	39		Digital/Analog supply voltage, negative terminal.
AV_{CC}	A1	40		Analog supply voltage, positive terminal.
QFN Pad	–	NA	NA	QFN package pad connection to D/AV_{SS} recommended.
Reserved	A4 B2 C3 D3 D4 D5 E3 E4 E5	–	NA	BGA package GND balls. Connection to DV_{SS}/AV_{SS} is recommended.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE : S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash key violation PC out of range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0xFFFE	31, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 6)	(non)-maskable (non)-maskable (non)-maskable	0xFFFC	30
Timer_B3	TBCCR0 CCIFG (see Note 3)	maskable	0xFFFA	29
Timer_B3	TBCCR1 and TBCCR2, CCIFGs, TBIFG (see Notes 2 and 3)	maskable	0xFFF8	28
Comparator_A+	CAIFG	maskable	0xFFF6	27
Watchdog timer	WDTIFG	maskable	0xFFF4	26
Timer_A3	TACCR0 CCIFG (see Note 3)	maskable	0xFFF2	25
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG (see Notes 2 and 3)	maskable	0xFFF0	24
USCI_A0/USCI_B0 Receive USCI_B0 I2C Status	UCA0RXIFG, UCB0RXIFG (see Notes 2 and 4)	maskable	0xFFEE	23
USCI_A0/USCI_B0 Transmit USCI_B0 I2C Receive / Transmit	UCA0TXIFG, UCB0TXIFG (see Notes 2 and 5)	maskable	0xFFEC	22
			0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 3)	maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0xFFE4	18
			0xFFE2	17
			0xFFE0	16
(see Note 7)			0xFFDE	15
(see Note 8)			0xFFDC–0xFFC0	14–0, lowest

NOTES:
1. A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF).
2. Multiple source flags.
3. Interrupt flags are located in the module.
4. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
5. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
6. Non-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
   Non-maskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
7. This location is used as bootstrap loader security key (BSLSKEY).
   A 0xAA55 at this location disables the BSL completely.
   A zero (0h) disables the erasure of the flash if an invalid password is supplied.
8. The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE Oscillator fault enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive interrupt enable

UCA0TXIE USCI_A0 transmit interrupt enable

UCB0RXIE USCI_B0 receive interrupt enable

UCB0TXIE USCI_B0 transmit interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up

PORIFG Power-on interrupt flag. Set on V_{CC} power up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					UCB0TX IFG	UCB0RX IFG	UCA0TX IFG	UCA0RX IFG
					rw-0	rw-0	rw-0	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430F2330	MSP430F2350	MSP430F2370
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB Flash 0xFFFF - 0xFFC0 0xFFFF - 0xE000	16KB Flash 0xFFFF - 0xFFC0 0xFFFF - 0xC000	32KB 0xFFFF - 0xFFC0 0xFFFF - 0x8000
Information memory	Size Flash	256 Byte 0x10FF - 0x1000	256 Byte 0x10FF - 0x1000	256 Byte 0x10FF - 0x1000
Boot memory	Size ROM	1KB 0x0FFF - 0x0C00	1KB 0x0FFF - 0x0C00	1KB 0x0FFF - 0x0C00
RAM	Size	1KB Byte 0x5FF - 0x0200	2KB Byte 0x9FF - 0x0200	2KB 0x09FF - 0x0200
Peripherals	16-bit 8-bit 8-bit SFR	0x01FF - 0x0100 0x00FF - 0x0010 0x000F - 0x0000	0x01FF - 0x0100 0x00FF - 0x0010 0x000F - 0x0000	0x01FF - 0x0100 0x00FF - 0x0010 0x000F - 0x0000

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

BSL FUNCTION	YFF PACKAGE PINS	RHA PACKAGE PINS
Data transmit	C4 - P1.1	5 - P1.1
Data receive	C6 - P2.2	14 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide*, literature number SLAU144.

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very low power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

DCO CALIBRATION DATA (PROVIDED FROM FACTORY IN FLASH INFO MEMORY SEGMENT A)			
DCO FREQUENCY	**CALIBRATION REGISTER**	**SIZE**	**ADDRESS**
1 MHz	CALBC1_1MHZ	byte	0x10FF
	CALDCO_1MHZ	byte	0x10FE
8 MHz	CALBC1_8MHZ	byte	0x10FD
	CALDCO_8MHZ	byte	0x10FC
12 MHz	CALBC1_12MHZ	byte	0x10FB
	CALDCO_12MHZ	byte	0x10FA
16 MHz	CALBC1_16MHZ	byte	0x10F9
	CALDCO_16MHZ	byte	0x10F8

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There are four 8-bit I/O ports implemented—ports P1 through P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

The MSP430F23x0 devices provide 32 total port I/O pins available externally. See the device pinout for more information.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
YFF	RHA					YFF	RHA
B4 - P1.0	4 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
C7 - P2.1	13 - P2.1	TAINCLK	INCLK				
C4 - P1.1	5 - P1.1	TA0	CCI0A	CCR0	TA0	C4 - P1.1	5 - P1.1
C6 - P2.2	14 - P2.2	TA0	CCI0B			B6 - P1.5	9 – P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
A5 - P1.2	6 - P1.2	TA1	CCI1A	CCR1	TA1	A5 - P1.2	6 - P1.2
		CAOUT (internal)	CCI1B			A7 - P1.6	10 - P1.6
		V_{SS}	GND			D7 - P2.3	15 - P2.3
		V_{CC}	V_{CC}				
B5 - P1.3	7 - P1.3	TA2	CCI2A	CCR2	TA2	B5 - P1.3	7 - P1.3
		ACLK (internal)	CCI2B			B7 - P1.7	11 - P1.7
		V_{SS}	GND			D6 - P2.4	16 - P2.4
		V_{CC}	V_{CC}				

timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
YFF	RHA					YFF	RHA
E2 - P4.7	33 - P4.7	TBCLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
		$\overline{\text{TBCLK}}$	INCLK				
F4 - P4.0	26 - P4.0	TB0	CCI0A	CCR0	TB0	F4 - P4.0	26 - P4.0
F3 - P4.3	29 - P4.3	TB0	CCI0B			F3 - P4.3	29 - P4.3
		V_{SS}	GND				
		V_{CC}	V_{CC}				
G3 - P4.1	27 - P4.1	TA1	CCI1A	CCR1	TB1	G3 - P4.1	27 - P4.1
G1 – P4.4	30 – P4.4	TB1	CCI1B			G1 - P4.4	30 - P4.4
		V_{SS}	GND				
		V_{CC}	V_{CC}				
G2 - P4.2	28 - P4.2	TB2	CCI2A	CCR2	TB2	G2 - P4.2	28 - P4.2
		ACLK (internal)	CCI2B			F1 - P4.5	31 - P4.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				

universal serial communications interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 pin or 4 pin) or I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI A0 provides support for SPI (3 pin or 4 pin), UART, enhanced UART and IrDA.

USCI B0 provides support for SPI (3 pin or 4 pin) and I2C.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_B3	Capture/compare register	TBCCR2	0x0196
	Capture/compare register	TBCCR1	0x0194
	Capture/compare register	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control	TBCCTL2	0x0186
	Capture/compare control	TBCCTL1	0x0184
	Capture/compare control	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare register	TACCR2	0x0176
	Capture/compare register	TACCR1	0x0174
	Capture/compare register	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Capture/compare control	TACCTL2	0x0166
	Capture/compare control	TACCTL1	0x0164
	Capture/compare control	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed +accumulate/operand1	MACS	0x0136
	Multiply+accumulate/operand1	MAC	0x0134
	Multiply signed/operand1	MPYS	0x0132
	Multiply unsigned/operand1	MPY	0x0130
Watchdog Timer+	Watchdog/timer control	WDTCTL	0x0120
PERIPHERALS WITH BYTE ACCESS			
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	0x06F
	USCI_B0 receive buffer	UCB0RXBUF	0x06E
	USCI_B0 status	UCB0STAT	0x06D
	USCI_B0 bit rate control 1	UCB0BR1	0x06B
	USCI_B0 bit rate control 0	UCB0BR0	0x06A
	USCI_B0 control 1	UCB0CTL1	0x069
	USCI_B0 control 0	UCB0CTL0	0x068
	USCI_B0 I2C slave address	UCB0SA	0x011A
	USCI_B0 I2C own address	UCB0OA	0x0118
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	0x0067
	USCI_A0 receive buffer	UCA0RXBUF	0x0066
	USCI_A0 status	UCA0STAT	0x0065
	USCI_A0 modulation control	UCA0MCTL	0x0064
	USCI_A0 baud rate control 1	UCA0BR1	0x0063
	USCI_A0 baud rate control 0	UCA0BR0	0x0062
	USCI_A0 control 1	UCA0CTL1	0x0061
	USCI_A0 control 0	UCA0CTL0	0x0060
	USCI_A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI_A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI_A0 auto baud rate control	UCA0ABCTL	0x005D

PERIPHERALS WITH BYTE ACCESS (continued)			
Basic Clock System+	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Port P4	Port P4 resistor enable	P4REN	0x0011
	Port P4 selection	P4SEL	0x001F
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Function	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

absolute maximum ratings (see Note 1)

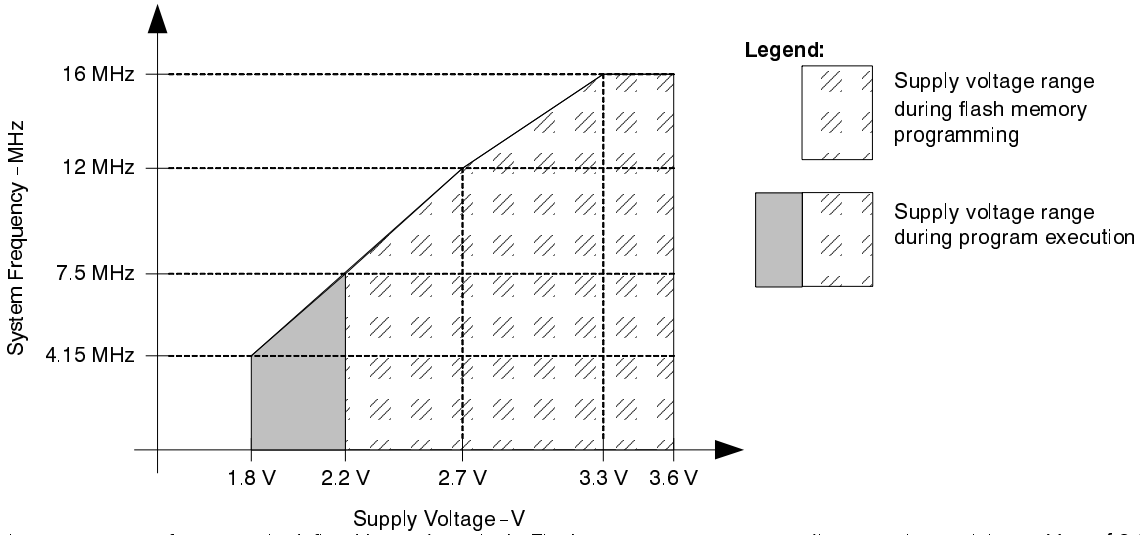
Voltage applied at V_{CC} to V_{SS} . . . . . −0.3 V to + 4.1 V
Voltage applied to any pin (see Note 2) . . . . . −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature: Unprogrammed device (see Note 3) . . . . . −55°C to 150°C
Programmed device (see Note 3) . . . . . −40°C to 105°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

PARAMETER		MIN	MAX	UNITS
Supply voltage during program execution, V_{CC}	AV_{CC} = DV_{CC} = V_{CC} (see Note 1)	1.8	3.6	V
Supply voltage during flash memory programming, V_{CC}	AV_{CC} = DV_{CC} = V_{CC} (see Note 1)	2.2	3.6	V
Supply voltage, V_{SS}	AV_{SS} = DV_{SS} = V_{SS}	0.0	0.0	V
Operating free-air temperature range, T_A	I version	−40	85	°C
	T version	−40	105	°C
Processor frequency $f_{SYSYTEM}$ (Maximum MCLK frequency) (see Notes 2 and 3 and Figure 1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%	dc	4.15	MHz
	V_{CC} = 2.7 V, Duty cycle = 50% ±10%	dc	12	
	V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	dc	16	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.
2. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
3. Modules might have a different maximum input clock specification. See the specification of the respective module in this datasheet.



NOTE : Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM, 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes from flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		270	370	µA
				3 V		390	550	
$I_{AM, 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		226		µA
				3 V		318		
$I_{AM, 4kHz}$	Active mode (AM) current (4kHz)	$f_{MCLK} = f_{SMCLK}$ = f_{ACLK} = 32,768 Hz/8 = 4,096 Hz, f_{DCO} = 0Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		2	6	µA
			105°C	2.2 V			14	
			–40°C to 85°C	3 V		3	9	
			105°C	3 V			17	
$I_{AM,100kHz}$	Active mode (AM) current (100kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100kHz, f_{ACLK} = 0Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–40°C to 85°C	2.2 V		60	85	µA
			105°C	2.2 V			95	
			–40°C to 85°C	3 V		72	95	
			105°C	3 V			105	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

typical characteristics - active mode supply current (into DV_{CC} + AV_{CC})

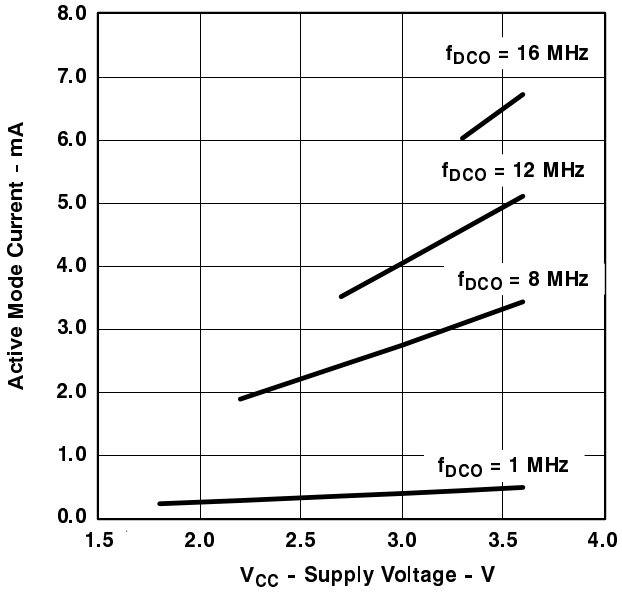


Figure 2. Active mode current vs V_{CC}, T_A = 25°C

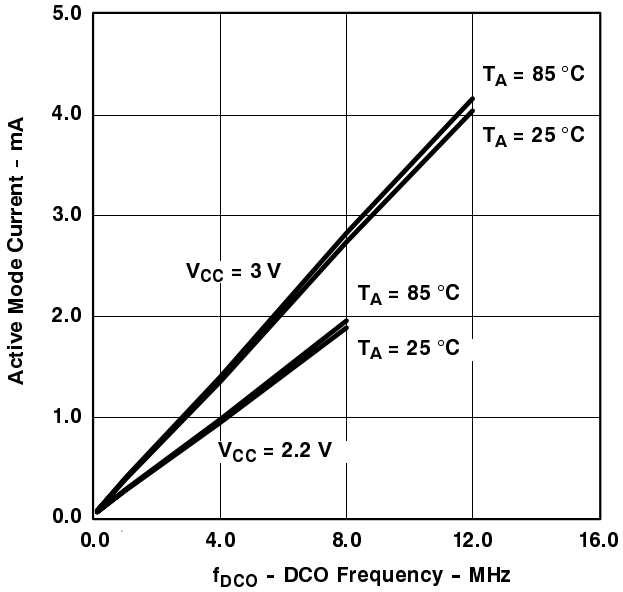


Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

low power mode supply currents (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0, 1MHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		68	84	µA
			105°C				90	µA
			–40°C to 85°C	3 V		88	110	µA
			105°C				115	µA
$I_{LPM0, 100kHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0MHz, $f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100kHz, f_{ACLK} = 0Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–40°C to 85°C	2.2 V		36	45	µA
			105°C				50	µA
			–40°C to 85°C	3 V		40	50	µA
			105°C				54	µA
I_{LPM2}	Low-power mode 2 (LPM2) current, see Note 4	$f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	–40°C to 85°C	2.2 V		20	28	µA
			105°C				32	µA
			–40°C to 85°C	3 V		23	32	µA
			105°C				37	µA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current, see Note 4	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–40°C to 25°C	2.2 V		0.7	1.0	µA
			85°C				3.3	
			105°C				10	
			–40°C to 25°C	3 V		0.85	1.2	µA
			85°C				3.8	
			105°C				12	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) see Note 4	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–40°C to 25°C	2.2 V		0.25	0.8	µA
			85°C				2.9	
			105°C				9	
			–40°C to 25°C	3 V		0.35	1.0	µA
			85°C				3.5	
			105°C				11	
I_{LPM4}	Low-power mode 4 (LPM4) current, see Note 5	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} = 0Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	–40°C	2.2V			0.5	µA
			25°C				0.5	
			85°C			1.7	2.7	
			105°C				8.6	
			–40°C	3V			0.5	µA
			25°C				0.5	
			85°C			1.9	3	
			105°C				9	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V–T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Schmitt-trigger inputs - Ports P1, P2, P3, P4, JTAG, $\overline{RST}$/NMI, and XIN (see Note)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			2.2 V	1.00		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			2.2 V	0.55		1.20	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

NOTE : XIN only in bypass mode.

inputs - Ports P1, P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger puls width to set interrupt flag, (see Note)	2.2 V/3 V	20			ns

NOTE : An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current - Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pull-up/pull-down resistor is disabled.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs - Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = -1.5 mA (see Notes 1)	2.2 V	V_{CC}-0.25		V_{CC}	V
		$I_{(OHmax)}$ = -6 mA (see Notes 2)	2.2 V	V_{CC}-0.6		V_{CC}	
		$I_{(OHmax)}$ = -1.5 mA (see Notes 1)	3 V	V_{CC}-0.25		V_{CC}	
		$I_{(OHmax)}$ = -6 mA (see Notes 2)	3 V	V_{CC}-0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	2.2 V	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	2.2 V	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Notes 1)	3 V	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Notes 2)	3 V	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency - Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (see Note 1 and 2)	2.2 V			7.5	MHz
			3 V			12	MHz
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (see Note 2)	2.2 V			7.5	MHz
			3 V			16	MHz

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

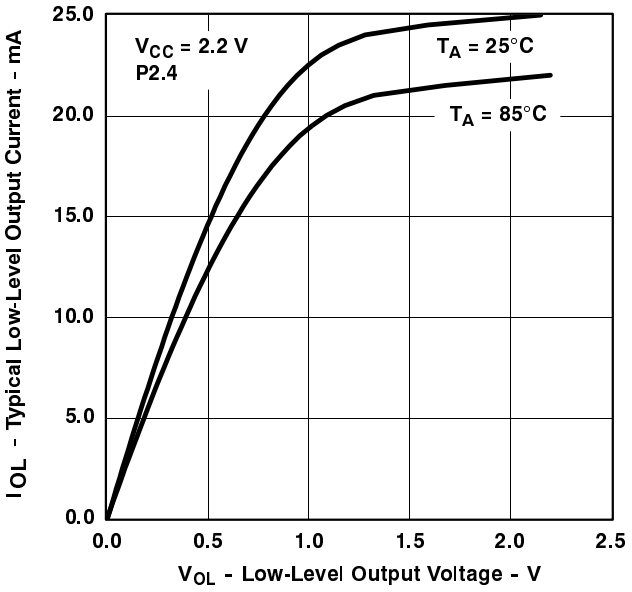


Figure 4

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

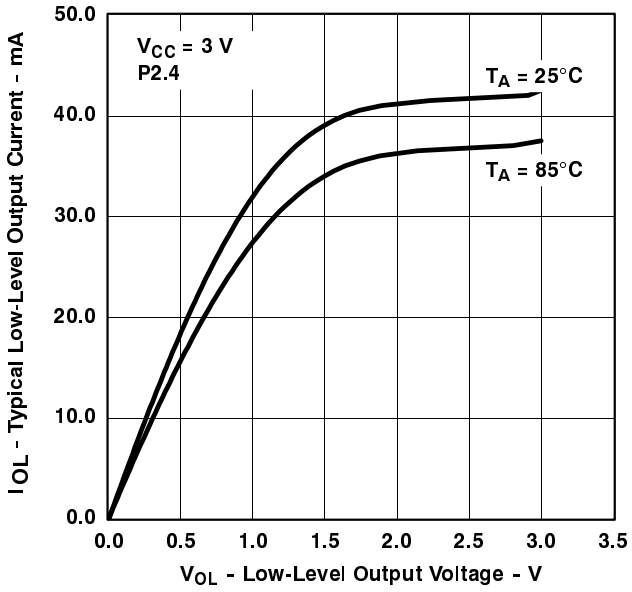


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

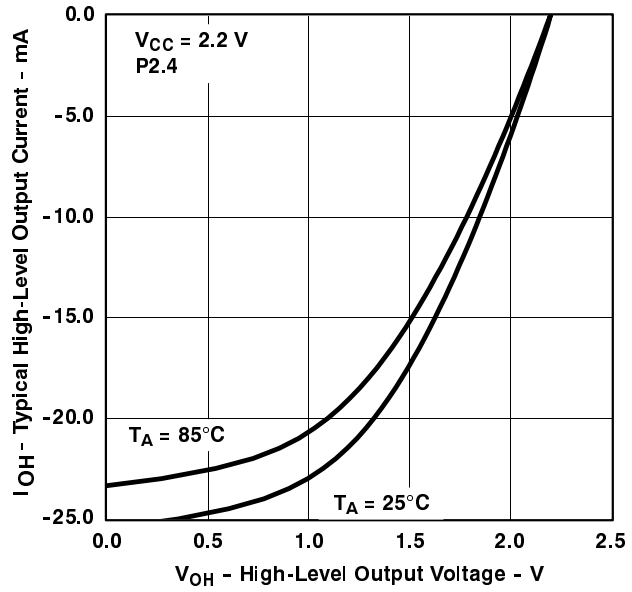


Figure 6

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

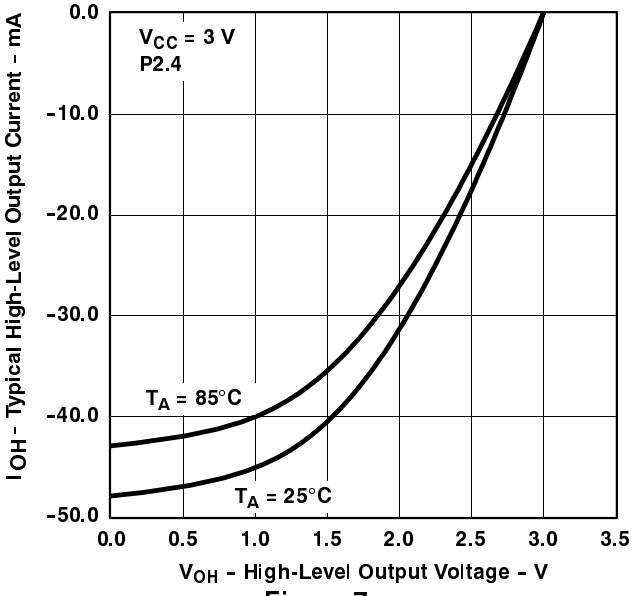


Figure 7

NOTE : One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s			$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	(see Figure 8 through Figure 10)	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	(see Figure 8)	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	(see Figure 8)					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

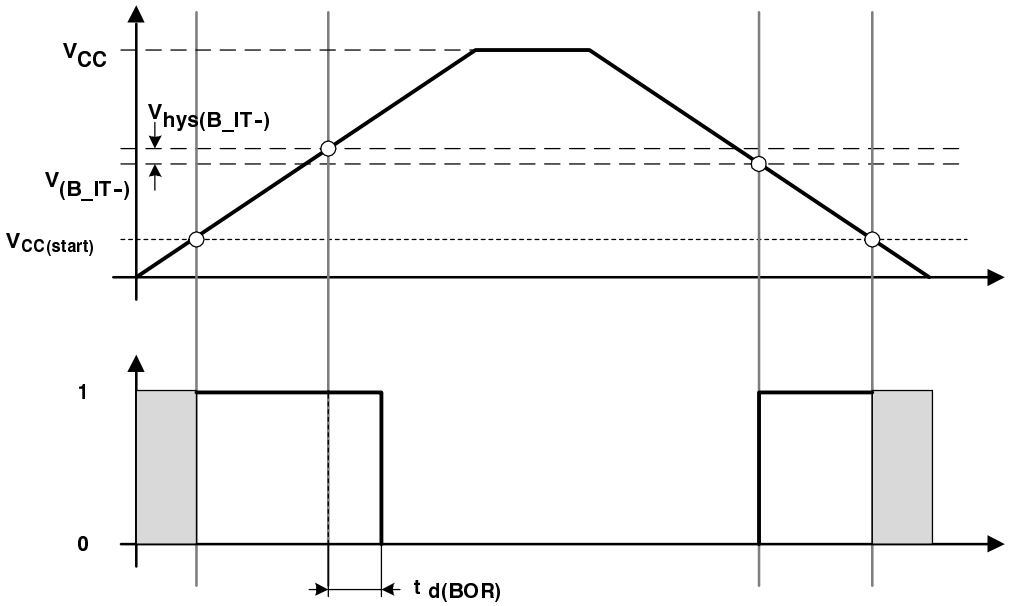


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)

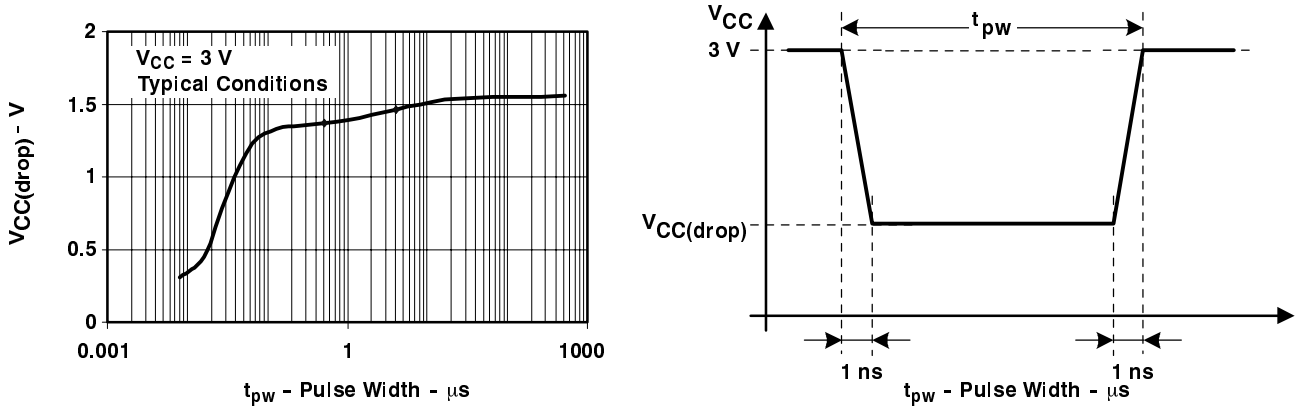


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

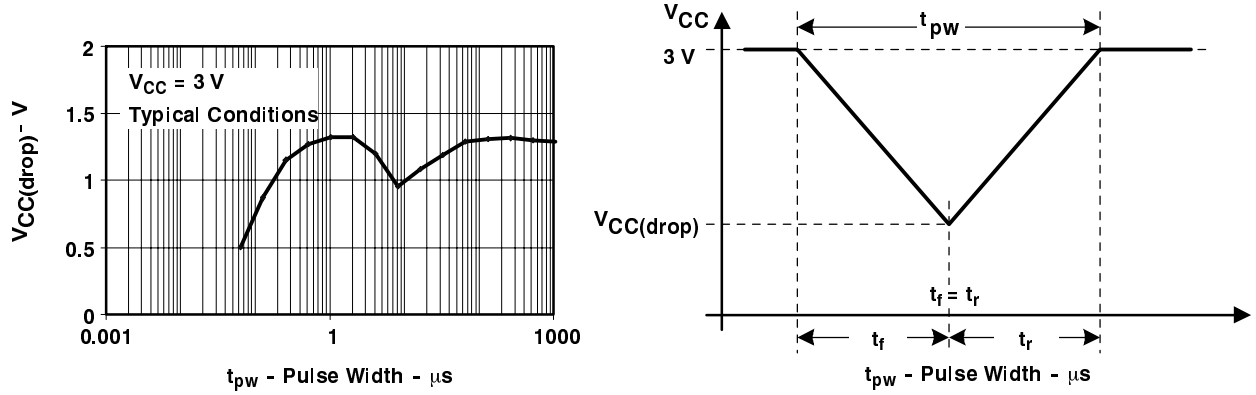


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3.0		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	
Duty cycle		Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies - tolerance at calibration

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	−1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies - tolerance over temperature 0°C to 85°C

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			0°C to 85°C	3.0 V	−2.5	±0.5	+2.5	%
8-MHz tolerance over temperature			0°C to 85°C	3.0 V	−2.5	±1	+2.5	%
12-MHz tolerance over temperature			0°C to 85°C	3.0 V	−2.5	±1	+2.5	%
16-MHz tolerance over temperature			0°C to 85°C	3.0 V	−3	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.970	1	1.030	MHz
				3.0 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.760	8	8.400	MHz
				3.0 V	7.800	8	8.200	
				3.6 V	7.600	8	8.240	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
				3.0 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3.0 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance over supply voltage V_{CC}

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1 MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	–3	±2	+3	%
8 MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	–3	±2	+3	%
12 MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	–3	±2	+3	%
16 MHz tolerance over V_{CC}			25°C	3.0 V to 3.6 V	–6	±2	+3	%
$f_{CAL(1MHz)}$	1MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8MHz calibration value	BCSCTL1= CALBC1_8MHZ , DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12MHz calibration value	BCSCTL1= CALBC1_12MHZ , DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3.0 V to 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies – overall tolerance

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall			–40°C to 105°C	1.8 V to 3.6 V	–5	±2	+5	%
8-MHz tolerance overall			–40°C to 105°C	1.8 V to 3.6 V	–5	±2	+5	%
12-MHz tolerance overall			–40°C to 105°C	2.2 V to 3.6 V	–5	±2	+5	%
16-MHz tolerance overall			–40°C to 105°C	3.0 V to 3.6 V	–6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	–40°C to 105°C	1.8 V to 3.6 V	0.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	–40°C to 105°C	1.8 V to 3.6 V	7.600	8	8.400	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	–40°C to 105°C	2.2 V to 3.6 V	11.40	12	12.60	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	–40°C to 105°C	3.0 V to 3.6 V	15.00	16	17.00	MHz

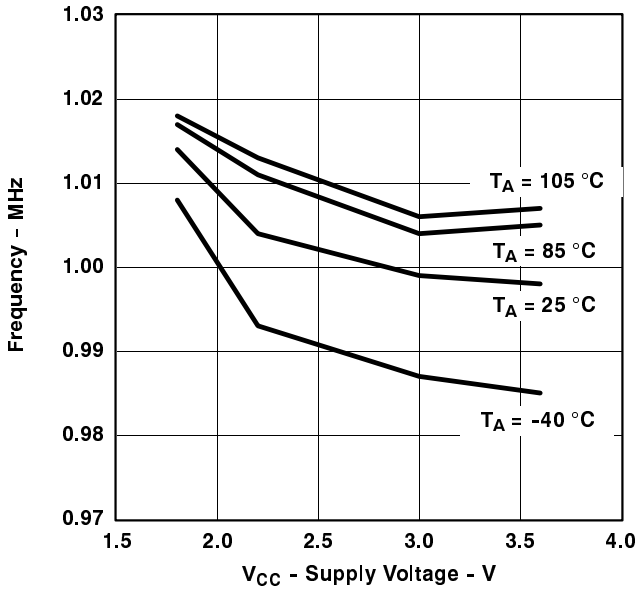


Figure 11. Calibrated 1-MHz Frequency vs V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	µs
		BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ	2.2 V/3 V			1.5	
		BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ	2.2 V/3 V			1	
		BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics – DCO clock wake-up time from LPM3/4

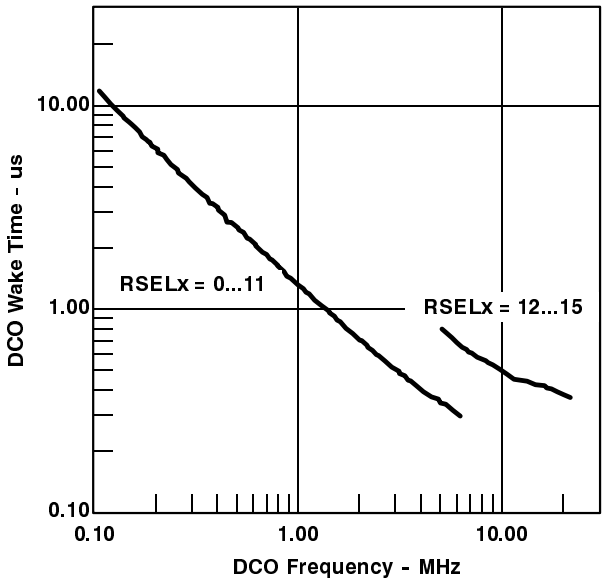


Figure 12. Clock Wake-Up Time From LPM3 vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO with external resistor R_{OSC} (see Note)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V		1.8		MHz
			3 V		1.95		
D_t	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		±0.1		%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		10		%/V

NOTE : R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

typical characteristics - DCO with external resistor R_{OSC}

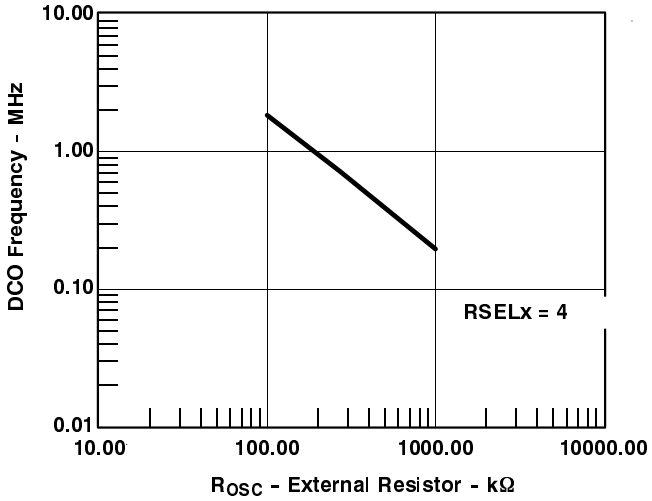


Figure 13. DCO Frequency vs R_{OSC}, V_{CC} = 2.2 V, T_A = 25°C

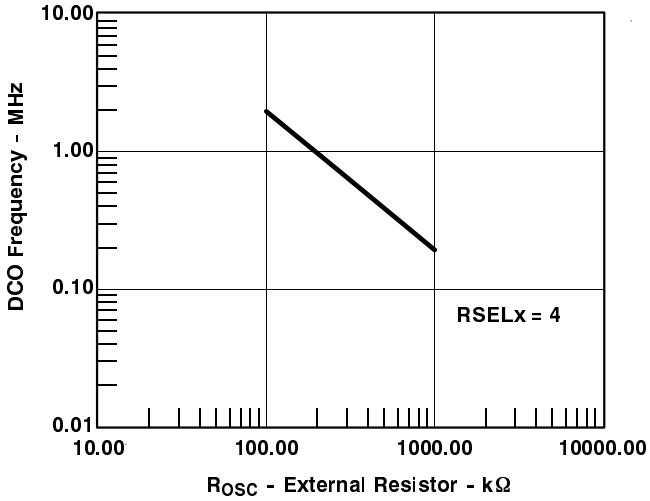


Figure 14. DCO Frequency vs R_{OSC}, V_{CC} = 3.0 V, T_A = 25°C

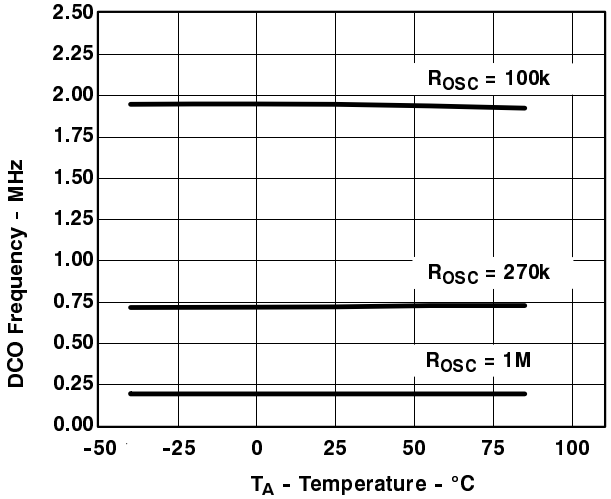


Figure 15. DCO Frequency vs Temperature, V_{CC} = 3.0 V

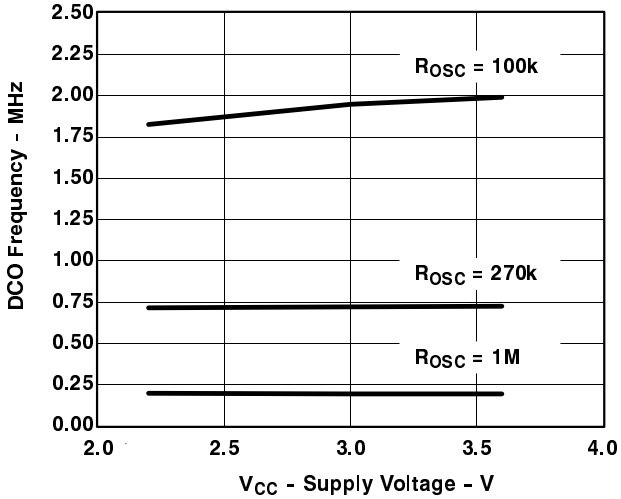


Figure 16. DCO Frequency vs V_{CC}, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		pF
		XTS = 0, XCAPx = 2			8.5		pF
		XTS = 0, XCAPx = 3			11		pF
Duty cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, XCAPx = 0. LFXT1Sx = 3 (see Note 2)	2.2 V/3 V	10		10000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		2.2 V/3 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift	See Note 1	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	See Note 2	1.8 V to 3.6 V		4		%/V

NOTES: 1. Calculated using the box method:
I Version: (MAX(–40...85°C) – MIN(–40...85°C))/MIN(–40...85°C)/(85°C – (–40°C))
T Version: (MAX(–40...105_C) – MIN(–40...105_C))/MIN(–40...105_C)/(105_C – (–40_C))
2. Calculated using the box method: (MAX(1.8...3.6V) – MIN(1.8...3.6V))/MIN(1.8...3.6V)/(3.6V – 1.8V)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, high frequency modes (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, XCAPx = 0, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, XCAPx = 0, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, XCAPx = 0, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3.0 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic level square wave input frequency, HF mode	XTS = 1, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3.0 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 17 and Figure 18)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	XTS = 1, XCAPx = 0 (see Note 2)			1		pF
Duty cycle	HF mode	XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V/3 V	40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency, HF mode (see Note 4)	XTS = 1, XCAPx = 0, LFXT1Sx = 3 (see Notes 3)	2.2 V/3 V	30		300	kHz

NOTES:
1. Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - LFXT1 oscillator in HF mode (XTS = 1)

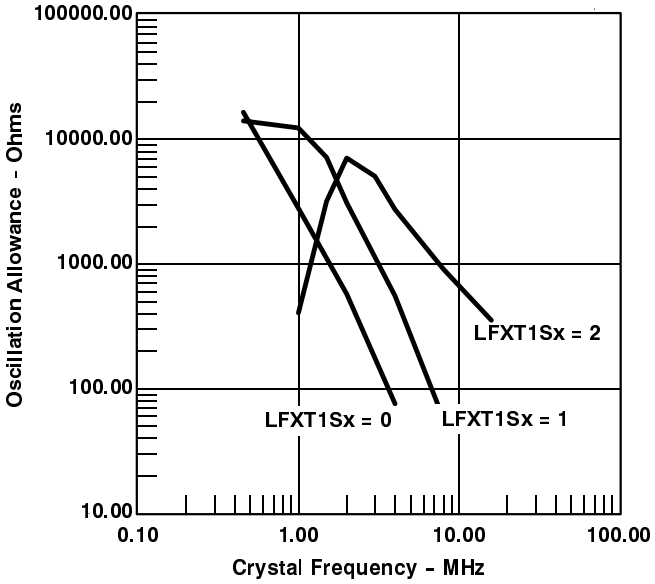


Figure 17. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

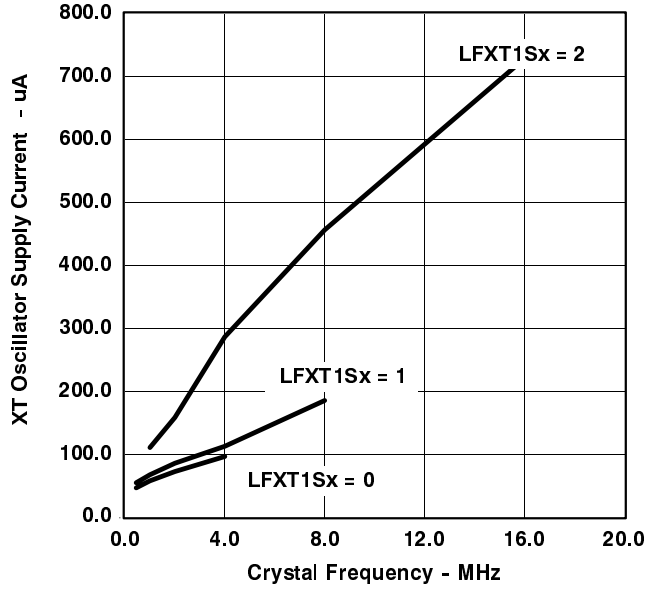


Figure 18. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TB,cap}$	Timer_B, capture timing	TB0, TB1, TB2	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baud rate in MBaud) (see Note 6)		2.2V /3 V	2			MHz
t_τ	UART receive deglitch time (see Note 7)		2.2 V	50	150		ns
			3 V	50	100		ns

NOTES: 6. The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.
7. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 19 and Figure 20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110			ns
			3 V	75			ns
$t_{HD,MI}$	SOMI input data hold time		2.2 V				ns
			3 V				ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			30	ns
			3 V			20	ns

NOTE : $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 21 and Figure 22)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	ns

NOTE : $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)8

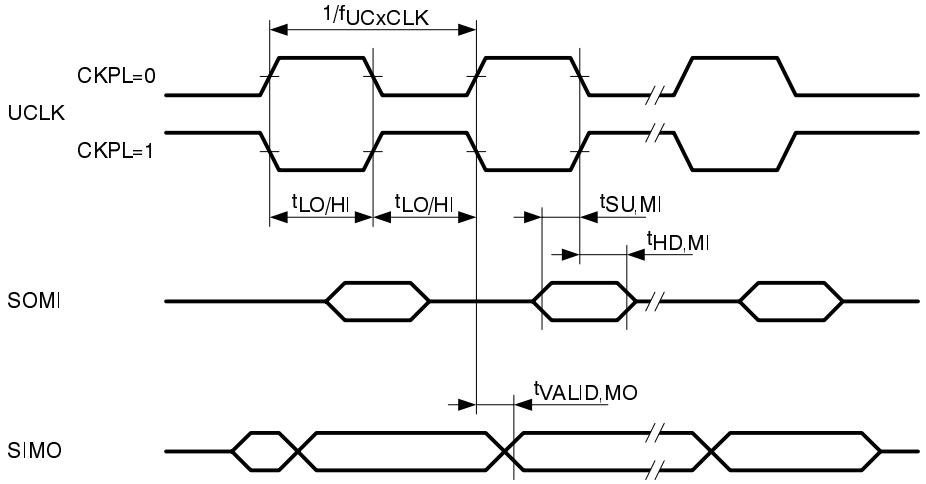


Figure 19. SPI Master Mode, CKPH = 0

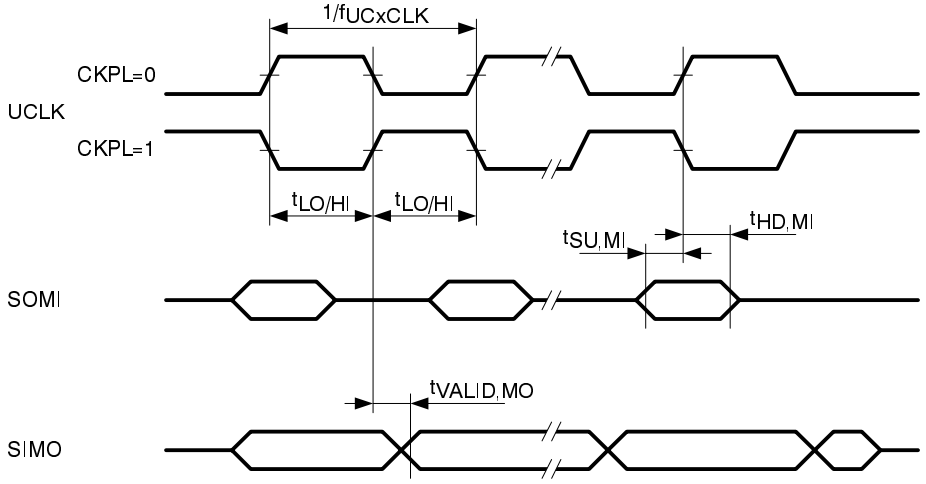


Figure 20. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)9

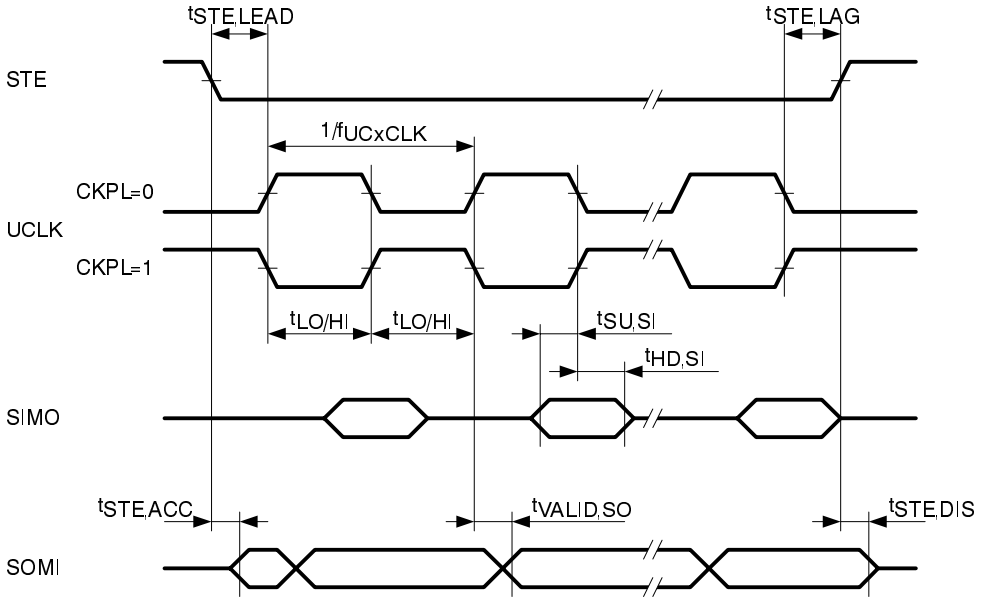


Figure 21. SPI Slave Mode, CKPH = 0

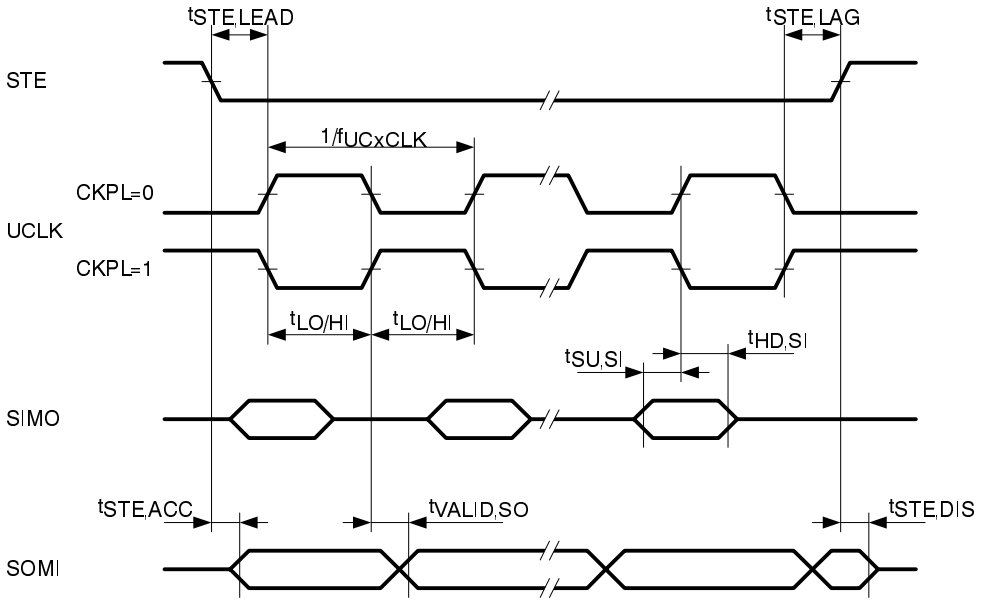


Figure 22. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 23)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.7			µs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

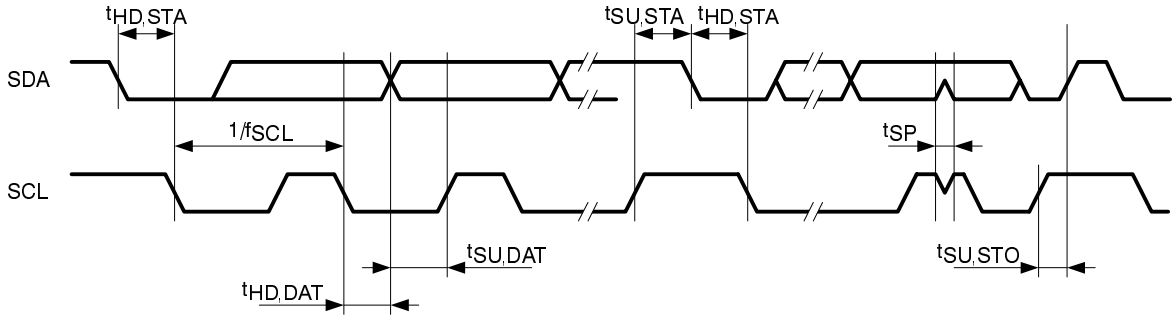


Figure 23. I2C Mode Timing

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Comparator_A+ (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	2.2 V		25	40	μA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P1.0/CA0 and P1.1/CA1	2.2 V		30	50	μA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON=1	2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC}\text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0 and P2.4/CA1	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5}V_{CC}\text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0 and P2.4/CA1	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 27 and Figure 28)	PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0 and P2.4/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	-30		30	mV
V_{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0 (see Note 3, Figure 24 and Figure 25)	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1 (see Note 3, Figure 24 and Figure 25)	2.2 V	1.4	1.9	2.8	μs
			3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
3. Response time measured at P1.3/CAOUT.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

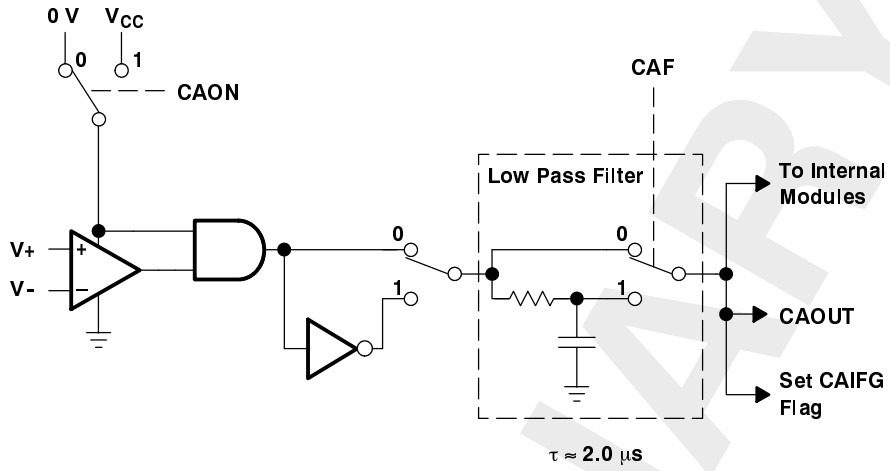


Figure 24. Block Diagram of Comparator_A+ Module

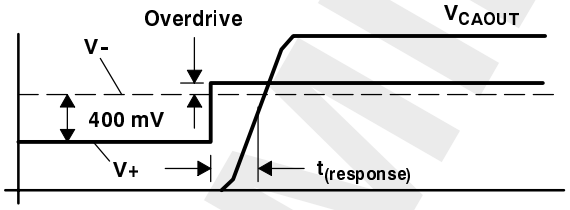


Figure 25. Overdrive Definition

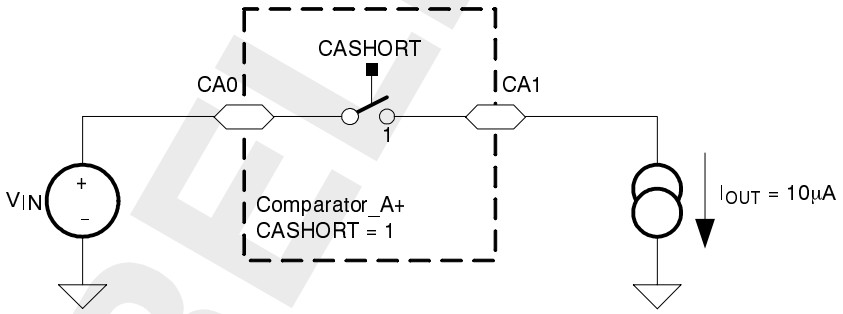


Figure 26. Comparator_A+ Short Resistance Test Condition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - Comparator_A+

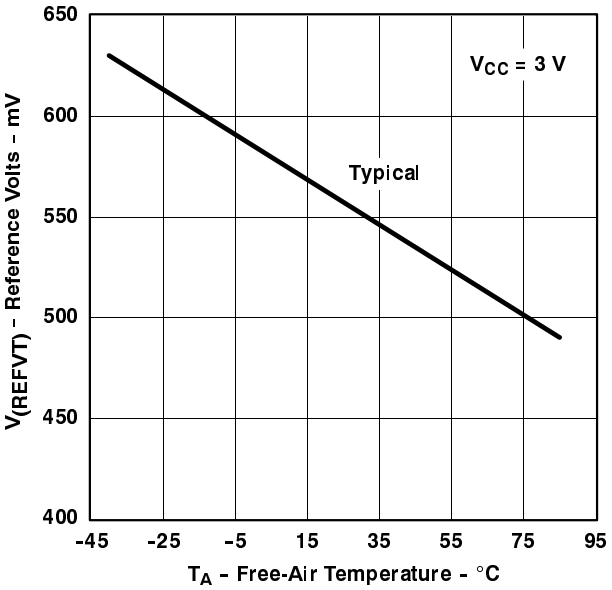


Figure 27. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

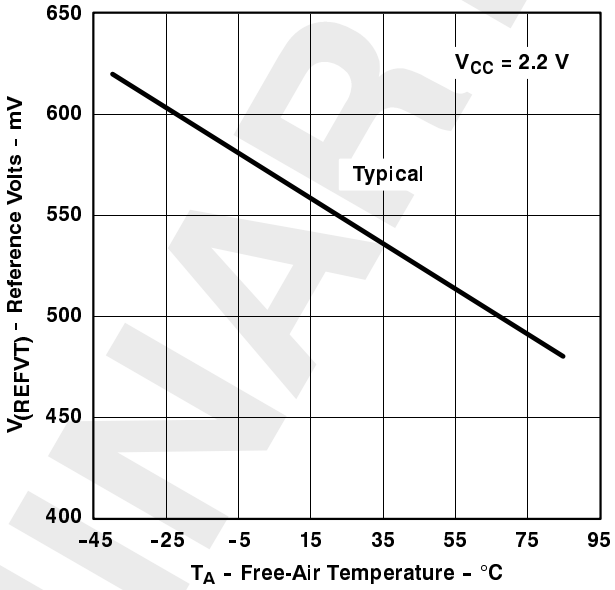


Figure 28. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

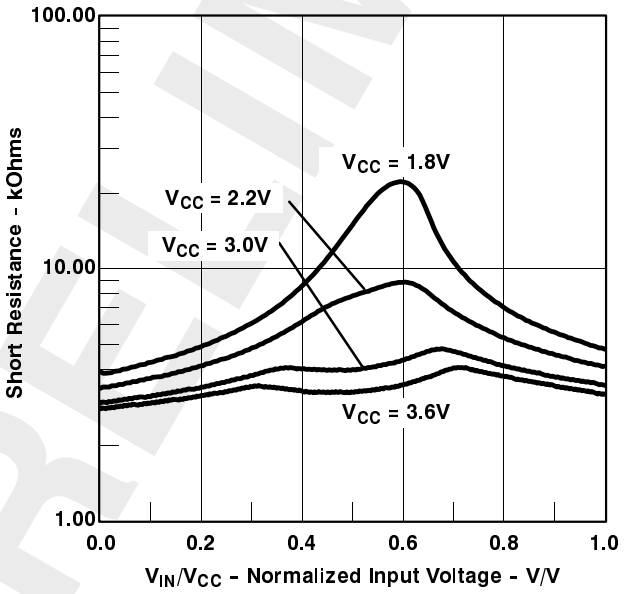


Figure 29. Short Resistance vs V_{IN}/V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	See Note 2			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	See Note 2			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	See Note 2			6		t_{FTG}
$t_{Mass Erase}$	Mass erase time	See Note 2			10593		t_{FTG}
$t_{Seg Erase}$	Segment erase time	See Note 2			4819		t_{FTG}

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note)	CPU halted	1.6			V

NOTE : This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	See Note 2	2.2 V/ 3 V	20	35	55	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

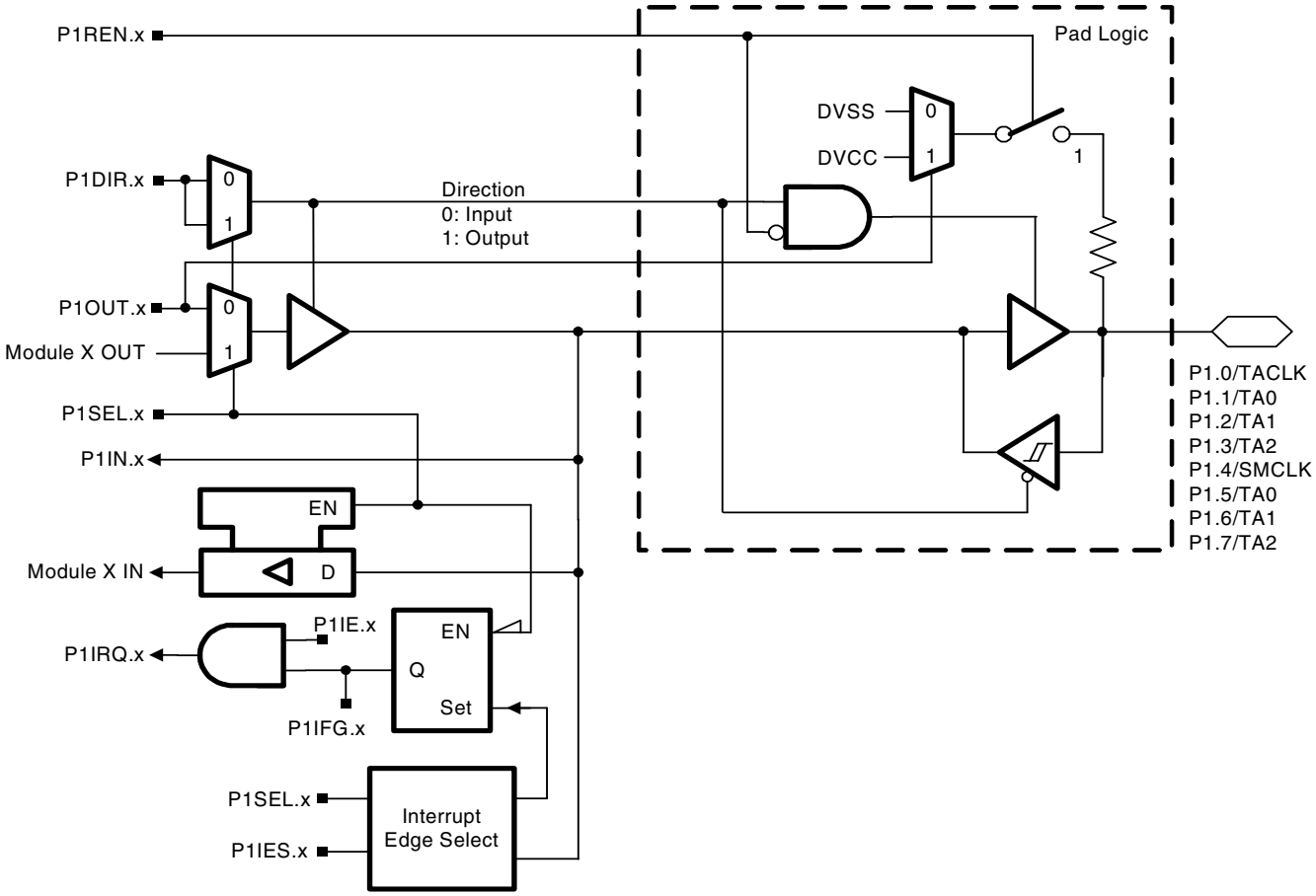
JTAG fuse (see Note)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTE : Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

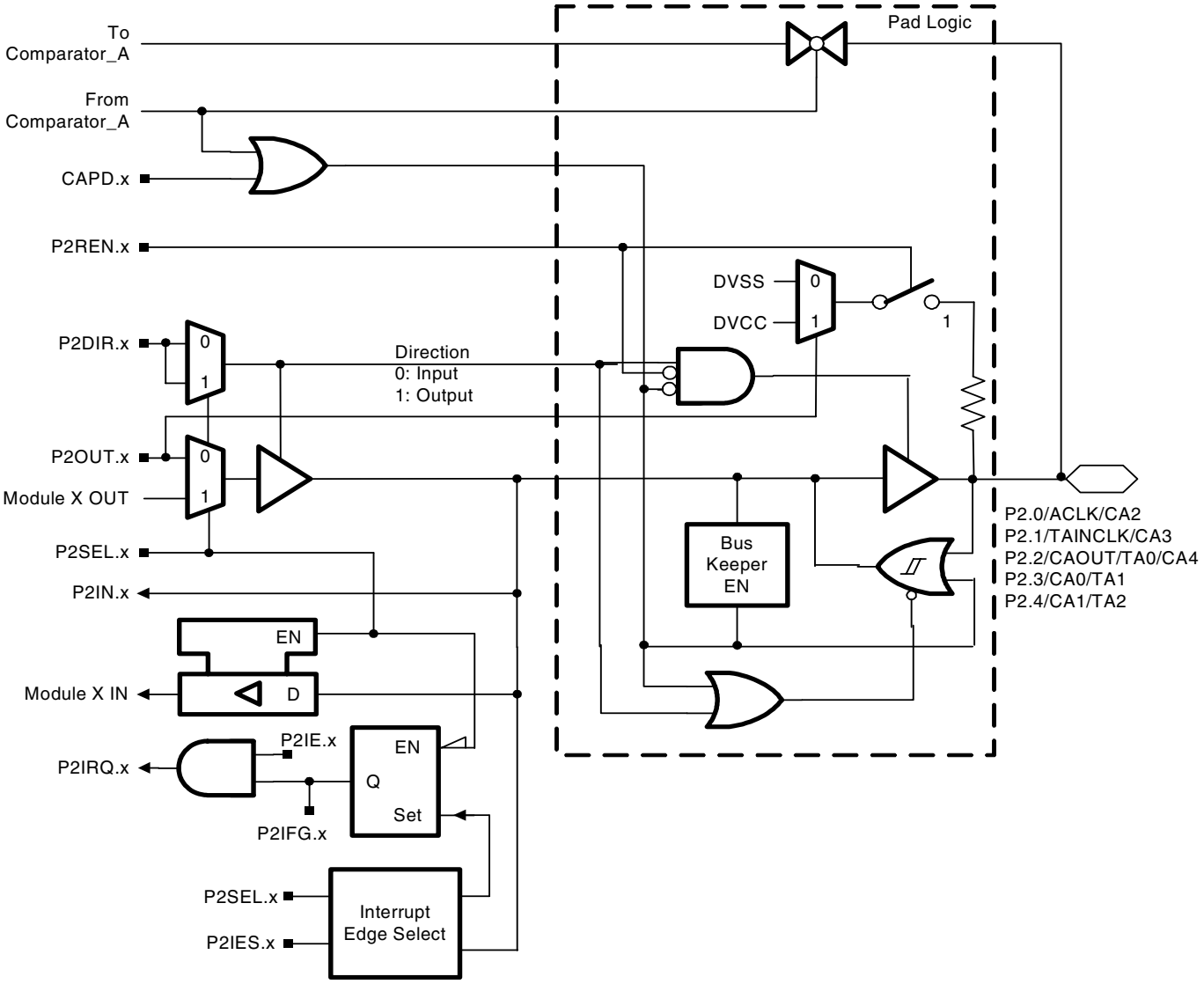
Port P1 pin schematic: P1.0 to P1.7, input/output with Schmitt trigger



Port P1.0 to P1.7 pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK	0	P1.0 (I/O)	I: 0, O: 1	0
		Timer_A3.TACLK	0	1
		DV_{SS}	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0, O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0, O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA2	1	1

Port P2 pin schematic: P2.0 to P2.4, input/output with Schmitt trigger

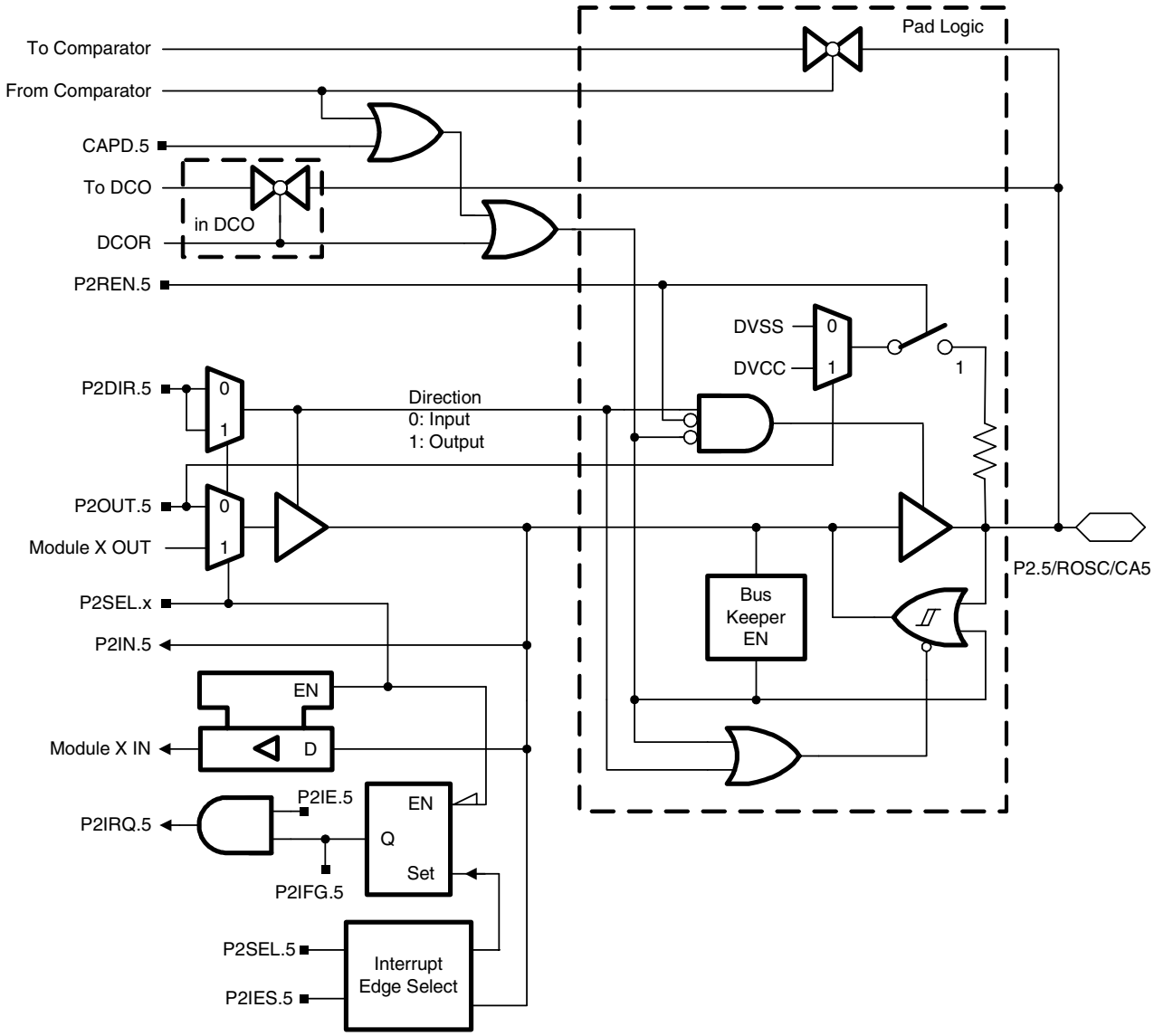


Port P2.0 to P2.4 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0, O: 1	0
		ACLK	0	1	1
		CA2 (see Note 4)	1	X	X
P2.1/TAINCLK/CA3	1	P2.1 (I/O)	0	I: 0, O: 1	0
		Timer_A3.TAINCLK	0	0	1
		DV_{SS}	0	1	1
		CA3 (see Note 4)	1	X	X
P2.2/CAOUT/TA0/ CA4	2	P2.2 (I/O)	0	I: 0, O: 1	0
		CAOUT	0	1	1
		TA0	0	0	1
		CA4 (see Note 4)	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0, O: 1	0
		CA0 (see Note 4)	1	X	X
		Timer_A3.TA1	0	1	1
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0, O: 1	0
		CA1 (see Note 4)	1	X	X
		Timer_A3.TA2	0	1	1

NOTES: 3. X: Don't care.
4. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P2 pin schematic: P2.5, input/output with Schmitt trigger

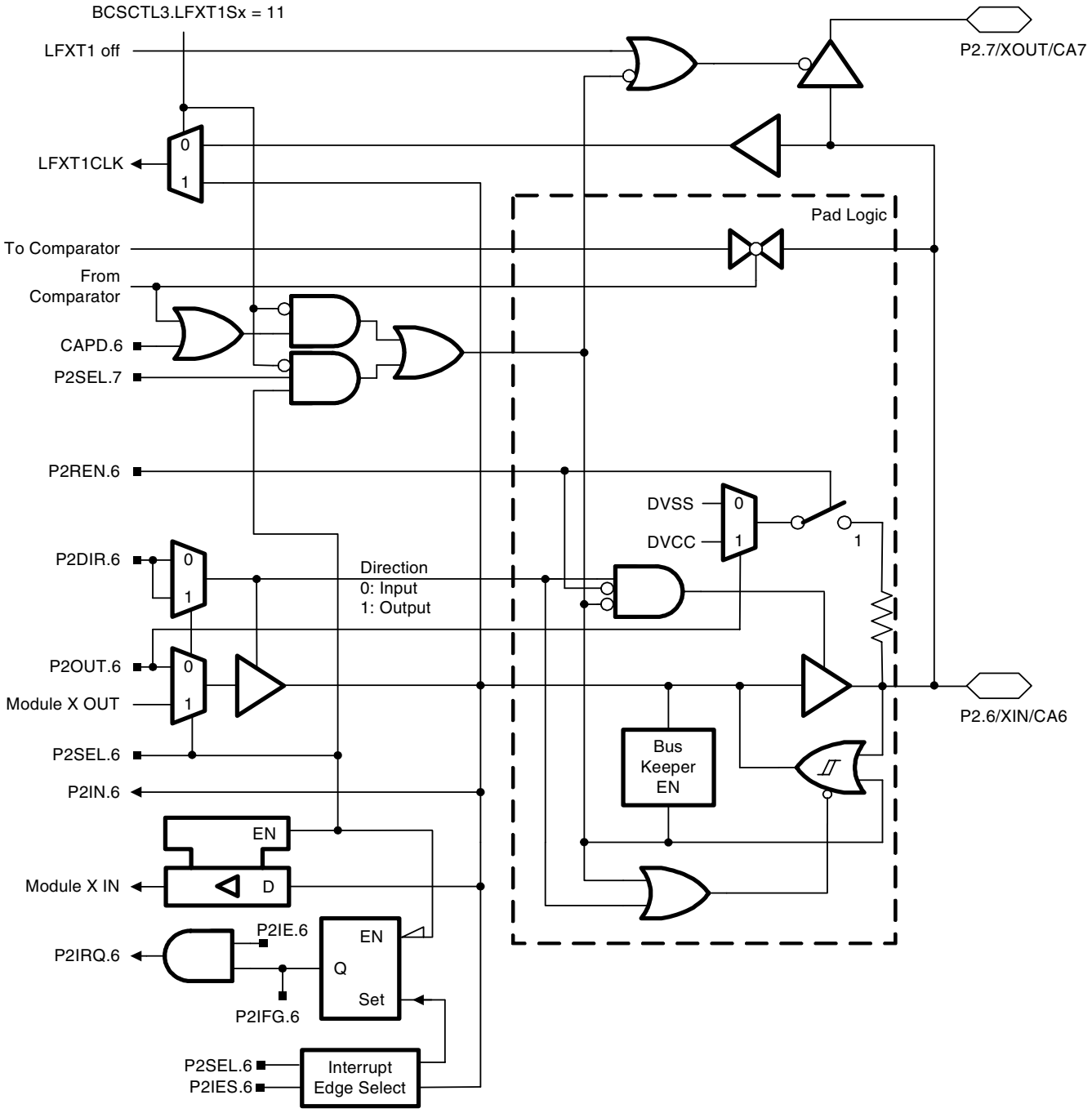


Port P2.5 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.5	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	I: 0, O: 1	0
		R_{OSC}	0	1	X	X
		DV_{SS}	0	0	1	1
		CA5 (see Note 6)	1	0	X	X

NOTES: 5. X: Don't care.
6. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P2 pin schematic: P2.6, input/output with Schmitt trigger

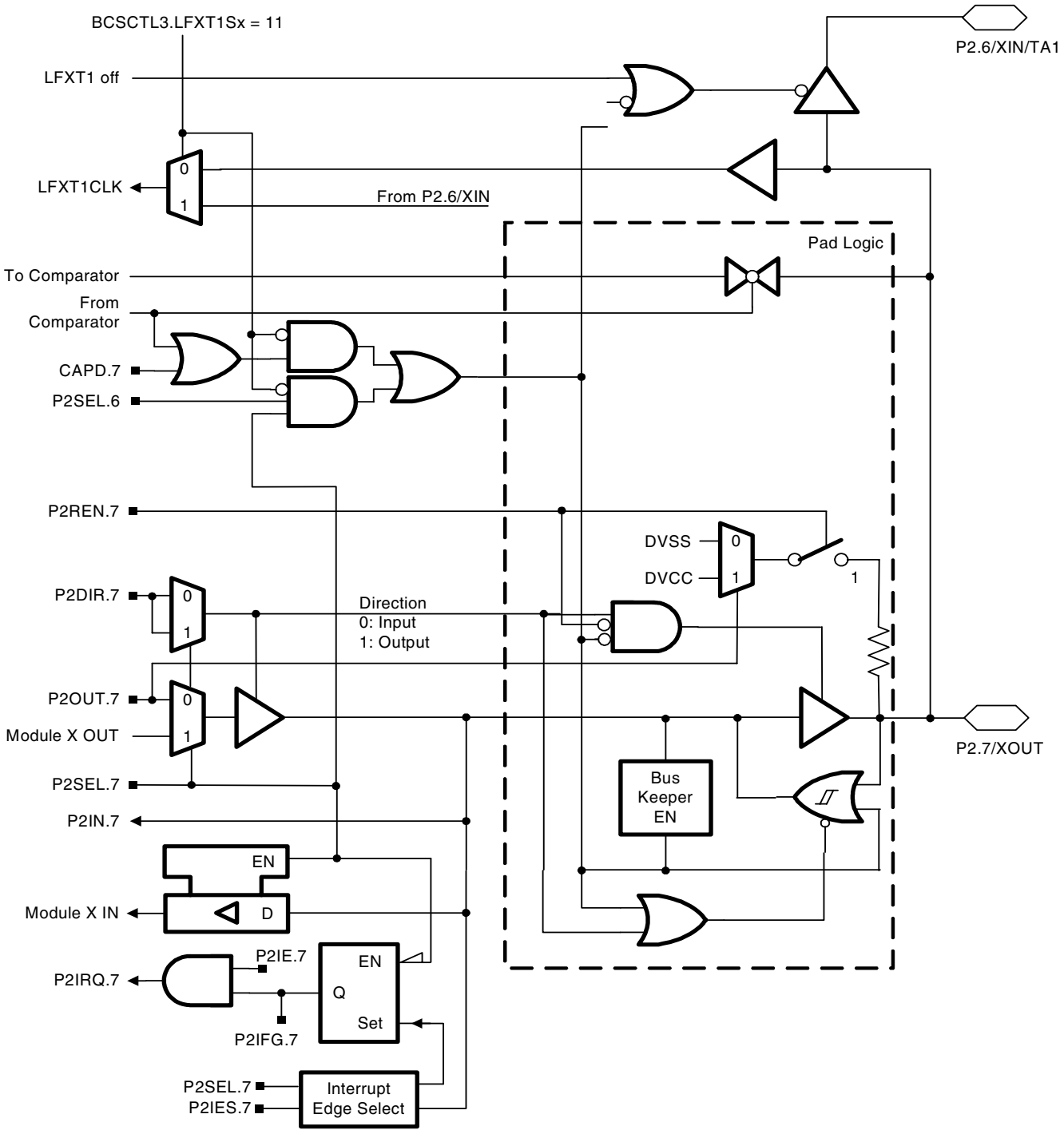


Port P2.6 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.6	P2DIR.6	P2SEL.6
P2.6/XIN/CA6	6	P2.6 (I/O)	0	I: 0, O: 1	0
		XIN (default)	X	1	1
		CA6 (see Note 8)	1	X	0

NOTES: 7. X: Don't care.
8. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P2 pin schematic: P2.7, input/output with Schmitt trigger

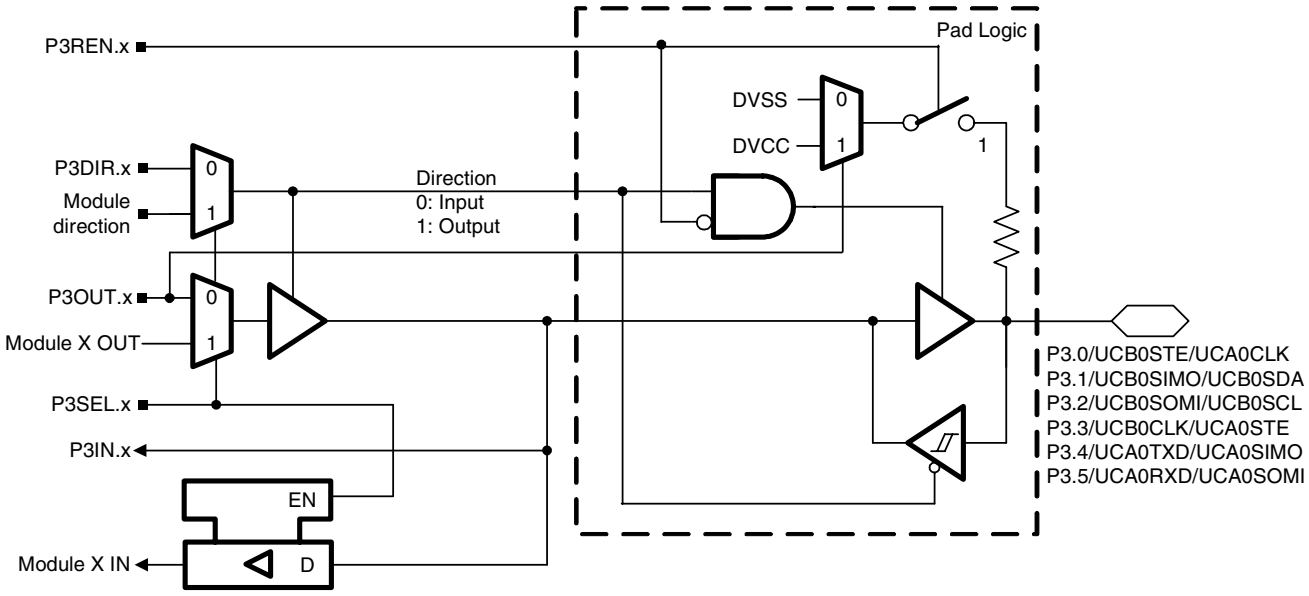


Port P2.7 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.7	P2DIR.7	P2SEL.7
P2.7/XOUT/CA7	7	P2.7 (I/O)	0	I: 0, O: 1	0
		XOUT (default)	X	1	1
		CA7 (see Note 10)	1	X	0

NOTES: 9. X: Don't care.
10. Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P3 pin schematic: P3.0 to P3.5, input/output with Schmitt trigger

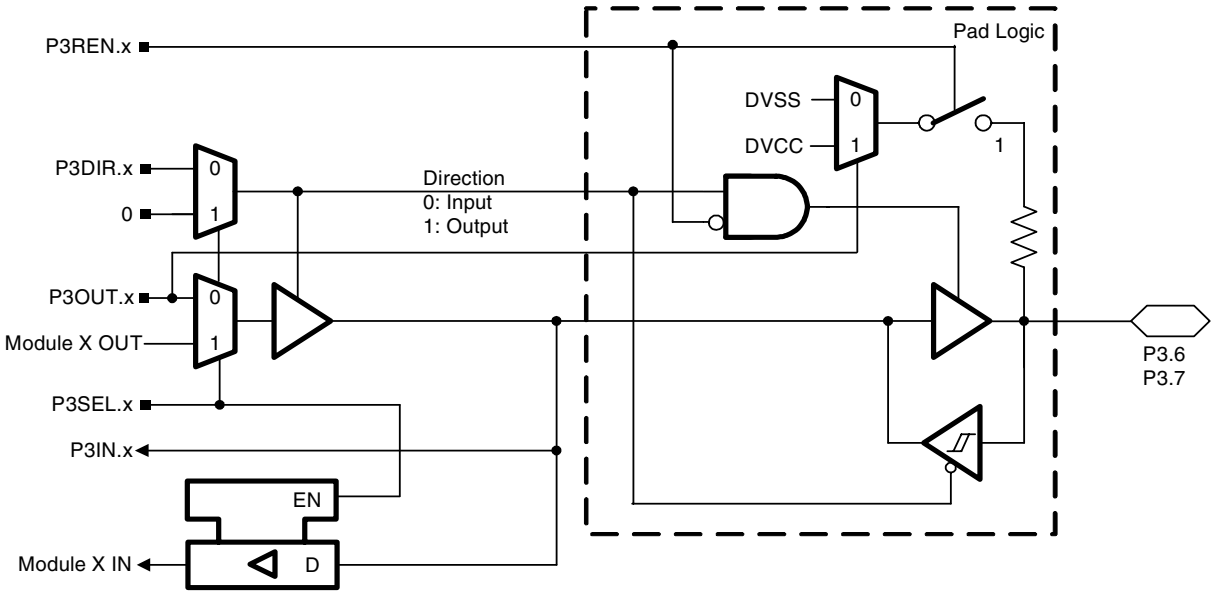


Port P3.0 to P3.5 pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/ UCA0CLK	0	P3.0 (I/O)	I: 0, O: 1	0
		UCB0STE/UCA0CLK (see Notes 1 and 2)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0, O: 1	0
		UCB0SIMO/UCB0SDA (see Notes 1, 2 and 3)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0, O: 1	0
		UCB0SOMI/UCB0SCL (see Notes 1, 2 and 3)	X	1
P3.3/UCB0CLK/ UCA0STE	3	P3.3 (I/O)	I: 0, O: 1	0
		UCB0CLK/UCA0STE (see Notes 1 and 2)	X	1
P3.4/UCA0TXD/ UCA0SIMO	4	P3.4 (I/O)	I: 0, O: 1	0
		UCA0TXD/UCA0SIMO (see Notes 1 and 2)	X	1
P3.5/UCA0RXD/ UCA0SOMI	5	P3.5 (I/O)	I: 0, O: 1	0
		UCA0RXD/UCA0SOMI (see Notes 1 and 2)	X	1

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

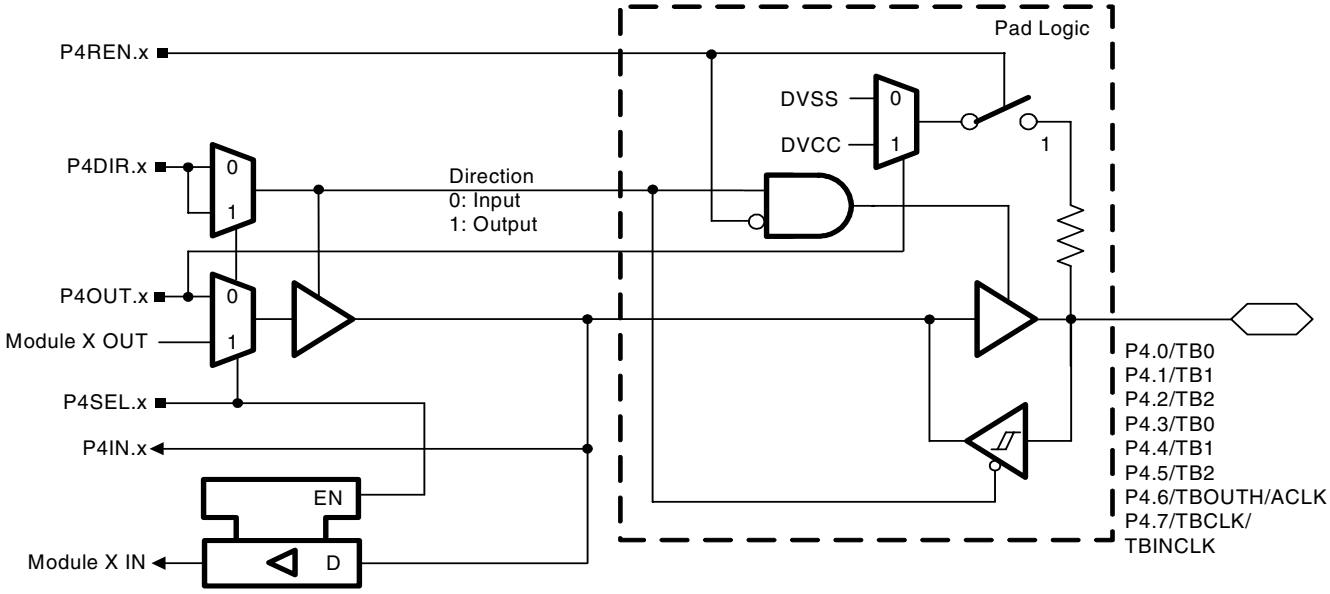
Port P3 pin schematic: P3.6 to P3.7, input/output with Schmitt trigger



Port P3.6 to P3.7 pin functions

PIN NAME (P3.X)	X	FUNCTION	P3DIR.x	P3SEL.x
P3.6	6	P3.6 (I/O)	I: 0, O: 1	0
P3.7	7	P3.7 (I/O)	I: 0, O: 1	0

Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt trigger

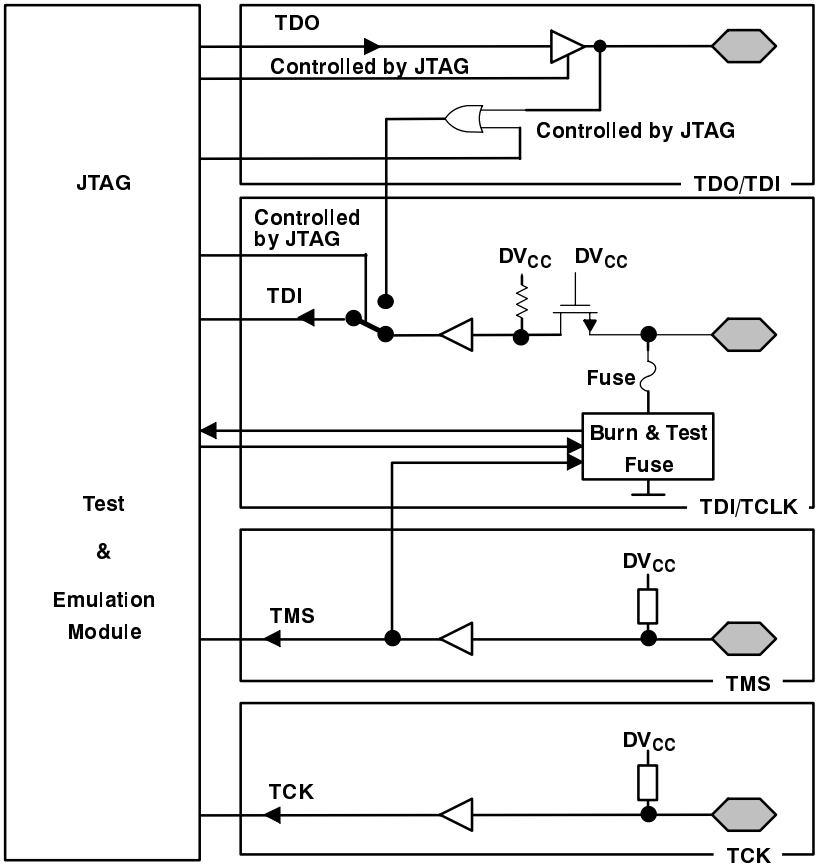


Port P4.0 to P4.7 pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0, O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.OUT0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0, O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.OUT1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0, O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.OUT2	1	1
P4.3/TB0	3	P4.3 (I/O)	I: 0, O: 1	0
		Timer_B3.CCI0B	0	1
		Timer_B3.OUT0	1	1
P4.4/TB1	4	P4.4 (I/O)	I: 0, O: 1	0
		Timer_B3.CCI1B	0	1
		Timer_B3.OUT1	1	1
P4.5/TB2	5	P4.5 (I/O)	I: 0, O: 1	0
		N/A	0	1
		Timer_B3.OUT2	1	1
P4.6/TBOUTH/ACLK	6	P4.6 (I/O)	I: 0, O: 1	0
		Timer_B3.TBOUTH	0	1
		ACLK	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0, O: 1	0
		Timer_B3.TBCLK	0	1

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

APPLICATION INFORMATION

JTAG fuse check mode

MSP430F23x0 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 30). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

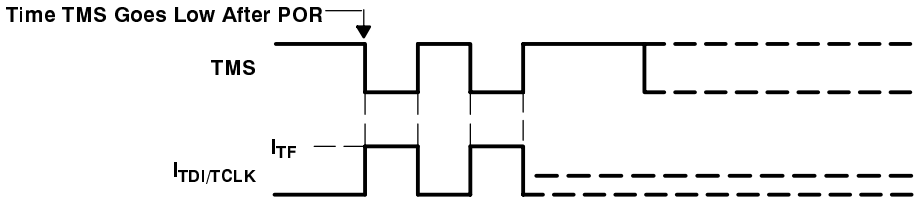


Figure 30. Fuse Check Mode Current

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS518	PRODUCT PREVIEW data sheet release
SLAS518A	PRODUCTION DATA data sheet release
SLAS518B	The USCI parameter section was revised, pages 36 to 39. Corrected the port schematics of port P2.6 and P2.7 Added in the DSBGA package version. Corrected WDTIFG description in IFG1 register. Corrected labels in Figure 17 and 18. Corrected test conditions of Comparator_A+ from P1.0, P1.1 to P2.3 and P2.4. Corrected the UART parameters.
SLAS518C	Release of MSP430F2330IYFF and MSP430F2350IYFF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2330IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2330IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2330IYFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2330IYFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2330TRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2330TRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2350IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2350IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2350IYFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2350IYFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2350TRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2350TRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2370IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2370IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2370IYFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2370IYFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
MSP430F2370TRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2370TRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

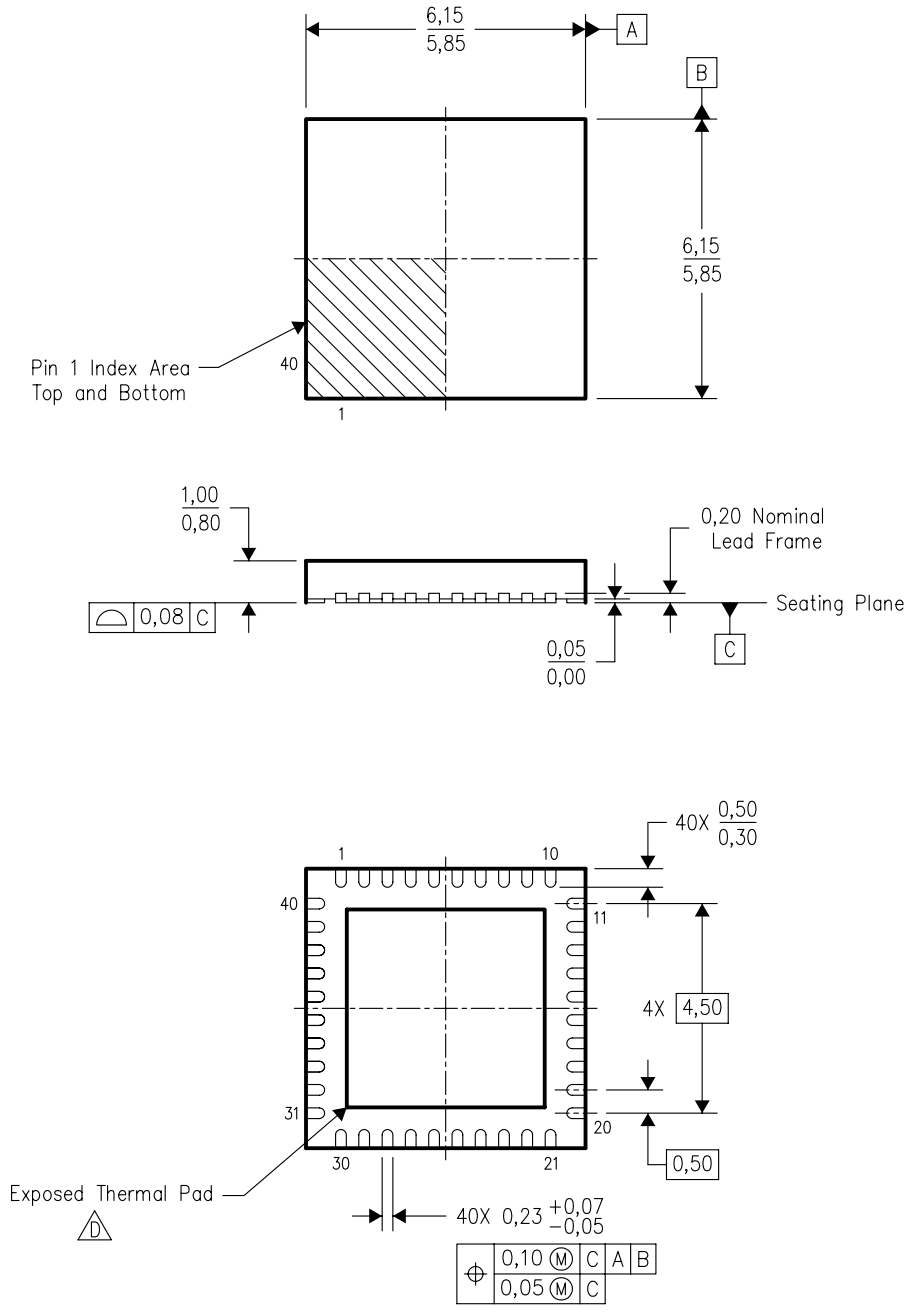
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RHA (S–PQFP–N40) PLASTIC QUAD FLATPACK



Bottom View

4204276/C 12/2004

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation VJJD–2.

THERMAL PAD MECHANICAL DATA

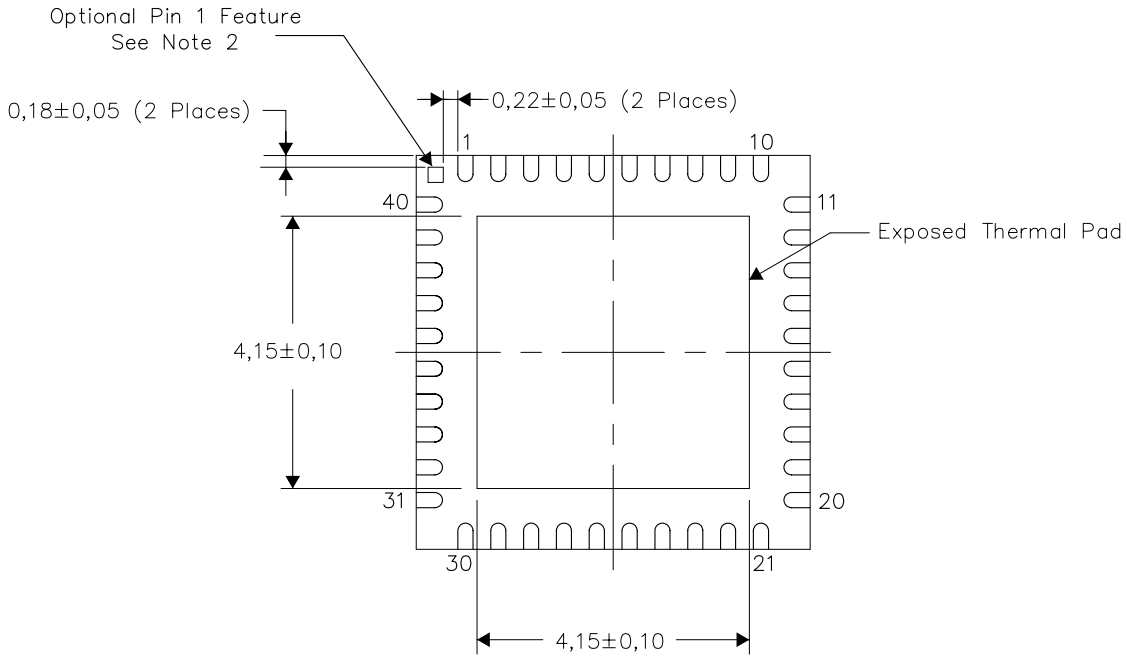
RHA (S–PVQFN–N40)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

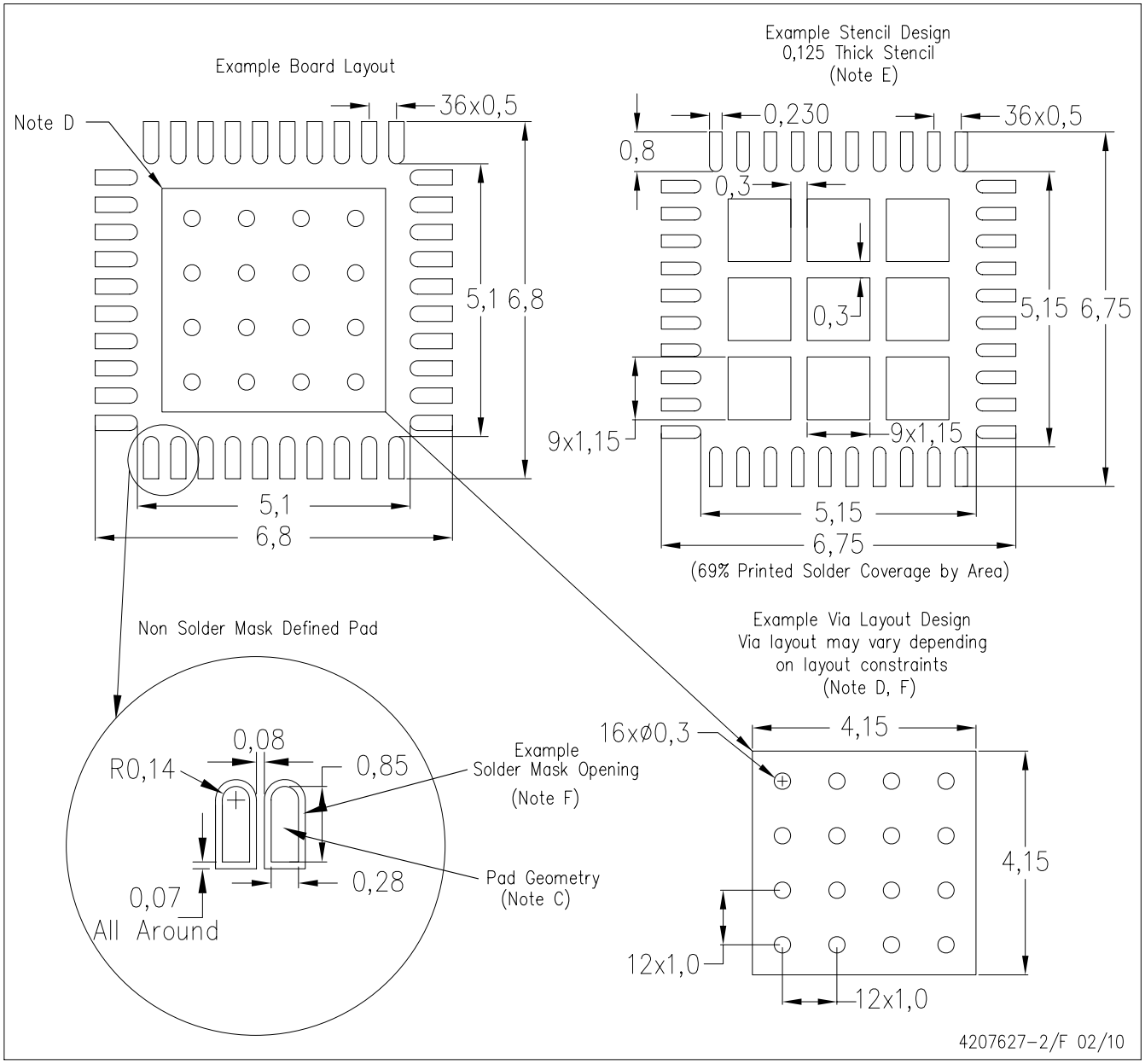


Bottom View

NOTES:
1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

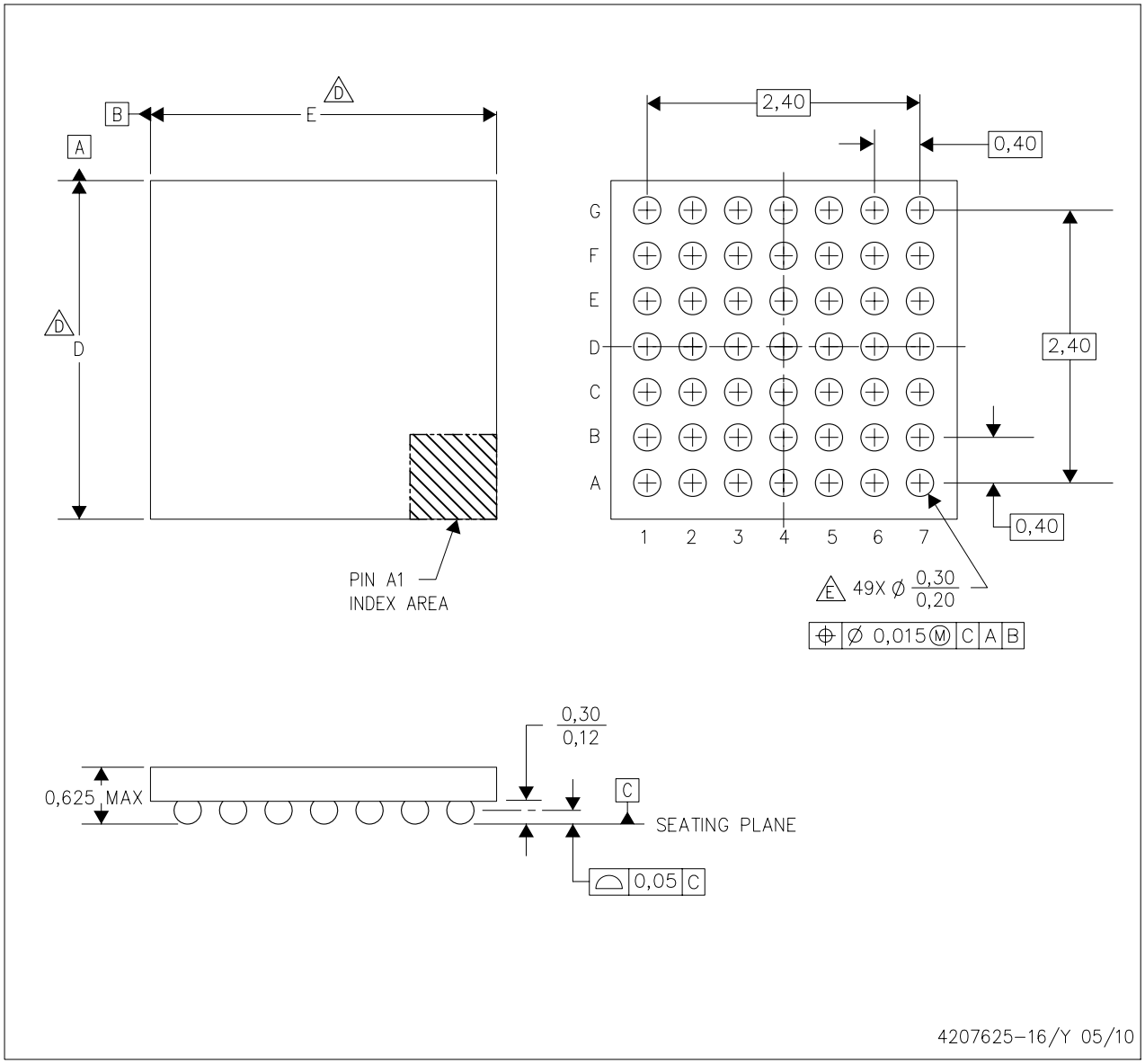
Exposed Thermal Pad Dimensions

RHA (S–PVQFN–N40)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YFF package can have dimension D ranging from 2.73 to 3.45 mm and dimension E ranging from 2.73 to 3.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 7 x 7 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.

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