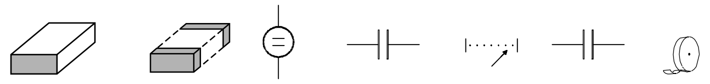
Multilayer ceramic capacitors

Chip capacitors, HighCV, X7R

Date: October 2006

Ordering code system



B37941 K 5 105 K 0 62

Packaging

60 ≙ cardboard tape, 180-mm reel
62 ≙ blister tape, 180-mm reel
70 ≙ cardboard tape, 360-mm reel
72 ≙ blister tape, 360-mm reel

Internal coding

Capacitance tolerance

K ≙ ±10% (standard)

Capacitance, coded (example)

474 ≙ 47 · 10^4 pF = 470 nF
105 ≙ 10 · 10^5 pF = 1 µF

Rated voltage

Rated voltage [VDC]	16	25	50
Code	9	0	5

Termination Standard: K ≙ nickel barrier for all case sizes

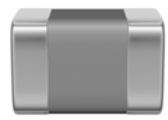
Type and size

Chip size (**inch** / mm)	Temperature characteristic X7R
0603 / 1608	B37931
0805 / 2012	B37941
1206 / 3216	B37872

Multilayer ceramic capacitors **Chip**

HighCV; X7R

Features



- Characteristic of class 2 dielectric
- Highest possible capacitance to rated voltage ratio
- High capacitance values up to 2.2 µF
- Voltage rating from 16 V to 50 V
- To AEC-Q200

Applications

- Coupling and bypass filters

Termination

- For soldering: Nickel barrier terminations (Ni)

Options

- Other capacitance values on request

Delivery mode

- Cardboard and blister tape (blister tape for chip thickness ≥1.2 ±0.1 mm)

Electrical data

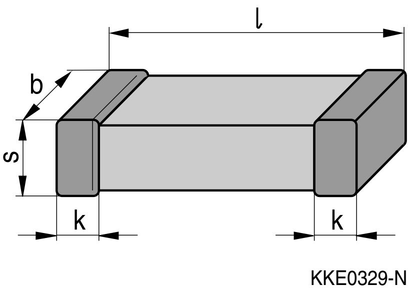
Temperature characteristic		X7R	
Max. relative capacitance change within –55 °C to +125 °C	ΔC/C	±15	%
Climatic category (IEC 60068-1)		55/125/56	
Standard		EIA	
Dielectric		Class 2	
Rated voltage[1)]	V_R	16; 25; 50	VDC
Test voltage	V_{test}	$2.5 \cdot V_R$/5 s	VDC
Capacitance range	C_R	100 nF … 2.2 µF	
Dissipation factor (limit value)	tan δ	$<50 \cdot 10^{-3}$ for ≤25 V $<25 \cdot 10^{-3}$ for 50 V	
Insulation resistance[2)] at +25 °C	R_{ins}	$>10^4$	MΩ
Time constant[2)] at +25 °C	τ	>500	s
Operating temperature range	T_{op}	–55 … +125	°C
Ageing[3)]		yes	

1) Note: No operation on AC line.
2) For C_R >10 nF the time constant $\tau = C \cdot R_{ins}$ is given.
3) Refer to chapter “General technical information”, “Ageing”.

Capacitance tolerances

Code letter	K (standard)
Tolerance	±10%

Dimensional drawing

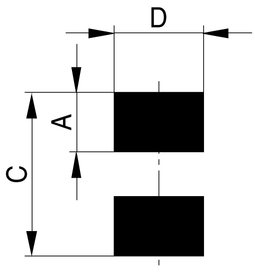


Dimensions (mm)

Case size (inch) (mm)	0603 1608	0805 2012	1206 3216
l	1.6 ±0.15	2.00 ±0.20	3.2 ±0.20
b	0.8 ±0.10	1.25 ±0.15	1.6 ±0.15
s	0.8 ±0.10	1.35 max.	1.80 max.
k	0.1 –0.4	0.13 –0.75	0.25 –0.75

Tolerances to CECC 32101-801

Recommended solder pad



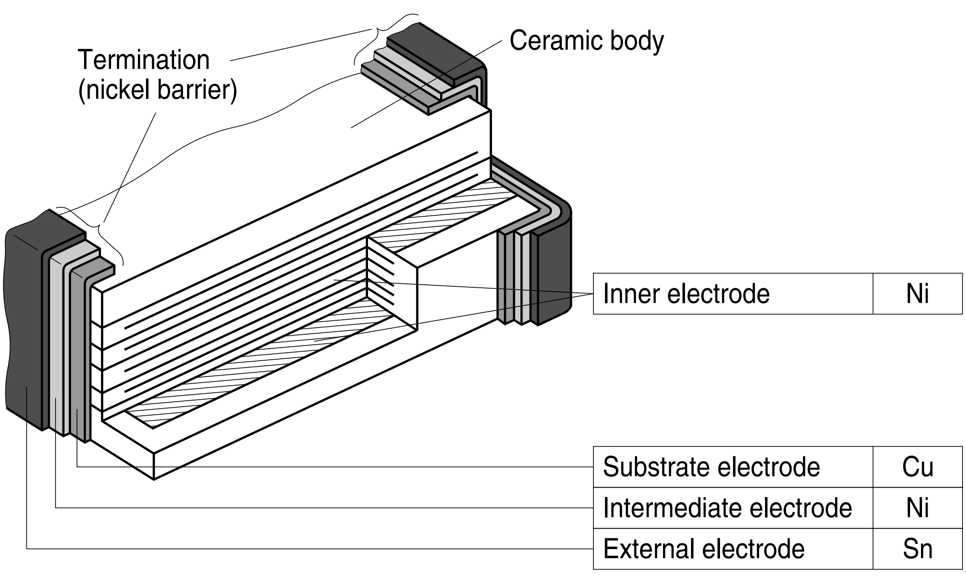
Recommended dimensions (mm) for reflow soldering

Case size (inch/mm)	Type	A	C	D
0603/1608	single chip	0.6 … 0.7	1.8 … 2.20	0.6 … 0.8
0805/2012	single chip	0.6 … 0.7	2.2 … 2.60	0.8 … 1.1
1206/3216	single chip	0.8 … 0.9	3.8 … 4.32	1.0 … 1.4

Recommended dimensions (mm) for wave soldering

Case size (inch/mm)	Type	A	C	D
0603/1608	single chip	0.8 … 0.9	2.2 … 2.8	0.6 … 0.8
0805/2012	single chip	0.9 … 1.0	2.8 … 3.2	0.8 … 1.1
1206/3216	single chip	1.0 … 1.1	4.2 … 4.8	1.0 … 1.4

Termination



Product range for HighCV chip capacitors, X7R

Size[1)] inch / mm	0603 / 1608			0805 / 2012			1206 / 3216		
Type	B37931			B37941			B37872		
C_R \ V_R (VDC)	16	25	50	16	25	50	16	25	50
100 nF			■						
220 nF	■	■		■	■	■			
330 nF				■	■	■			
470 nF				■	■	■			
1.0 µF				■	■	■	■	■	■
2.2 µF							■	■	

1) l × b (inch) / l × b (mm)

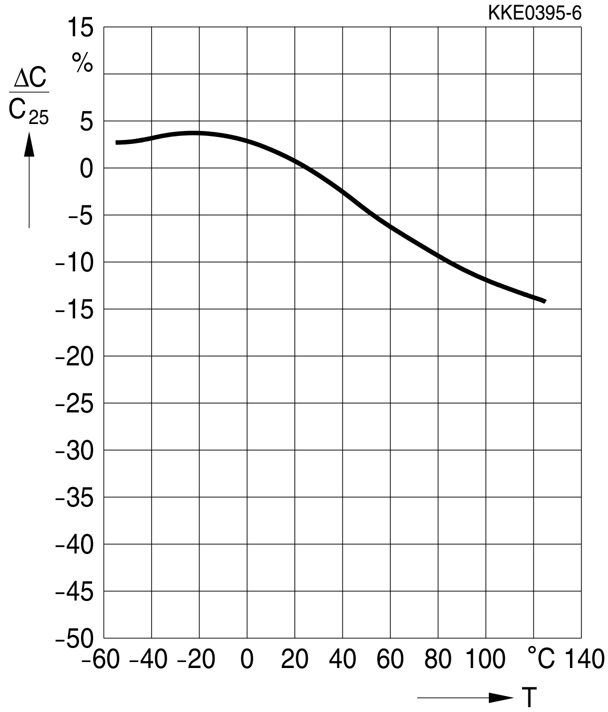
Ordering codes and packing for HighCV, X7R, 16, 25 and 50 VDC, nickel barrier terminations

C_R[1)]	Ordering code	Chip thickness mm	Cardboard tape, ∅ 180-mm reel ** ≙ 60 pcs/reel	Cardboard tape, ∅ 360-mm reel ** ≙ 70 pcs/reel
Case size 0603, 16 VDC				
220 nF	B37931K9224K0**	0.8 ±0.1	4000	16000
Case size 0603, 25 VDC				
220 nF	B37931K0224K0**	0.8 ±0.1	4000	16000
Case size 0603, 50 VDC				
100 nF	B37931K5104K0**	0.8 ±0.1	4000	16000
Case size 0805, 16 VDC				
220 nF	B37941K9224K0**	0.8 ±0.1	4000	16000
330 nF	B37941K9334K0**	0.8 ±0.1	4000	16000
470 nF	B37941K9474K0**	0.8 ±0.1	4000	16000
1.0 µF	B37941K9105K0**	1.2 ±0.1	3000[2)]	12000[3)]
Case size 0805, 25 VDC				
220 nF	B37941K0224K0**	0.8 ±0.1	4000	16000
330 nF	B37941K0334K0**	0.8 ±0.1	4000	16000
470 nF	B37941K0474K0**	0.8 ±0.1	4000	16000
1.0 µF	B37941K0105K0**	1.2 ±0.1	3000[2)]	12000[3)]
Case size 0805, 50 VDC				
220 nF	B37941K5224K0**	0.8 ±0.1	4000	16000
330 nF	B37941K5334K0**	1.2 ±0.1	3000[2)]	12000[3)]
470 nF	B37941K5474K0**	1.2 ±0.1	3000[2)]	12000[3)]
1.0 µF	B37941K5105K0**	1.2 ±0.1	3000[2)]	12000[3)]
Case size 1206, 16 VDC				
1.0 µF	B37872K9105K0**	1.2 ±0.1	3000[2)]	12000[3)]
2.2 µF	B37872K9225K0**	1.2 ±0.1	3000[2)]	12000[3)]
Case size 1206, 25 VDC				
1.0 µF	B37872K0105K0**	1.2 ±0.1	3000[2)]	12000[3)]
2.2 µF	B37872K0225K0**	1.2 ±0.1	3000[2)]	12000[3)]
Case size 1206, 50 VDC				
1.0 µF	B37872K5105K0**	1.2 ±0.1	3000[2)]	12000[3)]

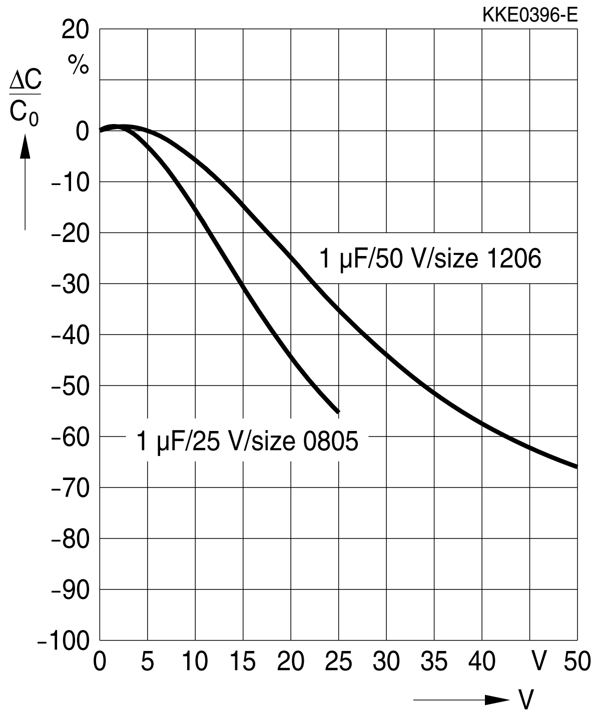
1) Other capacitance values on request.
2) Blister tape, 180-mm reel, ordering code ** ≙ 62
3) Blister tape, 330-mm reel, ordering code ** ≙ 72

Typical characteristics for HighCV X7R[1)]

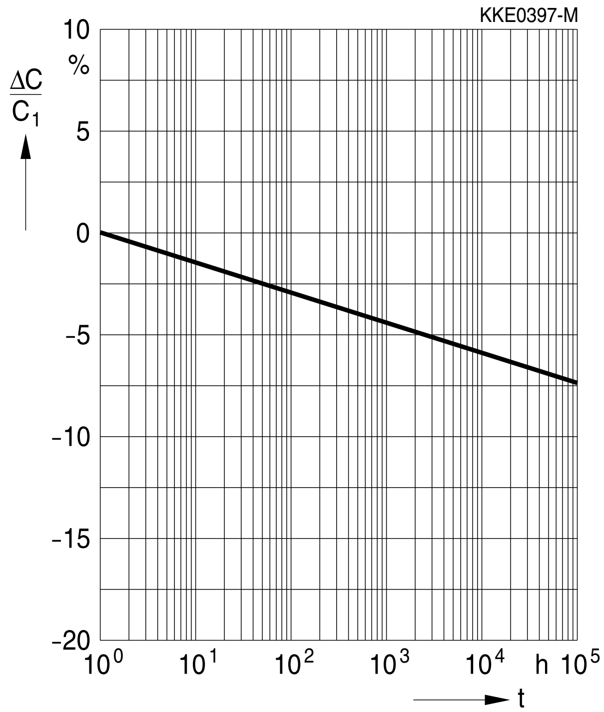
Capacitance change $\Delta C/C_{25}$ versus temperature T



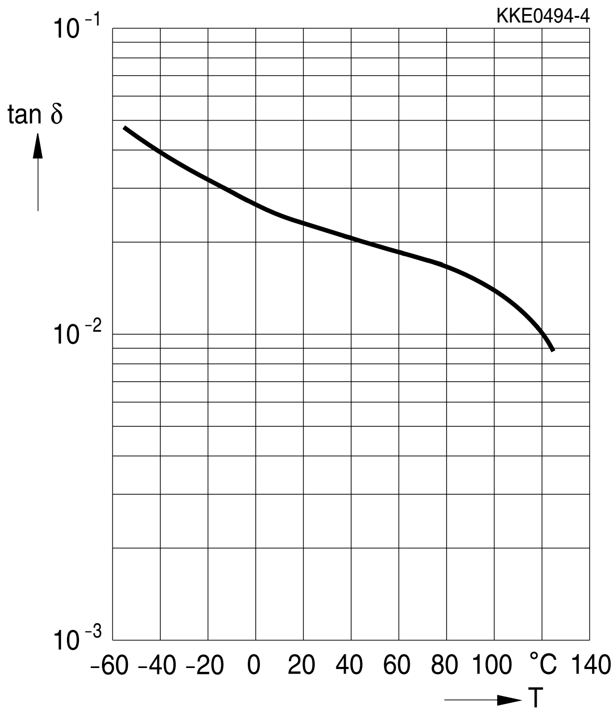
Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



Capacitance change $\Delta C/C_1$ versus time t



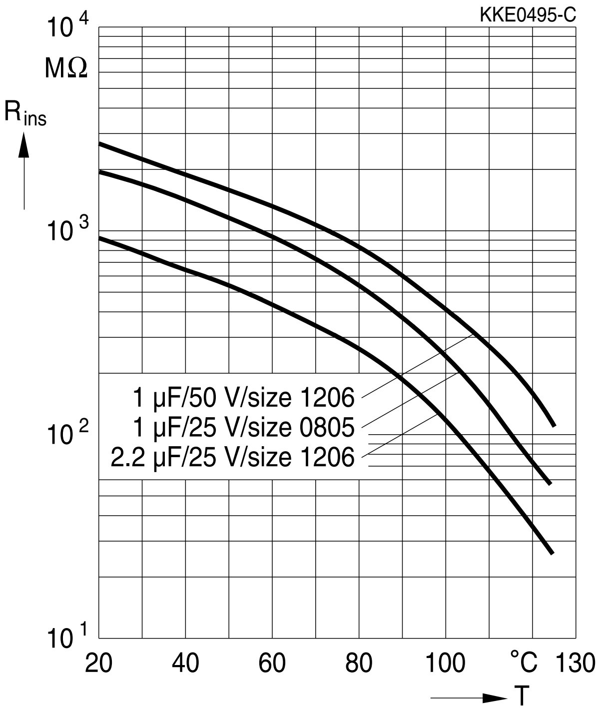
Dissipation factor $\tan \delta$ versus temperature T



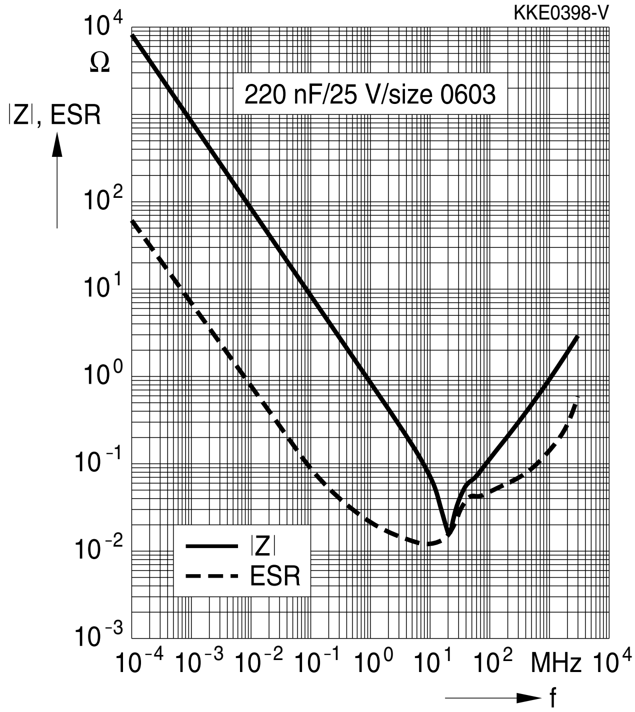
1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Typical characteristics for HighCV X7R[1)]

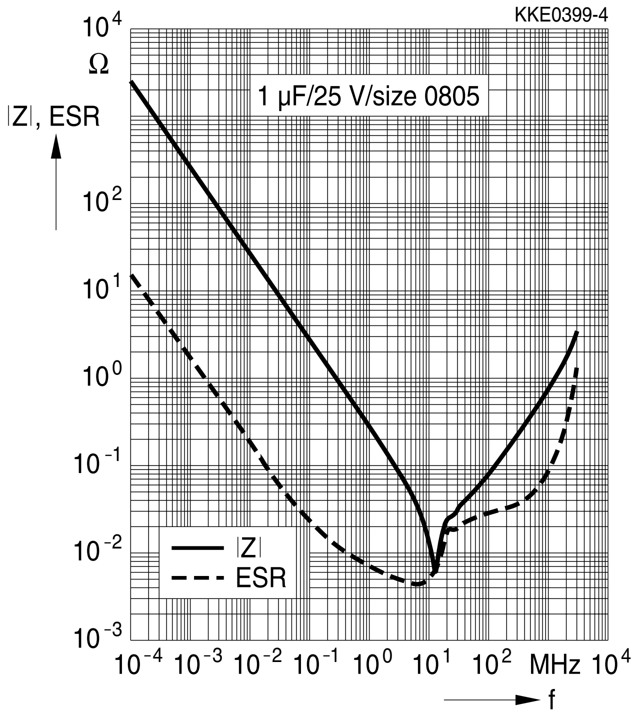
Insulation resistance R_{ins} versus temperature T



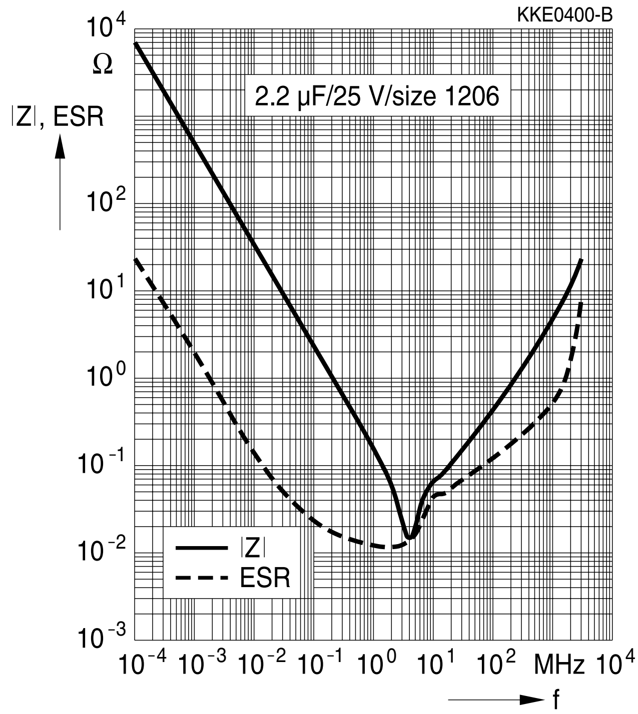
Impedance |Z| and ESR versus frequency f



Impedance |Z| and ESR versus frequency f



Impedance |Z| and ESR versus frequency f



1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

1. Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter “Reliability”).

The following should be considered in circuit board design

1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
2. At least FR4 circuit board material should be used.
3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).

The following should be considered in the placement process

1. Ensure correct positioning of the ceramic capacitor on the solder pad.
2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
3. Support the circuit board and reduce the placement forces.
4. A board should not be straightened (manually) if it has been distorted by soldering.
5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter “Soldering directions”).
10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
11. Ensure the correct solder meniscus height and solder quantity.
12. Ensure correct dosing of the cement quantity.
13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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