

## 32Kx8 Nonvolatile SRAM

### Features

- ▶ Data retention in the absence of power
- ▶ Automatic write-protection during power-up/power-down cycles
- ▶ Industry-standard 28-pin 32K x 8 pinout
- ▶ Conventional SRAM operation; unlimited write cycles
- ▶ 10-year minimum data retention in absence of power
- ▶ Battery internally isolated until power is applied

### General Description

The CMOS bq4011 is a nonvolatile 262,144-bit static RAM organized as 32,768 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

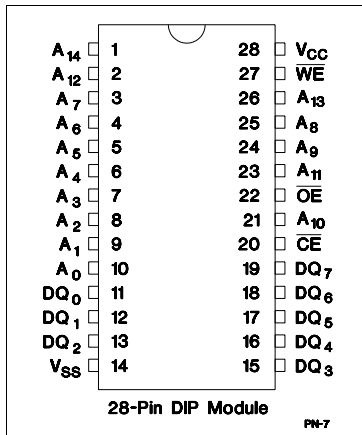
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V<sub>CC</sub> falls out of tolerance, the SRAM is unconditionally write-protected to prevent inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V<sub>CC</sub> returns valid.

The bq4011 uses an extremely low standby current CMOS SRAM, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4011 requires no external circuitry and is socket-compatible with industry-standard SRAMs and most EPROMs and EEPROMs.

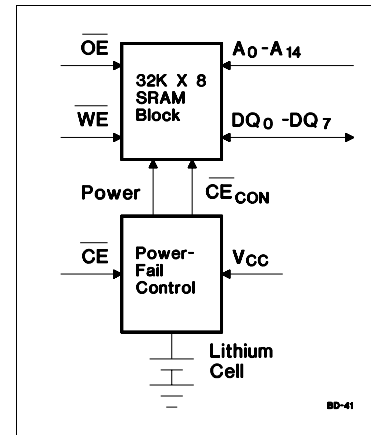
### Pin Connections



### Pin Names

- A<sub>0</sub>–A<sub>14</sub> Address inputs
- DQ<sub>0</sub>–DQ<sub>7</sub> Data input/output
- $\overline{\text{CE}}$  Chip enable input
- $\overline{\text{OE}}$  Output enable input
- $\overline{\text{WE}}$  Write enable input
- V<sub>CC</sub> +5 volt supply input
- V<sub>SS</sub> Ground

### Block Diagram



### Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
			bq4011Y-70	70	-10%
bq4011 -100	100	-5%	bq4011Y -100	100	-10%
bq4011 -150	150	-5%	bq4011Y -150	150	-10%
bq4011 -200	200	-5%	bq4011Y -200	200	-10%

# bq4011/bq4011Y

## Functional Description

When power is valid, the bq4011 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4011 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the  $V_{CC}$  supply for a power-fail-detect threshold  $V_{PFD}$ . The bq4011 monitors for  $V_{PFD} = 4.62V$  typical for use in systems with 5% supply tolerance. The bq4011Y monitors for  $V_{PFD} = 4.37V$  typical for use in systems with 10% supply tolerance.

When  $V_{CC}$  falls below the  $V_{PFD}$  threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time  $t_{WPT}$ , write-protection takes place.

As  $V_{CC}$  falls past  $V_{PFD}$  and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid  $V_{CC}$  is applied.

When  $V_{CC}$  returns to a level above the internal backup cell voltage, the supply is switched back to  $V_{CC}$ . After  $V_{CC}$  ramps above the  $V_{PFD}$  threshold, write-protection continues for a time  $t_{CER}$  (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cell used by the bq4011 has an extremely long shelf life and provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cell is electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of  $V_{CC}$ , this isolation is broken, and the lithium backup cell provides data retention on subsequent power-downs.

## Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	X	D <sub>IN</sub>	Active

## Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
$V_{CC}$	DC voltage applied on $V_{CC}$ relative to $V_{SS}$	-0.3 to 7.0	V	
$V_T$	DC voltage applied on any pin excluding $V_{CC}$ relative to $V_{SS}$	-0.3 to 7.0	V	$V_T \leq V_{CC} + 0.3$
$T_{OPR}$	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
$T_{STG}$	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
$T_{BIAS}$	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
$T_{SOLDER}$	Soldering temperature	+260	°C	For 10 seconds

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Aug. 1993 C

**Recommended DC Operating Conditions** ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V	bq4011Y/bq4011Y-xxxN
		4.75	5.0	5.5	V	bq4011
V <sub>SS</sub>	Supply voltage	0	0	0	V	
V <sub>IL</sub>	Input low voltage	-0.3	-	0.8	V	
V <sub>IH</sub>	Input high voltage	2.2	-	V <sub>CC</sub> + 0.3	V	

**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ .

**DC Electrical Characteristics** ( $T_A = T_{OPR}$ ,  $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I <sub>LI</sub>	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to $V_{CC}$
I <sub>LO</sub>	Output leakage current	-	-	± 1	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V <sub>OH</sub>	Output high voltage	2.4	-	-	V	$I_{OH} = -1.0$ mA
V <sub>OL</sub>	Output low voltage	-	-	0.4	V	$I_{OL} = 2.1$ mA
I <sub>SB1</sub>	Standby supply current	-	4	7	mA	$\overline{CE} = V_{IH}$
I <sub>SB2</sub>	Standby supply current	-	2.5	4	mA	$\overline{CE} \geq V_{CC} - 0.2V$ , $0V \leq V_{IN} \leq 0.2V$ , or $V_{IN} \geq V_{CC} - 0.2V$
I <sub>CC</sub>	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$ , $I_{I/O} = 0$ mA
V <sub>PF<sub>D</sub></sub>	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4011
		4.30	4.37	4.50	V	bq4011Y
V <sub>SO</sub>	Supply switch-over voltage	-	3	-	V	

**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5V$ .

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $F = 1\text{MHz}$ ,  $V_{CC} = 5.0V$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C <sub>I/O</sub>	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C <sub>IN</sub>	Input capacitance	-	-	10	pF	Input voltage = 0V

**Note:** These parameters are sampled and not 100% tested.

# bq4011/bq4011Y

## AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

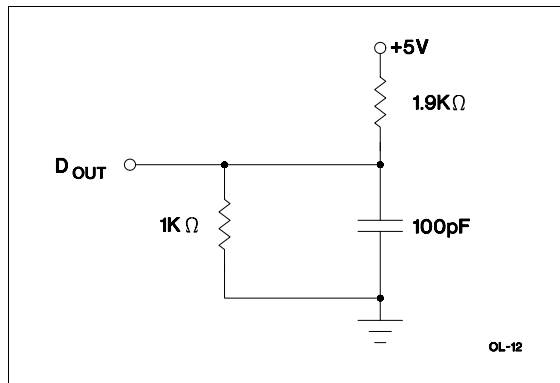


Figure 1. Output Load A

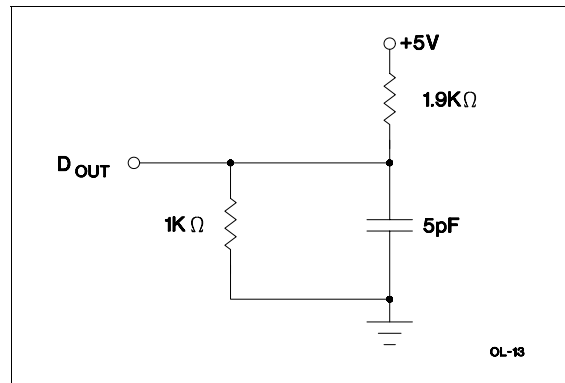


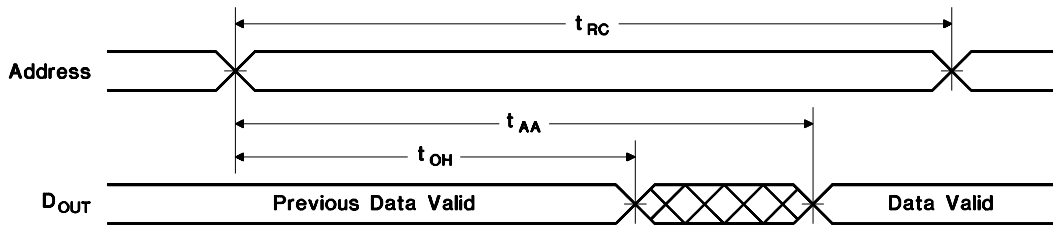
Figure 2. Output Load B

## Read Cycle ( $T_A = T_{OPR}$ , $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read cycle time	70	-	100	-	150	-	200	-	ns	
t <sub>AA</sub>	Address access time	-	70	-	100	-	150	-	200	ns	Output load A
t <sub>ACE</sub>	Chip enable access time	-	70	-	100	-	150	-	200	ns	Output load A
t <sub>OE</sub>	Output enable to output valid	-	35	-	50	-	70	-	90	ns	Output load A
t <sub>CLZ</sub>	Chip enable to output in low Z	5	-	5	-	10	-	10	-	ns	Output load B
t <sub>OLZ</sub>	Output enable to output in low Z	5	-	5	-	5	-	5	-	ns	Output load B
t <sub>CHZ</sub>	Chip disable to output in high Z	0	25	0	40	0	60	0	70	ns	Output load B
t <sub>OHZ</sub>	Output disable to output in high Z	0	25	0	35	0	50	0	70	ns	Output load B
t <sub>OH</sub>	Output hold from address change	10	-	10	-	10	-	10	-	ns	Output load A

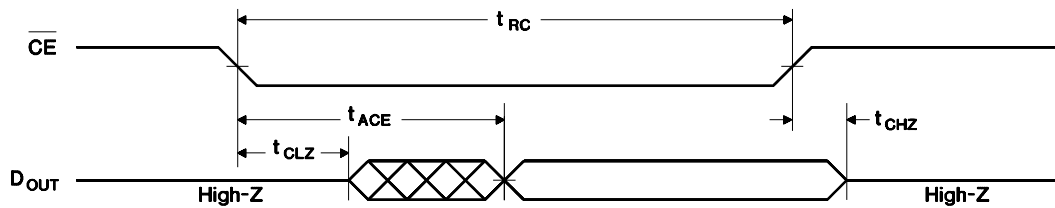
Aug. 1993 C

Read Cycle No. 1 (Address Access) <sup>1,2</sup>



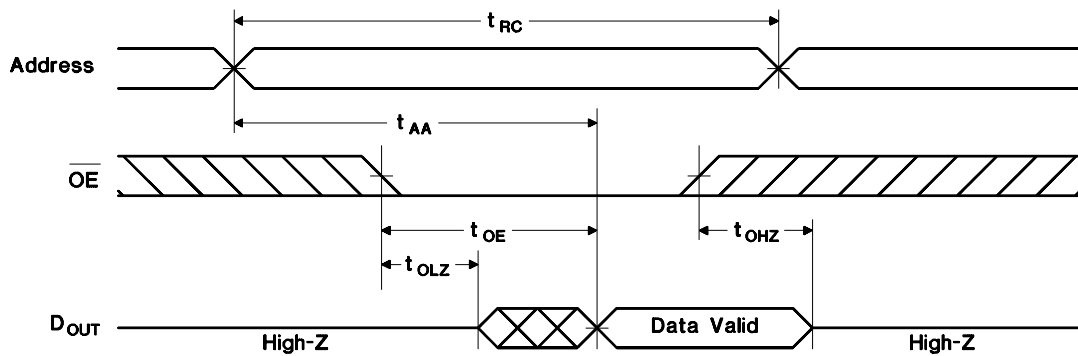
RC-1

Read Cycle No. 2 ( $\overline{\text{CE}}$  Access) <sup>1,3,4</sup>



RC-2

Read Cycle No. 3 ( $\overline{\text{OE}}$  Access) <sup>1,5</sup>



RC-3

- Notes:**
1.  $\overline{\text{WE}}$  is held high for a read cycle.
  2. Device is continuously selected:  $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ .
  3. Address is valid prior to or coincident with  $\overline{\text{CE}}$  transition low.
  4.  $\overline{\text{OE}} = V_{\text{IL}}$ .
  5. Device is continuously selected:  $\overline{\text{CE}} = V_{\text{IL}}$ .

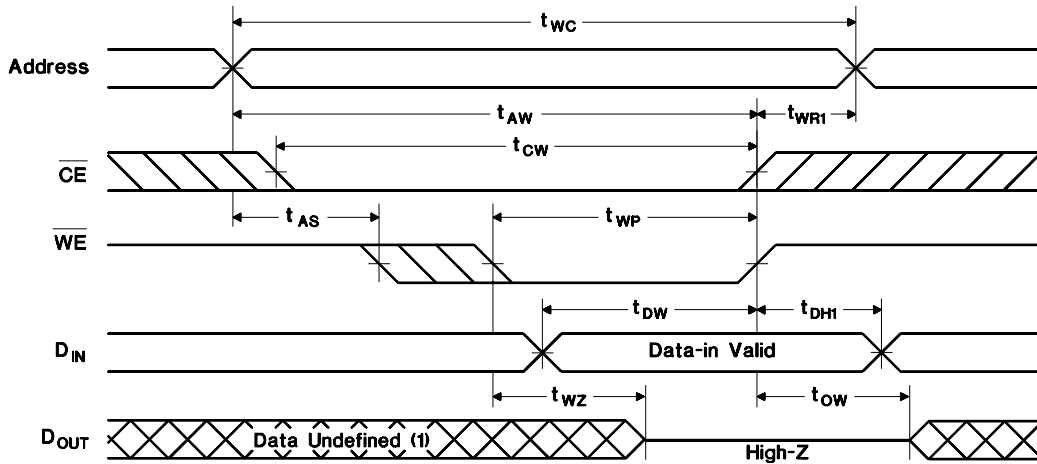
## bq4011/bq4011Y

### Write Cycle (TA = TOPR, VCCmin ≤ VCC ≤ VCCmax)

Symbol	Parameter	-70/-70N		-100		-150/-150N		-200		Units	Conditions/Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
tWC	Write cycle time	70	-	100	-	150	-	200	-	ns	
tCW	Chip enable to end of write	55	-	90	-	100	-	150	-	ns	(1)
tAW	Address valid to end of write	55	-	80	-	90	-	150	-	ns	(1)
tAS	Address setup time	0	-	0	-	0	-	0	-	ns	Measured from address valid to beginning of write. (2)
tWP	Write pulse width	55	-	75	-	90	-	130	-	ns	Measured from beginning of write to end of write. (1)
tWR1	Write recovery time (write cycle 1)	5	-	5	-	5	-	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
tWR2	Write recovery time (write cycle 2)	15	-	15	-	15	-	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
tDW	Data valid to end of write	30	-	40	-	50	-	70	-	ns	Measured from first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$ .
tDH1	Data hold time (write cycle 1)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
tDH2	Data hold time (write cycle 2)	0	-	0	-	0	-	0	-	ns	Measured from $\overline{CE}$ going high to end of write cycle.(4)
tWZ	Write enabled to output in high Z	0	25	0	35	0	50	0	70	ns	I/O pins are in output state. (5)
tOW	Output active from end of write	5	-	5	-	5	-	5	-	ns	I/O pins are in output state. (5)

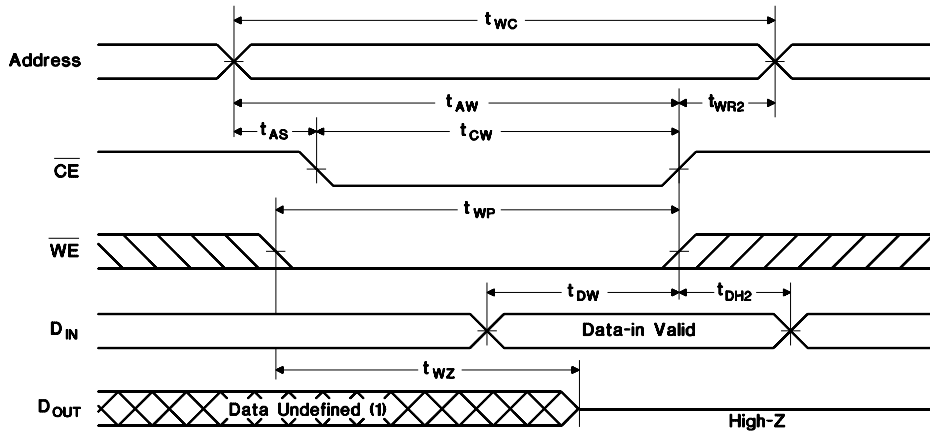
- Notes:**
1. A write ends at the earlier transition of  $\overline{CE}$  going high and  $\overline{WE}$  going high.
  2. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CE}$  going low and  $\overline{WE}$  going low.
  3. Either tWR1 or tWR2 must be met.
  4. Either tDH1 or tDH2 must be met.
  5. If  $\overline{CE}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high-impedance state.

**Write Cycle No. 1 ( $\overline{WE}$ -Controlled)** 1,2,3



WC-3

**Write Cycle No. 2 ( $\overline{CE}$ -Controlled)** 1,2,3,4,5



WC-4

- Notes:**
1.  $\overline{CE}$  or  $\overline{WE}$  must be high during address transition.
  2. Because I/O may be active ( $\overline{OE}$  low) during this period, data input signals of opposite polarity to the outputs must not be applied.
  3. If  $\overline{OE}$  is high, the I/O pins remain in a state of high impedance.
  4. Either  $t_{WR1}$  or  $t_{WR2}$  must be met.
  5. Either  $t_{DH1}$  or  $t_{DH2}$  must be met.

# bq4011/bq4011Y

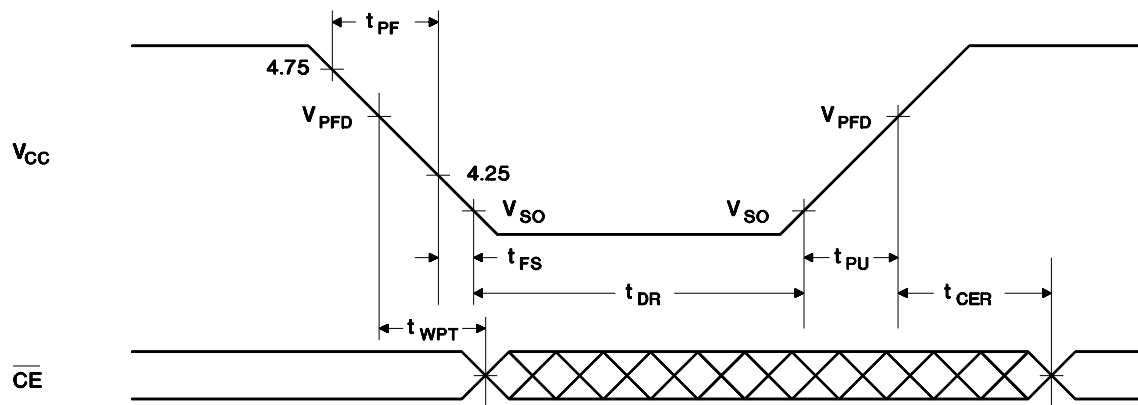
## Power-Down/Power-Up Cycle ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$t_{PF}$	$V_{CC}$ slew, 4.75 to 4.25 V	300	-	-	$\mu s$	
$t_{FS}$	$V_{CC}$ slew, 4.25 to $V_{SO}$	10	-	-	$\mu s$	
$t_{PU}$	$V_{CC}$ slew, $V_{SO}$ to $V_{PFD}$ (max.)	0	-	-	$\mu s$	
$t_{CER}$	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.
$t_{DR}$	Data-retention time in absence of $V_{CC}$	10	-	-	years	$T_A = 25^\circ C$ . (2)
$t_{DR-N}$	Data-retention time in absence of $V_{CC}$	6	-	-	years	$T_A = 25^\circ C$ (2); industrial temperature range (-N) only.
$t_{WPT}$	Write-protect time	40	100	150	$\mu s$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected.

- Notes:**
1. Typical values indicate operation at  $T_A = 25^\circ C$ ,  $V_{CC} = 5V$ .
  2. Battery is disconnected from circuit until after  $V_{CC}$  is applied for the first time.  $t_{DR}$  is the accumulated time in absence of power beginning when power is first applied to the device.

**Caution:** Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

## Power-Down/Power-Up Timing



PD-B

Aug. 1993 C

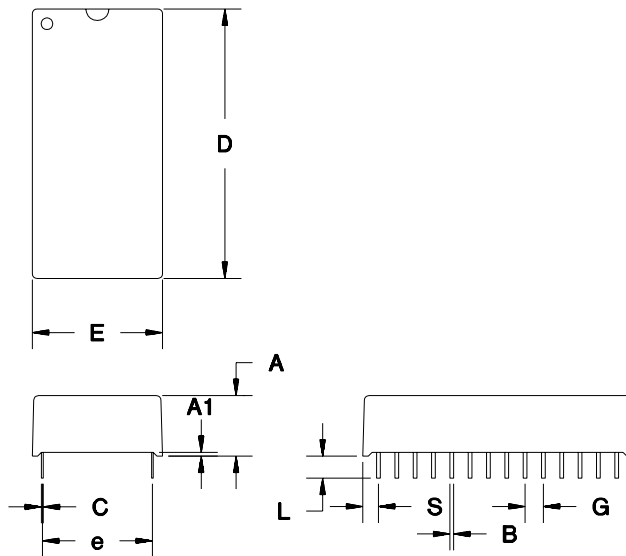


**Data Sheet Revision History**

Change No.	Page No.	Description
1	2, 3, 4, 6, 8, 9	Added industrial temperature range for bq4011YMA-150N.
2	1, 4, 6, 9	Added 70 ns speed grade for bq4011Y-70 and added industrial temperature range for bq4011YMA-70N.

**Notes:** Change 1 = Sept 1992 B changes from Sept. 1990 A.  
 Change 2 = Aug. 1993 C changes from Sept. 1991 B.

**28-Pin MA (A-type module)**



**28-Pin MA (A-Type Module)**

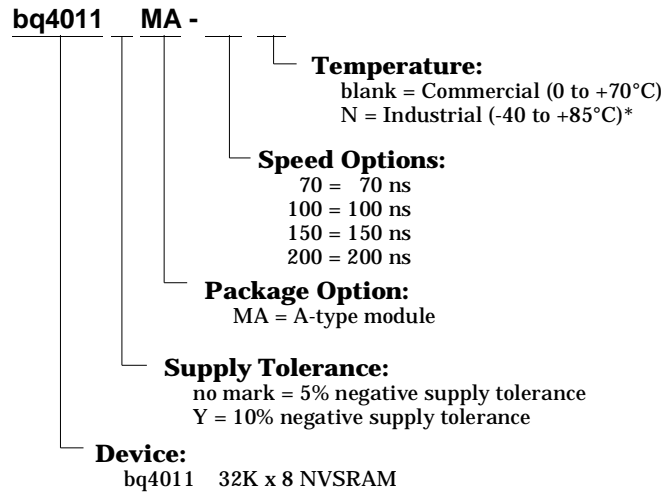
Dimension	Minimum	Maximum
A	0.365	0.375
A1	0.015	-
B	0.017	0.023
C	0.008	0.013
D	1.470	1.500
E	0.710	0.740
e	0.590	0.630
G	0.090	0.110
L	0.120	0.150
S	0.075	0.110

All dimensions are in inches.

# bq4011/bq4011Y

---

## Ordering Information



**\*Note:** Only 10% supply ("Y") version is available in industrial temperature range; contact factory for speed grade availability.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
BQ4011MA-100	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011MA-150	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011MA-200	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-100	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-150	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-150N	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-200	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-70	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI
BQ4011YMA-70N	ACTIVE	DIP MOD ULE	MA	0	1	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265