ATF15xx-DK3 Development Kit

User Guide

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Section 1
Introduction

1.1 CPLD Development/ Programmer Kit

The Atmel CPLD Development/Programmer Kit (P/N: ATF15xx-DK3) is a complete development system and an In-System Programming (ISP) programmer for the ATF15xx family of industry standard pin compatible Complex Programmable Logic Devices (CPLDs) with Logic Doubling® features. This kit provides designers a very quick and easy way to develop prototypes and evaluate new designs with an ATF15xx ISP CPLD. The ATF15xx family of ISP CPLDs includes the ATF15xxAS, ATF15xxASL, ATF15xxASV, ATF15xxASVL, and ATF15xxBE CPLDs. With the availability of the different Socket Adapter Boards to support all the package types(1) offered in the ATF15xx family of ISP CPLDs, this CPLD Development/Programmer Board can be used as an ISP programmer to program the ATF15xx ISP CPLDs in all the available package types(1) through the industry standard JTAG interface (IEEE 1149.1).

1.2 Kit Contents

- CPLD Development/Programmer Board
- 44-pin TQFP Socket Adapter Board (P/N: ATF15xx-DK3-SAA44)(2)
- Atmel CPLD ISP Multi-Volt (MV) Download Cable
- Atmel PLD Software CDs (includes ProChip Designer®, Precision RTL Synthesis, ModelSim, latest ProChip patch, Atmel-WinCUPL™, and other EPLD software)
- Two 44-pin TQFP Sample Devices (one ATF1502BE and one ATF1504ASV)

Notes: 1. Socket adapter board for 100-pin PQFP is not offered.
2. Only the 44-pin TQFP Socket Adapter Board is included in this kit. Other Socket Adapter Boards are sold separately. Please refer to Section 1.6 for ordering information of the Socket Adapter Boards.

1.3 Kit Features

1.3.1 CPLD Development/ Programmer Board

- 10-pin JTAG-ISP port
- Regulated power supply circuits for 9V DC power source
- Selectable 5V, 3.3V, 2.5V, or 1.8V I/O voltage supply
- Selectable 1.8V, 3.3V, or 5.0V core voltage supply

- 44-pin TQFP Socket Adapter Board
- Headers for I/O pins of the ATF15xx device
- 2 MHz Crystal Oscillator
- Four 7-segment LED displays
- Eight individual LEDs
- Eight push-button switches
- Global Clear and Output Enable push-button switches
- Current measurement jumpers

1.3.2 Logic Doubling CPLDs

- ATF1502BE 1.8V low-power 32-macrocell ISP CPLD with Logic Doubling architecture
- ATF1504ASV 3.3V 64-macrocell ISP CPLD with Logic Doubling architecture

1.3.3 CPLD ISP Download Cable

- 5V/3.3V/2.5V/1.8V ISP Download Cable for PC Parallel Printer (LPT) Port

1.3.4 PLD Software CD-ROM

- Free Atmel-WinCUPL Design Software
- ProChip Designer v4.0
- ProChip Designer v4.0 Patch
- Precision RTL Synthesis
- ModelSim
- Atmel CPLD ISP Software (ATMISP)
- POF2JED Conversion Utility
- User Guides and Tutorials

1.4 Device Support

The Atmel CPLD Development/Programmer Board supports the following devices in all speed grades and packages (except 100-PQFP):

ATF1502BE	ATF1508ASV/ASVL
ATF1502AS/ASL	ATF1502ASV
ATF1504BE	ATF1504ASV/ASVL
ATF1504AS/ASL	ATF1508AS/ASL

1.5 System Requirements

The minimum hardware and software requirements to program an ATF15xx ISP CPLD designed using the ProChip Designer Software on the CPLD Development/Programmer Board through the Atmel CPLD ISP Software (ATMISP) V6.0 or later are:

- Pentium® or Pentium-compatible microprocessor-based computer
- Windows XP®, Windows® 98, Windows NT® 4.0, or Windows 2000
- 64-MByte RAM
- 200-MByte free hard disk space
- Windows-supported mouse
- Available parallel printer (LPT) port
- 9V DC power supply with 500 mA of supply current
- SVGA monitor (800 x 600 resolution)

1.6 Ordering Information

Part Number	Description
ATF15xx-DK3	Atmel CPLD Development/Programmer Kit (includes ATF15xxDK3-SAA44)
ATF15xxDK3-SAA100	100-pin TQFP Socket Adapter Board for DK3 Board
ATF15xxDK3-SAJ44	44-pin PLCC Socket Adapter Board for DK3 Board
ATF15xxDK3-SAJ84	84-pin PLCC Socket Adapter Board for DK3 Board
ATF15xxDK3-SAA44	44-pin TQFP Socket Adapter Board for DK3 Board

Other socket adapters to support other packages will be available in the near future.

1.7 References

To help PLD designers use the different Atmel PLD software, documentation such as help files, tutorials, application notes/briefs, and user guides are available.

1.7.1 ProChip Designer

ProChip Desinger Help Files	From the ProChip Designer main window, click on HELP and then select PROCHIP DESIGNER HELP.
Tutorials	From the ProChip Designer main window, click on HELP and then select TUTORIALS.
Known Problems & Solutions	From the ProChip Designer main window, click on HELP and then select REVIEW KPS.

1.7.2 Atmel-WinCUPL

Help Files	From the Atmel-WinCUPL main window, click on HELP and then select CONTENTS.
CUPL Programmers Reference Guide	From the Atmel-WinCUPL main window, click on HELP and then select CUPL PROGRAMMERS REFERENCE.
Tutorials	From the Atmel-WinCUPL main window, click on HELP, select ATMEL INFO and then select TUTORIAL1.PDF.
Known Problems & Solutions	From the Atmel-WinCUPL main window, click on HELP, select ATMEL INFO and then select CUPL_BUG.PDF.

1.7.3 ATMISP

Help Files	From the ATMISP main window, click on HELP and then select ISP HELP.
Tutorials	From the ATMISP main window, click on HELP, and then select ATMISP TUTORIAL.
Known Problems & Solutions	Using Windows Explorer, go to the directory where ATMISP is installed and open the README.TXT file through any ASCII text editor.

1.7.4 POF2JED

ATF15xx Conversion Application Brief	from the POF2JED main window, click on HELP and then select CONVERSION OPTIONS.

1.8 Technical Support

For technical support on any Atmel PLD related issues, please contact Atmel PLD Applications Group at:

URL: www.atmel.com/dyn/products/support.asp

FAQ: www.atmel.com/dyn/products/tech_support.asp?faq=y

Hotline: 1-408-436-4333

Email : pld@atmel.com

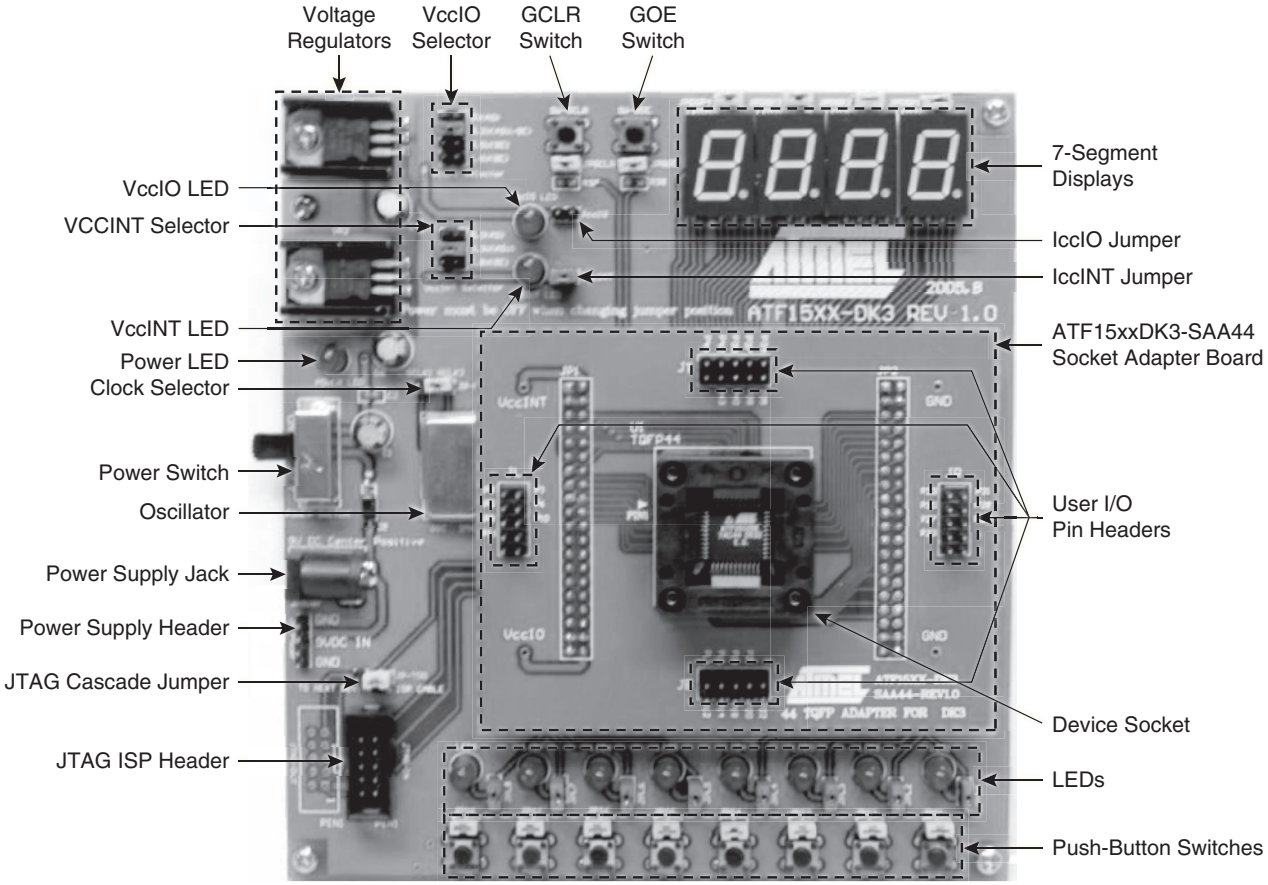
Section 2

Hardware Description

2.1 Atmel CPLD Development/ Programmer Board

Atmel CPLD Development/Programmer Board along with the Socket Adapter Board as shown in Figure 2-1 contains many features that designers will find very useful when developing, prototyping, or evaluating their ATF15xx CPLD design. Features such as push-button switches, LEDs, 7-segment displays, 2-MHz crystal oscillator, 5V/3.3V/2.5V/1.8V VCCI/O selector, 1.8V/3.3V/5.0V VCCINT selector, JTAG-ISP port, and socket adapters make this a very versatile starter/development kit and an ISP programmer for the ATF15xx family of JTAG-ISP CPLDs.

Figure 2-1. CPLD Development/Programmer Board with 44-pin TQFP Socket Adapter Board



2.1.1 7-segment Displays with Selectable Jumpers

Atmel CPLD Development/Programmer Board contains four seven-segment displays to allow the designers to observe the outputs of the ATF15xx CPLD. These four displays are labeled DSP1, DSP2, DSP3, and DSP4, and have common anode LEDs with the common anode lines connected to VCCIO (I/O supply voltage for the CPLD) through series resistors with selectable jumpers labeled JPDSP1, JPDSP2, JPDSP3, or JPDSP4. These jumpers can be removed to disable the displays by unconnecting the VCCIO to the displays. Individual cathode lines are connected to the I/O pins of the ATF15xx CPLD on the CPLD Development/Programmer Board. To turn on a particular segment including the DOT of a display, the corresponding ATF15xx I/O pin connected to this LED segment must be in a logic low state with the corresponding selectable jumper set. Hence, the outputs of the ATF15xx need to be configured as active-low outputs in the design file. These displays work best at 2.5V VCCIO or higher.

Each segment of each display is hard-wired to one specific I/O pin of the ATF15xx. For the higher pin count devices (100-pin and larger), all seven segments and the DOT segments of the four displays are connected to the I/O pins of the ATF15xx. However, for the lower pin count devices, only a subset of the displays (1st and 4th displays) are connected to the ATF15xx's I/O pins. Tables 2-1, 2-2, 2-3, and 2-4 show the connections for 7-segment displays to the ATF15xx in different package types. The circuit schematic of the displays and jumpers is shown in Figure 2-2.

Figure 2-2. Circuit Diagram of 7-segment Display and Jumpers

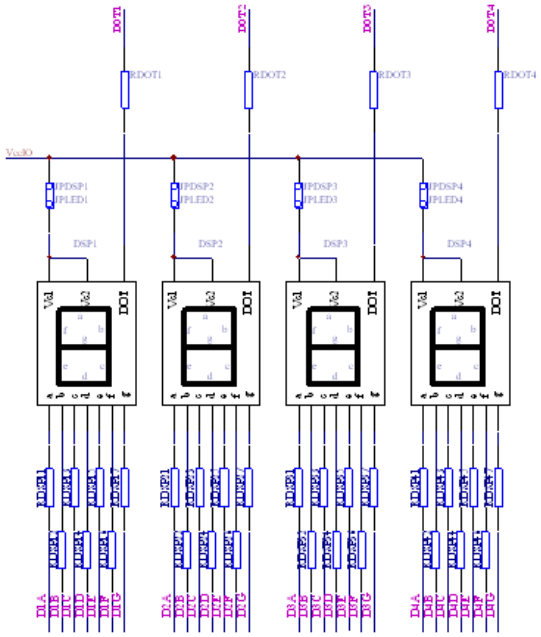


Table 2-1. Connections of ATF15xx 44-pin TQFP to 7-segment Displays

DSP/Segment	PLD Pin #	DSP/Segment	PLD Pin #
1/A	27	3/A	NC
1/B	33	3/B	NC
1/C	30	3/C	NC
1/D	21	3/D	NC
1/E	18	3/E	NC
1/F	23	3/F	NC
1/G	20	3/G	NC
1/DOT	31	3/DOT	NC
2/A	NC	4/A	3
2/B	NC	4/B	10
2/C	NC	4/C	6
2/D	NC	4/D	43
2/E	NC	4/E	35
2/F	NC	4/F	42
2/G	NC	4/G	34
2/DOT	NC	4/DOT	11

Table 2-2. Connections of ATF15xx 44-pin PLCC to 7-segment Displays

DSP/Segment	PLD Pin #	DSP/Segment	PLD Pin #
1/A	33	3/A	NC
1/B	39	3/B	NC
1/C	36	3/C	NC
1/D	27	3/D	NC
1/E	24	3/E	NC
1/F	29	3/F	NC
1/G	26	3/G	NC
1/DOT	37	3/DOT	NC
2/A	NC	4/A	9
2/B	NC	4/B	16
2/C	NC	4/C	12
2/D	NC	4/D	5
2/E	NC	4/E	41
2/F	NC	4/F	4
2/G	NC	4/G	40
2/DOT	NC	4/DOT	17

Table 2-3. Connections of ATF15xx 84-pin PLCC to 7-segment Displays

DSP/Segment	PLD Pin #	DSP/Segment	PLD Pin #
1/A	68	3/A	22
1/B	74	3/B	28
1/C	70	3/C	25
1/D	63	3/D	21
1/E	58	3/E	16
1/F	65	3/F	17
1/G	61	3/G	12
1/DOT	73	3/DOT	29
2/A	52	4/A	5
2/B	57	4/B	10
2/C	55	4/C	8
2/D	48	4/D	79
2/E	41	4/E	76
2/F	50	4/F	77
2/G	45	4/G	75
2/DOT	50	4/DOT	11

Table 2-4. Connections of ATF15xx 100-pin TQFP to 7-segment Displays

DSP/Segment	PLD Pin #	DSP/Segment	PLD Pin #
1/A	67	3/A	13
1/B	71	3/B	19
1/C	69	3/C	16
1/D	61	3/D	8
1/E	57	3/E	83
1/F	64	3/F	6
1/G	60	3/G	92
1/DOT	75	3/DOT	20
2/A	52	4/A	100
2/B	54	4/B	94
2/C	47	4/C	97
2/D	41	4/D	81
2/E	46	4/E	76
2/F	40	4/F	80
2/G	45	4/G	79
2/DOT	56	4/DOT	93

2.1.2 LEDs with Selectable Jumpers

Atmel CPLD Development/Programmer Board has eight individual LEDs, which allow designers to display the output signals from the user I/Os of the ATF15xx CPLD. These eight LEDs are labeled LED1 to LED8 on the Atmel CPLD Development/Programmer Board. The cathode of each LED is connected to ground through a series resistor while the anode of each LED is connected to a user I/O pin of the CPLD through the JPL1/JPL2/PL3/JPL4/JPL5/JPL6/JPL7/JPL8 selectable jumper. These jumpers can be removed to disable the LEDs by unconnecting the anodes of the LEDs to the I/O pins of the CPLD. Figure 2-3 shows the circuit diagram of the LEDs with the selection jumpers.

To turn on a particular LED, the corresponding ATF15xx I/O pin connected to the LED must be in a logic high state with the corresponding jumper set. Hence, the outputs of the ATF15xx need to be configured as active-high outputs in the design files. These LEDs work best at 2.5V VCCIO or higher.

The lower pin-count devices (44-pin) only have four I/Os connected to LED1, LED2, LED3, and LED4. For the higher pin-count devices (100-pin and larger), all eight LEDs are connected to the I/Os of the device. Tables 2-5, 2-6, 2-7, and 2-8 show the connections of the CPLD I/Os to the LEDs in the different package types.

Figure 2-3. Circuit Diagram of the LEDs and Jumpers

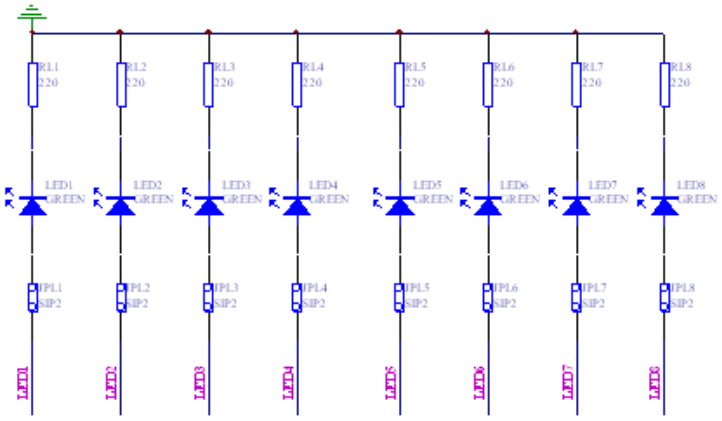


Table 2-5. Connections of ATF15xx 44-pin TQFP to LEDs

LED #	PLD Pin #
LED1	28
LED2	25
LED3	22
LED4	19

Table 2-6. Connections of ATF15xx 44-pin PLCC to LEDs

LED #	PLD Pin #
LED1	34
LED2	31
LED3	28
LED4	25

Table 2-7. Connections of ATF15xx 84-pin PLCC to LEDs

LED #	PLD Pin #
LED1	69
LED2	67
LED3	64
LED4	60
LED5	27
LED6	24
LED7	18
LED8	15

Table 2-8. Connections of ATF15xx 100-pin TQFP to LEDs

LED #	PLD Pin #
LED1	68
LED2	65
LED3	63
LED4	58
LED5	17
LED6	14
LED7	10
LED8	9

2.1.3 Push-button Switches with Selectable Jumpers for I/O Pins

Atmel CPLD Development/Programmer Board contains eight push-button switches, which are connected to the I/O pins of the CPLD. They allow designers to send input logic signals to the user I/O pins of the ATF15xx CPLD. These eight switches are labeled SW1 to SW8 on the Atmel CPLD Development/Programmer Board. One end of each input push-button switch is connected to VCCIO while the other end of each push-button switch is connected to a pull-down resistor and then connected to the specific I/O pin of the CPLD through the JPS1/JPS2/JPS3/JPS4/JPS5/JPS6/JPS7/JPS8 selectable jumper.

If any one of these switches is pressed and the corresponding jumper is set, the specific I/O pin of the device will be driven to a logic high state by the output of switch circuit. Since each push-button switch is also connected to a pull-down resistor, the input will have a logic low state if the switch is not pressed with the corresponding jumper set. If the push-button jumper is not set, the corresponding pin will be treated as an unconnected pin. Figure 2-4 on page 2-7 is a circuit diagram of the push-button switch and selectable jumper. Tables 2-9, 2-10, 2-11, and 2-12 show the connections of these eight push-button switches to the CPLD I/O pins in the different package types.

Figure 2-4. Circuit Diagram of the Push-button Switches and Jumpers for the I/O Pins

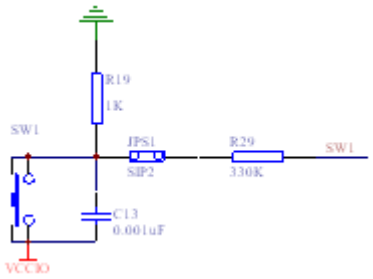


Table 2-9. Connections of ATF15xx 44-pin TQFP to the Switches for I/O Pins

Push Button #	PLD Pin #
SW1	15
SW2	14
SW3	13
SW4	12
SW5	8
SW6	5
SW7	2
SW8	44

Table 2-10. Connections of ATF15xx 44-pin PLCC to the Switches for I/O Pins

Push Button #	PLD Pin #
SW1	21
SW2	20
SW3	19
SW4	18
SW5	14
SW6	11
SW7	8
SW8	6

Table 2-11. Connections of ATF15xx 84-pin PLCC to the Switches for I/O Pins

Push Button #	PLD Pin #
SW1	54
SW2	51
SW3	49
SW4	44
SW5	9
SW6	6
SW7	4
SW8	80

Table 2-12. Connections of ATF15xx 100-pin TQFP to the Switches for I/O Pins

Push Button #	PLD Pin #
SW1	48
SW2	36
SW3	44
SW4	37
SW5	96
SW6	98
SW7	84
SW8	99

2.1.4 Push-button Switches with Selectable Jumpers for GCLR and OE1 Pins

Atmel CPLD Development/Programmer Board also contains two push-button switches for the Global Clear (GCLR) and Output Enable (OE1) pins of the CPLD. They allow the designers to control the logic states of the OE1 and GCLR inputs of the ATF15xx CPLD. These two switches are labeled SW-GCLR and SW-GOE1 on the Atmel CPLD Development/Programmer Board. One end of the SW-GCLR input push-button switch is connected to ground (GND). The other end of the push-button switch is connected to a pull-up resistor to VCCIO, and then connected to the GCLR dedicated input pin of the ATF15xx. It is intended to be used as an active-low reset signal to reset the registers in the ATF15xx with the JPGCLR selectable jumper set. Similarly, one end of the SW-GOE1 input push-button switch is connected to ground (GND). The other end of the push-button switch is connected to a pull-up resistor to VCCIO, and then connected to the OE1 dedicated input pin of the ATF15xx. It is intended to be used as an active-low output enable signal to control the enabling/disabling of the tri-state output buffers in the ATF15xx with the JPGOE selectable jumper set. Figure 2-5 on page 2-9 is the circuit diagram of these two push-button switches and the jumpers for the GCLR and OE1 pins.

If any of these push-button switches is pressed and the corresponding jumper is set, then the specific I/O of the CPLD will be driven to a logic low state. Since each push-button is also connected to a pull-up resistor, the corresponding CPLD input will have a logic high state if the push-button switch is not pressed with the corresponding selectable jumper set. If the selectable jumper is not set, the corresponding dedicated input pin of the CPLD can be considered a “no connect” (NC) pin. Table 2-13 on page 2-9

shows the pin numbers of the GCLR and OE1 dedicated input pins of the ATF15xx in all the different available package types.

Figure 2-5. Circuit Diagram of Push-button Switches and Selectable Jumpers for GCLR and OE1

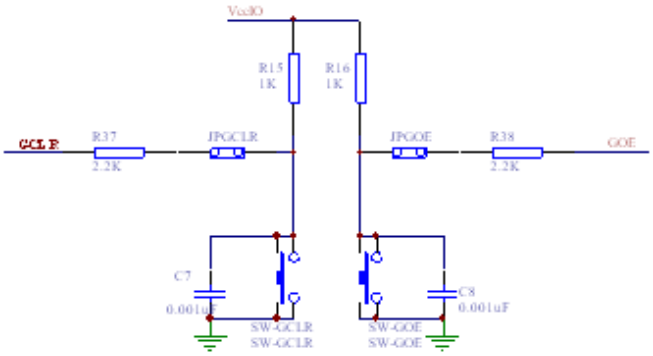


Table 2-13. Pin Numbers of GCLR and OE1

	44-pin TQFP	44-pin PLCC	84-pin PLCC	100-pin TQFP
GCLR	39	1	1	89
OE1	38	44	84	88

2.1.5 2 MHz Oscillator and Clock Selection Jumper

The Clock Selection Jumper, labeled JP-GCLK, on the CPLD Development/Programmer Board is a two-position jumper that allows the users to select which GCLK dedicated input pin (either GCLK1 or GCLK2) of the ATF15xx should be connected to the output of the 2 MHz oscillator. In addition, the jumper can be removed to allow an external clock source to be connected to GCLK1 and/or GCLK2 of the ATF15xx. Figure 2-6 is the circuit diagram of the oscillator and selection jumper. Table 2-14 on page 2-10 shows the pin numbers for the GCLK1 and GCLK2 dedicated input pins of the ATF15xx in all the different available package types.

Note: If GCLK1 jumper is set, the jumper will be located toward the side of the board. On the other hand, if GCLK2 jumper is set, the jumper will be located toward the middle of the board.

Figure 2-6. Circuit Diagram of Oscillator and Clock Selection Jumper

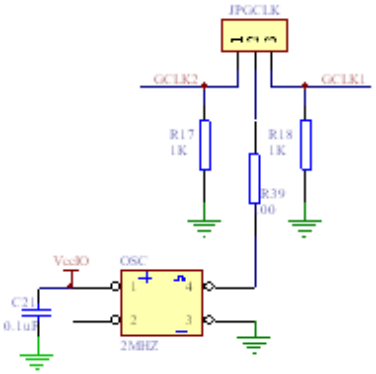


Table 2-14. Pin Numbers of GCLK1 and GCLK2

	44-pin TQFP	44-pin PLCC	84-pin PLCC	100-pin TQFP
GCLK1	37	43	83	87
GCLK2	40	2	2	90

2.1.6 VCCIO and VCCINT Voltage Selection Jumpers and LEDs

The VCCIO and VCCINT Voltage Selection Jumpers, labeled VCCIO Selector and VCCINT Selector respectively on ATF15xx-DK3 Development/Programming Board, allow the designers to select I/O supply voltage level (VCCIO) and core supply voltage level (VCCINT) that are used for the target CPLD on the board. Once these jumpers are set correctly, the LEDs (labeled VCCINT LED and VCCIO LED) will be turn on as expected. However, at lower supply voltage levels (i.e. 2.5V or lower), the LEDs might be very dim.

For ATF15xxAS/ASL (5.0V) CPLDs, both the VCCIO Selector and VCCINT Selector jumpers MUST BE set to 5.0V. For ATF15xxASV/ASVL (3.3V) CPLDs, both the VCCIO Selector and VCCINT Selector Jumpers MUST BE set to 3.3V only. For the ATF15xxBE (1.8V) CPLDs, designers MUST SET VCCINT Selector jumper to 1.8V for its core voltage supply. However, designers can set the VCCIO Selector jumper to 3.3V, 2.5V, or 1.8V (but not 5.0V) in order for the I/Os of the ATF15xxBE CPLD to interface with different voltage levels devices.

Note: The power of the CPLD Development/Programmer Board MUST BE turned OFF when changing the position of the VCCIO or VCCINT voltage selection jumper (VCCIO Selector or VCCINT Selector).

2.1.7 ICCIO and ICCINT Jumpers

The IccIO and IccINT jumpers can be removed and used as Icc measurement points. When the jumpers are removed, current meters can be connected to the posts to measure the current consumption of the target CPLD. When users are not using these jumpers to measure the current, these jumpers must be set in order for the board and CPLD to operate.

2.1.8 Voltage Regulators

Two voltage regulators, labeled VR1 and VR2, are used to independently generate and regulate the VCCINT and VCCIO voltages from the 9V DC power supply. For details, please review the schematic of the ATF15xx-DK3 board.

2.1.9 Power Supply Switch and Power LED

The Power Supply Switch, labeled POWER SWITCH, can be switched to the ON or OFF position, which is used to turn on or off the power of the ATF15xx-DK3 board respectively. It allows the 9V DC voltage at the Power Supply Jack to pass to the voltage regulators when it is in the ON position. When the Power Supply Switch is turned ON, the Power LED (labeled POWER LED) will light up to indicate that the ATF15xx-DK3 board is supplied with power.

2.1.10 Power Supply Jack and Power Supply Header

The Atmel ATF15xx-DK3 Development/Programmer Board contains two different types of power supply connectors labeled JPower and JP Power. Either one of these power supply connectors can be used to connect a 9V DC power source to the board. The first power connector, labeled JPower, is a barrel power jack with a 2.1mm diameter post and it mates to a 2.1mm (inner diameter) x 5.5mm (outer diameter) female plug. The second is the power supply header, labeled JP Power, is a 4-pin male 0.1" header with 0.025" square posts. The availability of these two types of power connectors allows the users to choose the type of power supply equipment to use for ATF15xx-DK3 Development/Programmer Board. However, please note that only one of these two power supply connectors should be powered with a 9V DC source but not both at the same time.

2.1.11 JTAG ISP Connector and TDO Selection Jumper

The JTAG ISP Connector, labeled JTAG-IN, is used to connect the ATF15xx's JTAG port pins (TCK, TDI, TMS and TDO) through the ISP download cable to the parallel printer (LPT) port of a PC for JTAG ISP programming of the ATF15xx. Polarized connectors are used on the ATF15xx-DK3 and ISP Download Cable (ATDH1150VPC) Rev 6.0 or later to minimize connection problems. The PIN1 label at the bottom of the JTAG ISP connector indicates the pin 1 position of the 10-pin header and further reduces the chance of connecting the ISP Download Cable incorrectly.

To the left of the JTAG-IN connector, there are two columns of vias and they are labeled JTAG-OUT. They are intended to allow the users to create a JTAG daisy chain to perform JTAG operations to multiple devices. Users will need to solder the same type of connector as the one used for JTAG-IN into the JTAG-OUT position in order to utilize this available feature.

To create a JTAG daisy chain using multiple ATF15xx-DK3 boards, the TDO Selection Jumper, labeled JP-TDO, must be set to the appropriate position. For all the devices in the daisy chain except the last device, this jumper must be set to the "TO NEXT DEVICE" position. For the last device in the chain, this jumper must be set to the "TO ISP CABLE" position. When this jumper is in the "TO NEXT DEVICE" position, the TDO of that particular JTAG device will be connected to the TDI of the next JTAG device in the chain. When this jumper is in the "TO ISP CABLE" position, the TDO of that device will be connected to the TDO of the JTAG 10-pin connector, which will allow the TDO signal of the that device in the chain to be transmitted back to the host PC with the ISP software. Figure 2-7 below is a circuit diagram of the JTAG connectors and the JP-TDO jumper. Table 2-15 on page 2-12 lists the pin numbers of the four JTAG pins for the ATF15xx in all the available packages.

For a single device setup, the position of the JP-TDO jumper must be set to "TO ISP CABLE".

Figure 2-7. Circuit Diagram of the JTAG ISP Connectors and TDO Jumper

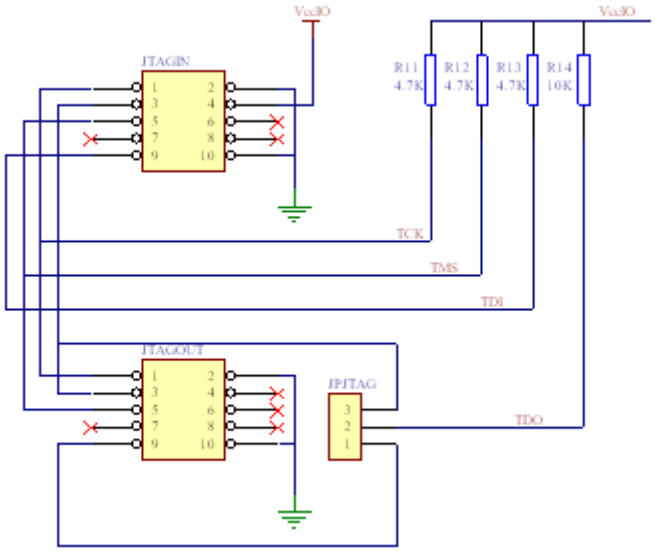


Table 2-15. Pin Numbers of JTAG Port Signals

	44-pin TQFP	44-pin PLCC	84-pin PLCC	100-pin TQFP
TDI	1	7	14	4
TDO	32	38	71	73
TMS	7	13	23	15
TCK	26	32	62	62

The ISP algorithm is controlled by the ATMISP software, which is running on the PC. The four JTAG signals are generated by the LPT port and they are buffered by the ISP download cable before going into the ATF15xx on the CPLD Development/Programmer Board. The pinout for the 10-pin JTAG Port Header on the CPLD Development/Programmer Board is shown in Figure 2-8 and the dimensions of this 10-pin male JTAG header are shown in Figure 2-9.

Figure 2-8. Pinout Diagram of 10-pin JTAG Port Header (Top-view)

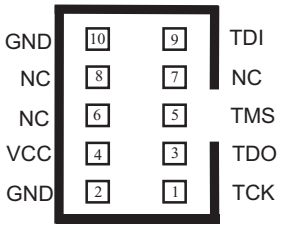
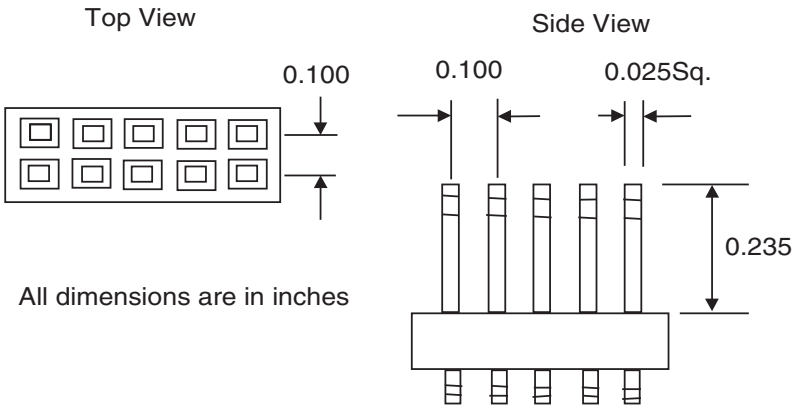


Figure 2-9. 10-pin Male Header Dimensions



The pinout of this 10-pin JTAG Port Header is compatible with the Altera® ByteBlaster, ByteBlasterMV, and ByteBlaster II cables. In addition, the ATMISP software allows users to choose either the Atmel CPLD ISP Cable or the ByteBlaster/ByteBlasterMV/ByteBlaster II cable to implement ISP.

2.2 Socket Adapter Board

Atmel ATF15xx-DK3 CPLD Development/Programmer Socket Adapter Boards (ATF15xx-DK3-XXXXX) are circuit boards that interface with the Atmel ATF15xx-DK3 CPLD Development/Programmer Board. They are used in conjunction with the ATF15xx-DK3 CPLD Development/Programmer Board to evaluate/program Atmel ATF15xx ISP CPLDs with different package types. At press time, there are four Socket Adapter Boards available for the ATF15xx-DK3 covering the 44-TQFP, 44-PLCC, 84-

PLCC, and 100-TQFP package types in the ATF15xx family of CPLDs. Socket Adapter boards for other packages will become available in the near future.

Each socket adapter board contains a socket for the Atmel ATF15xx device and with male headers on the bottom side, labeled JP1 and JP2. The headers on the bottom side mate with the female headers on the ATF15xx-DK3 board, labeled JP4 and JP3. The four 7-segment displays, push-button switches, JTAG port signals, oscillator, VCCINT, VCCIO, and GND on the CPLD Development/Programmer Board are connected to the ATF15xx device on the Socket Adapter Board through these two sets of connectors.

On the top of the 44-TQFP socket adapter, there are four 10-pin connectors with the same dimensions as the JTAG ISP connector. The pins of these four connectors are connected to the input and I/O pins (except the four JTAG pins) of the target CPLD device. They can be used to connect to an oscilloscope or logic analyzer to capture the activities of the input and I/O pins of the CPLD. They also can be used to connect the input and I/O pins of the CPLD to other external boards or devices for system level evaluation or testing.

2.3 Atmel CPLD ISP Download Cable

The Atmel CPLD ISP Download Cable (P/N: ATDH1150VPC) connects the parallel printer (LPT) port of your PC to the 10-pin JTAG header on the Atmel CPLD Development/Programmer Board or a custom circuit board. This is shown in Figure 2-10 on page 2-14. This ISP cable acts as a buffer to buffer the JTAG signals between the PC's LPT port and the ATF15xx on the circuit board. The Power-On LED on the back of the 25-pin male connector housing indicates that the cable is connected properly. Make sure this LED is turned on before using the Atmel CPLD ISP Software (ATMISP).

This ISP cable consists of a 25-pin (DB25) male connector, which is connected to the LPT port of a PC. The 10-pin female plug connects to the 10-pin male JTAG header on the ISP circuit board. The red color stripe on the ribbon cable indicates the orientation of Pin 1 of the female plug. The 10-pin male JTAG header on the CPLD Development/Programmer Board is polarized to prevent users from inserting the female plug in the wrong orientation.

The Atmel CPLD Development/Programmer kits includes an Atmel ISP cable; however, other supported ISP cables can also be used. The use of the ISP cable on Atmel development kit is depending on the device that is selected.

The following shows the appropriate ISP cable that can be used for the different voltage families of Atmel CPLDs.

1. Atmel-ISP Cable (Rev 4.0 or earlier) can be used for ATF15xxAS/ASL (5.0V) device only.
2. Atmel-ISP Cable (Rev 5.0) can be used for ATF15xxAS/ASL (5.0V) or ATF15xxASV/ASVL (3.3V) device only.
3. Atmel-ISP Cable (Rev 6.0), also known as the "Atmel CPLD-ISP MV Cable", can be used for ATF15xxAS/ASL (5.0V) or ATF15xxASV/ASVL (3.3V) or ATF15xxBE (1.8V core) device.
4. ByteBlaster ISP Cable can be used for ATF15xxAS/ASL (5.0V) device only.
5. ByteBlasterMV ISP Cable can be used for ATF15xxAS/ASL (5.0V) or ATF15xxASV/ASVL (3.3V) device only.
6. ByteBlaster II ISP Cable can be used for ATF15xxAS/ASL (5.0V) or ATF15xxASV/ASVL (3.3V) or ATF15xxBE (1.8V core) device.

Figure 2-10. Atmel ISP Cable Connection to ISP Hardware Board/Circuit Board

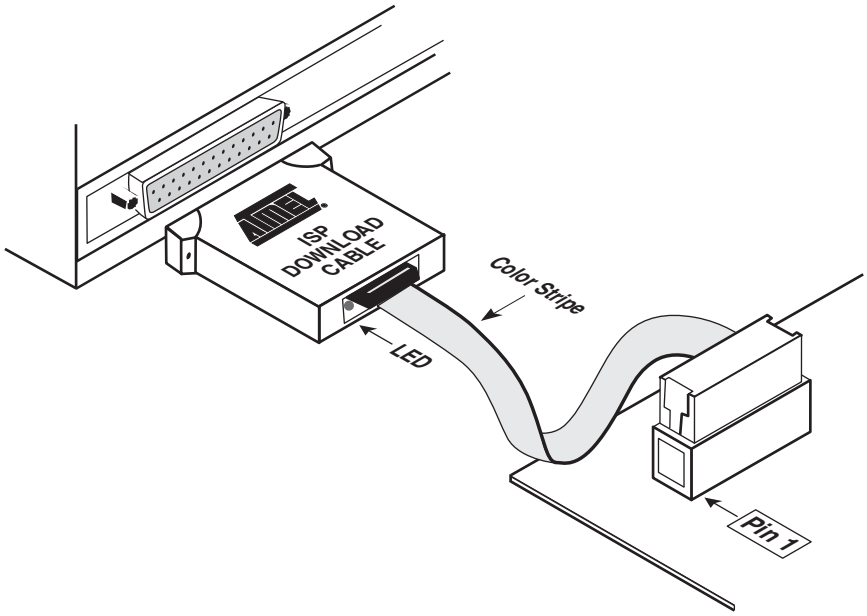
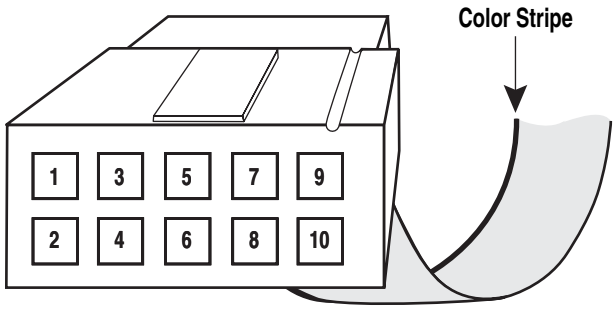


Figure 2-11 shows the pinout for the 10-pin female header on the Atmel ISP cable. The pinout on the 10-pin male header on the PC board (if used for ISP) must match this pinout.

Figure 2-11. Atmel ISP Download Cable 10-pin Female Header Pinout



Note: Your circuit board must supply Vcc and GND to the Atmel CPLD ISP Cable through the 10-pin male header. When programming ATF15xxBE device, VCCIO must be used for the ISP Cable.

Section 3

CPLD Design Flow Tutorial

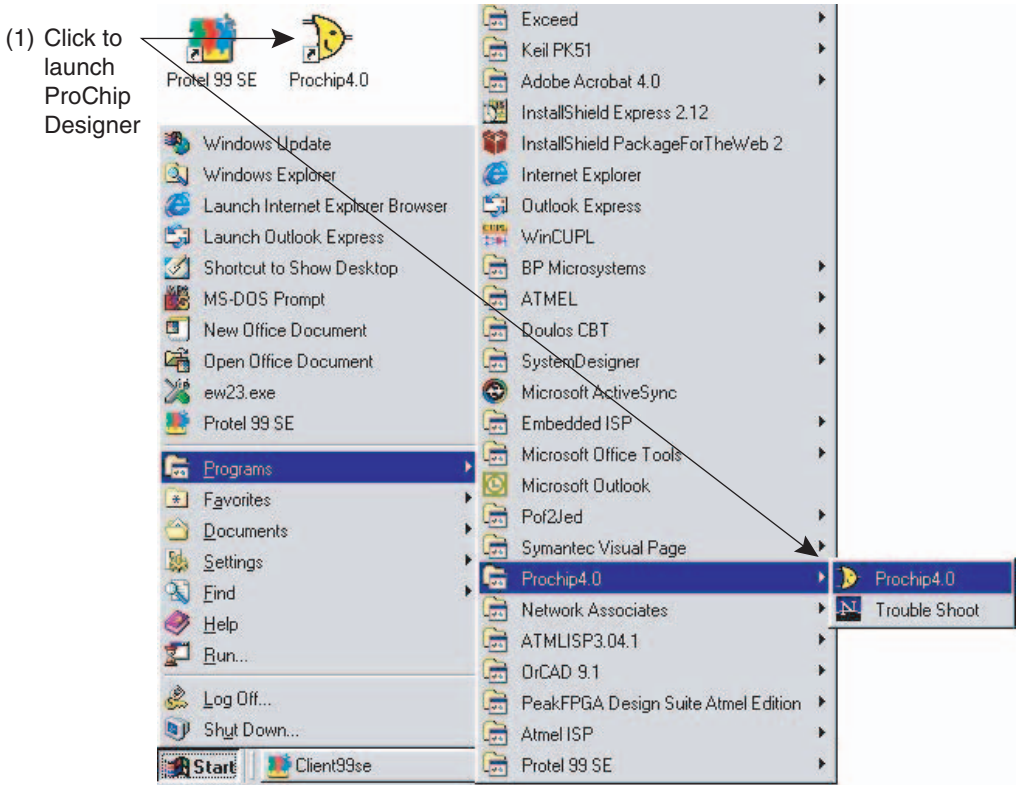
This tutorial will guide you through a complete VHDL design cycle for the Atmel ATF15xx CPLD. It provides step-by-step procedure to go through each phase of the design cycle from design entry, logic synthesis, device fitting, in-system programming, and finally verifying the design on the Atmel ATF15xx-DK3 CPLD Development/Programming Board.

Note: To complete this tutorial, ProChip Designer V4.0 with Level 2 Update and Atmel-ISP Software (ATMISP) V6.1 are required.

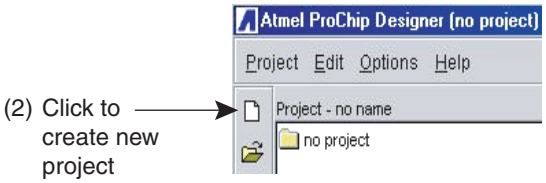
3.1 Create a Project using the "New Project Wizard"

Before starting the design process, a Project File must be created within ProChip Designer. ProChip Designer's New Project Wizard provides a very easy way to create a new project file.

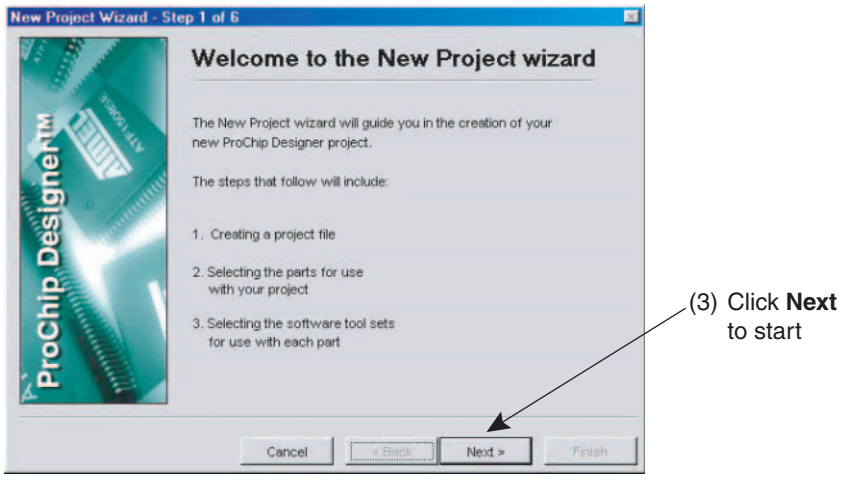
1. Click on the **Start** > **Programs** > **ProChip** icon to launch ProChip Designer. Or double-click on the **ProChip** icon on the desktop.



2. Click on **Project** > **New** or double-click on the **New Project** shortcut button to launch the New Project Wizard.



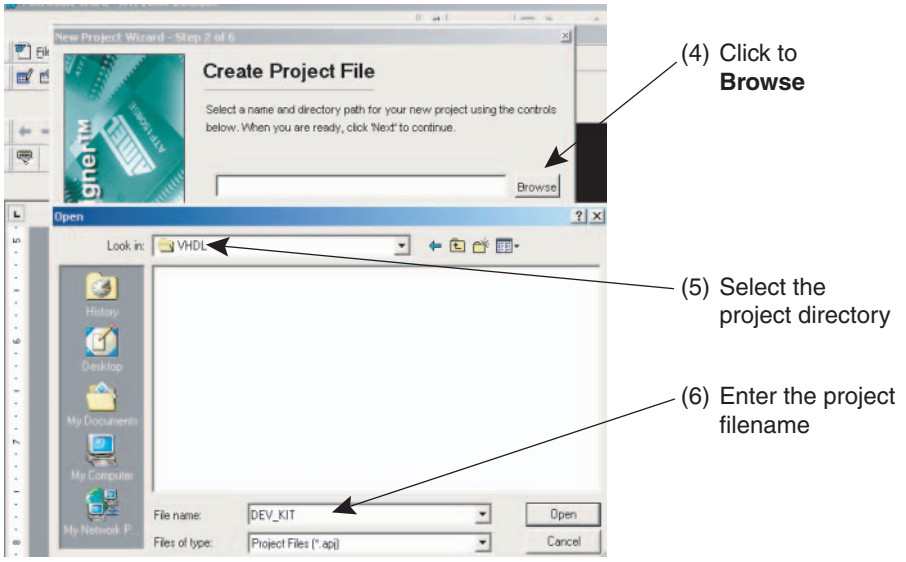
3. Click on the **Next** button to start the project file creation process.



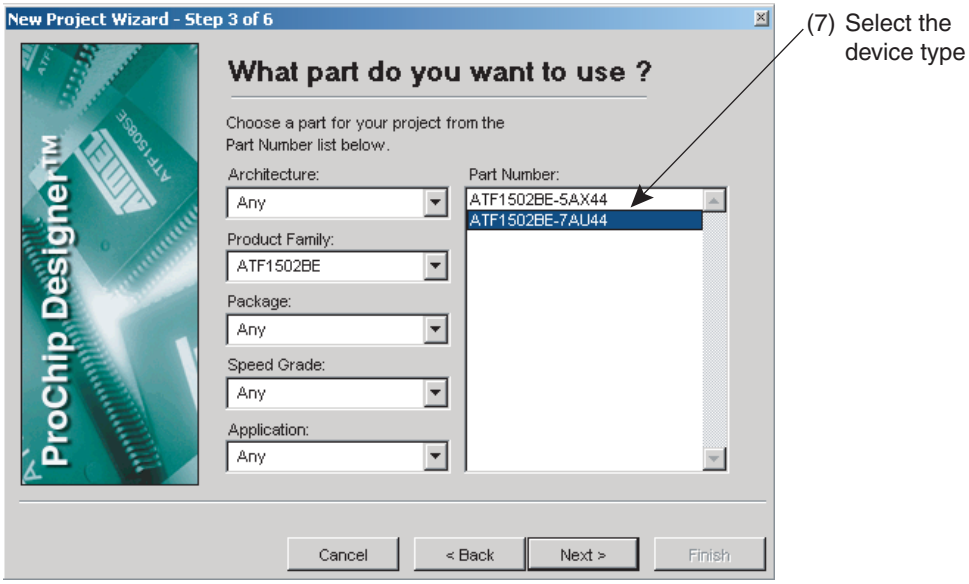
4. Click on the **Browse** button to open the browser window.

5. Use **C:\PROCHIP\DESIGNS\VHDL** as the directory of the project.
6. Enter **DEV_KIT.APJ** as the project filename. The extension of a project file must be **.APJ**.

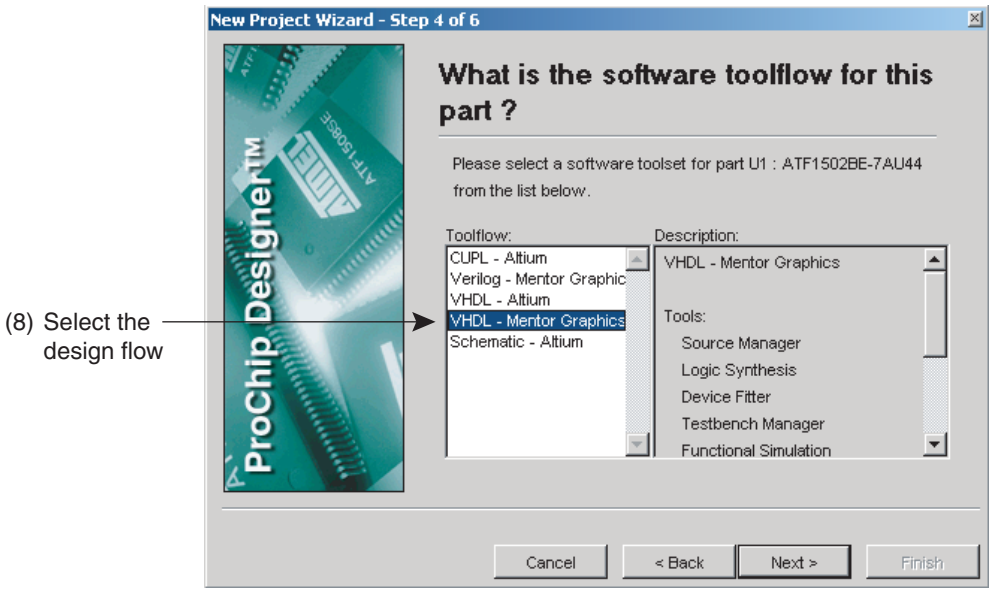
Note: The name and directory of the design project is specified in this window. All design, simulation, and other project files must be placed in this project directory.



7. Choose **ATF1502BE-7AU44** as the target device type for the project. Also review the filters that allow for selection of a specific speed grade or package type.



8. Select **VHDL - Mentor Graphics** as the software tool for this design flow.

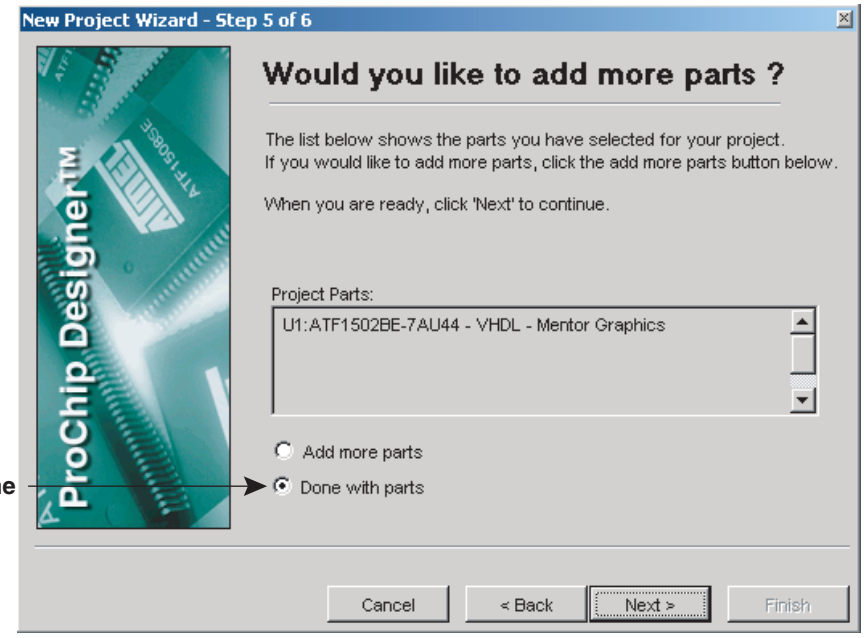


ProChip Designer V4.0 with software patch level 1 and later version supports the following design flows:

Design Flow	Design Flow Type
CUPL – Altium	CUPL design compiled through Altium Protel 99SE
Verilog – Mentor Graphics	Verilog design synthesized through Mentor Graphics Precision
VHDL – Altium	VHDL design synthesized through the Altium PeakFPGA
VHDL – Mentor Graphics	VHDL design synthesized through Mentor Graphics Precision
Schematic – Altium	Schematic design compiled through Altium Protel 99SE

9. Select **Done with parts** so that there will be only one device in this project.

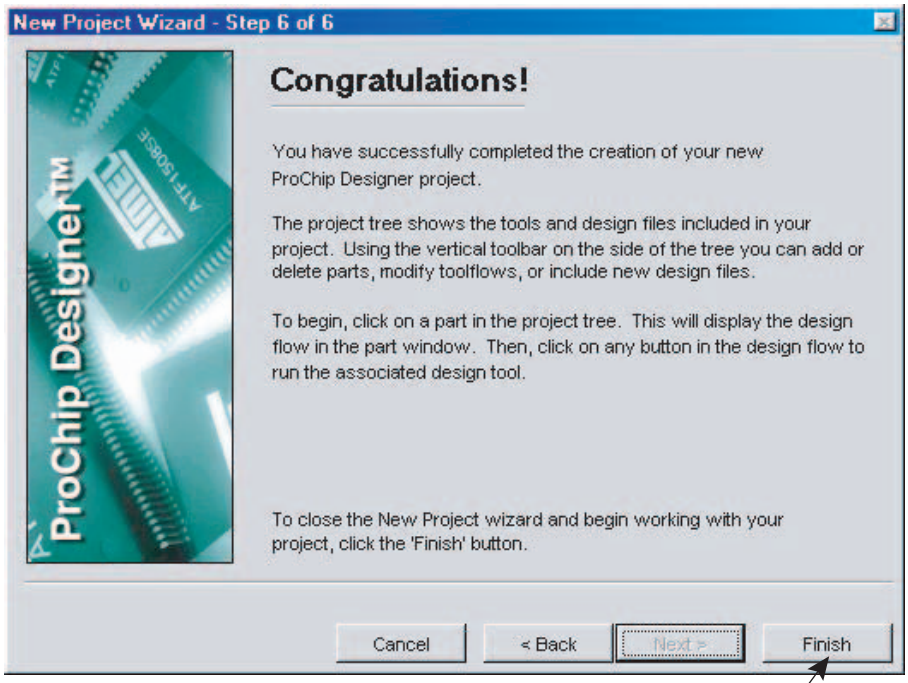
On the other hand, users can select **Add more parts** to include more parts to the current project directory.



(9) Select **Done with parts**

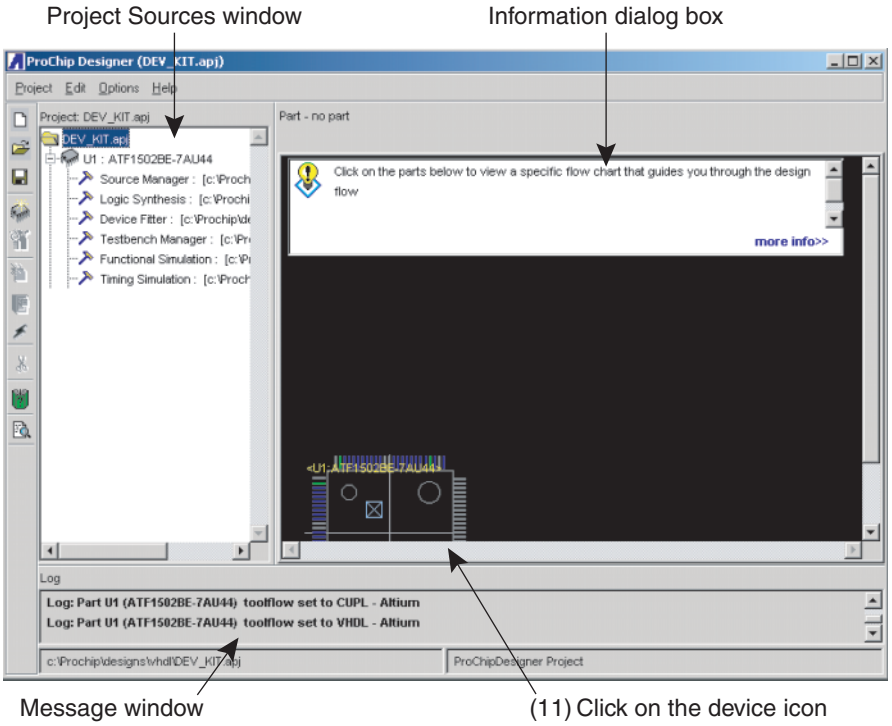
10. Click the **Finish** button to finish the New Project Wizard and the project creation process.

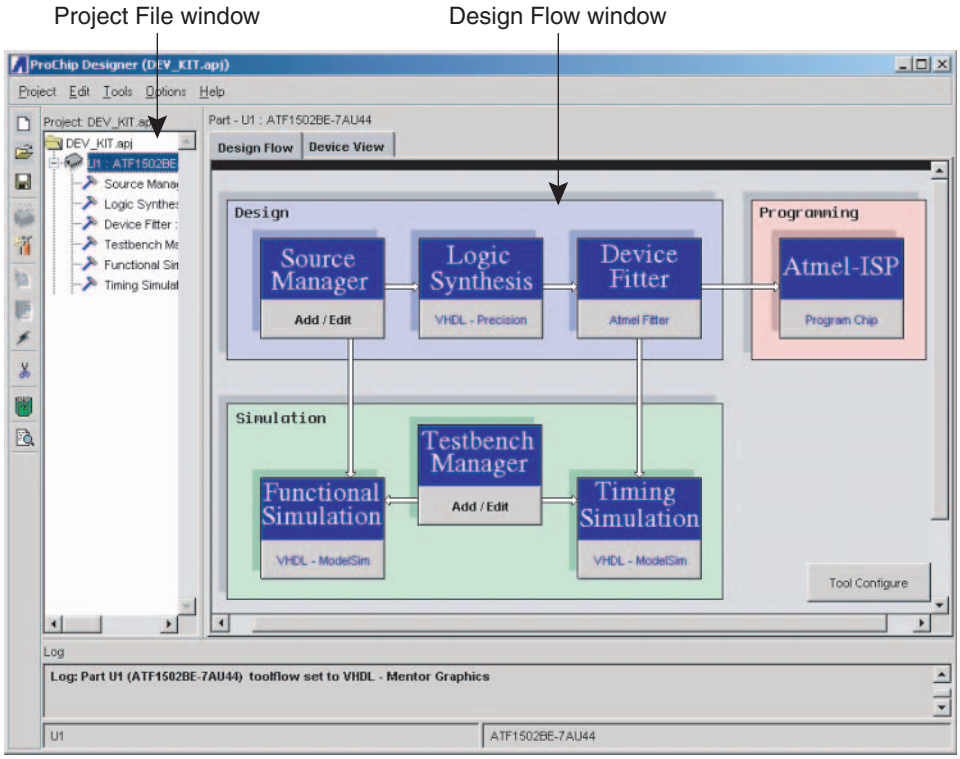
This closes the New Project Wizard and opens the ProChip Designer window. The sources in the project are shown in the left window.



(10) Select **Finish** to end the New Project Wizard

11. Click on the **ATF1502BE-7AU44** device icon to view the Design Flow window.

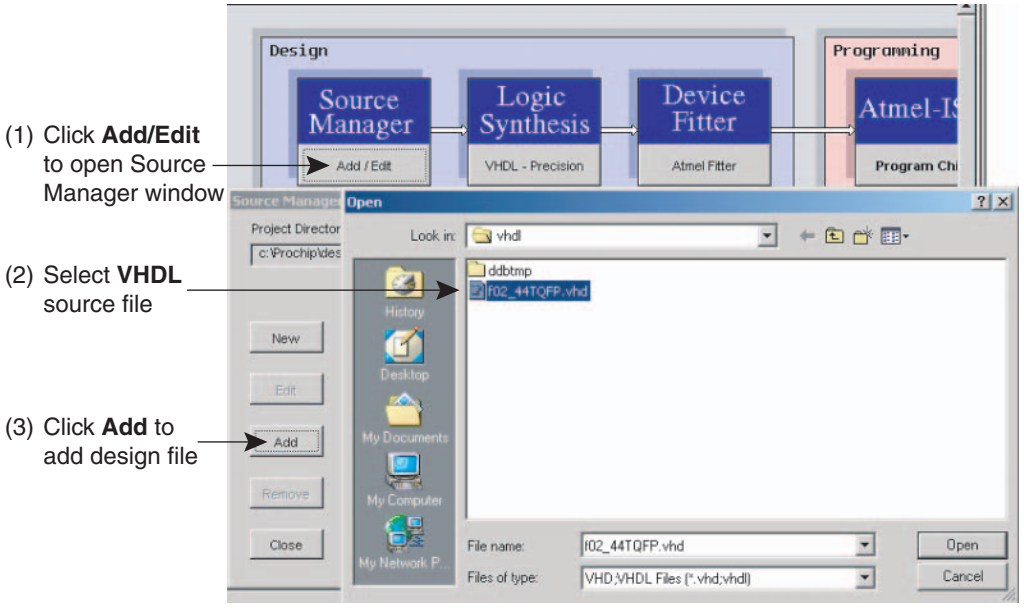




3.2 Add a Design File

Once the project file is created, the next step is to add the design source file(s) into your project. For this tutorial, a single VHDL design file will be added into the project.

1. Click on the **Add/Edit** button from Source Manager to open the Source Manager window. You can view the Source Manager help file by clicking on the **Help** button within the Source Manager window to view the description for the different processes.
2. In the Source Manager window, click on the **Add** button to add a VHDL design file to the project.
3. In the File Manager window, select **.VHD** from the C:\PROCHIP\DESIGNS\VHDL directory as the source design file for this project.



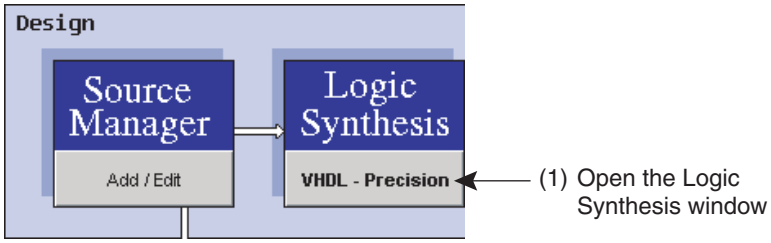
This VHDL design is available at the end of this document.

The F02_44TQFP.VHD file is a VHDL design that uses two 7-segment displays and the built-in oscillator on the Atmel ATF15xx-DK3 CPLD Development/Programmer Board to generate two scrolling “0” characters. This design will also pass the states of the I/O push-button switches (SW1-SW4) to the LEDs at LED1-LED4 on the ATF15xx-DK3 CPLD Development/Programmer Board. For details, please review the VHDL code.

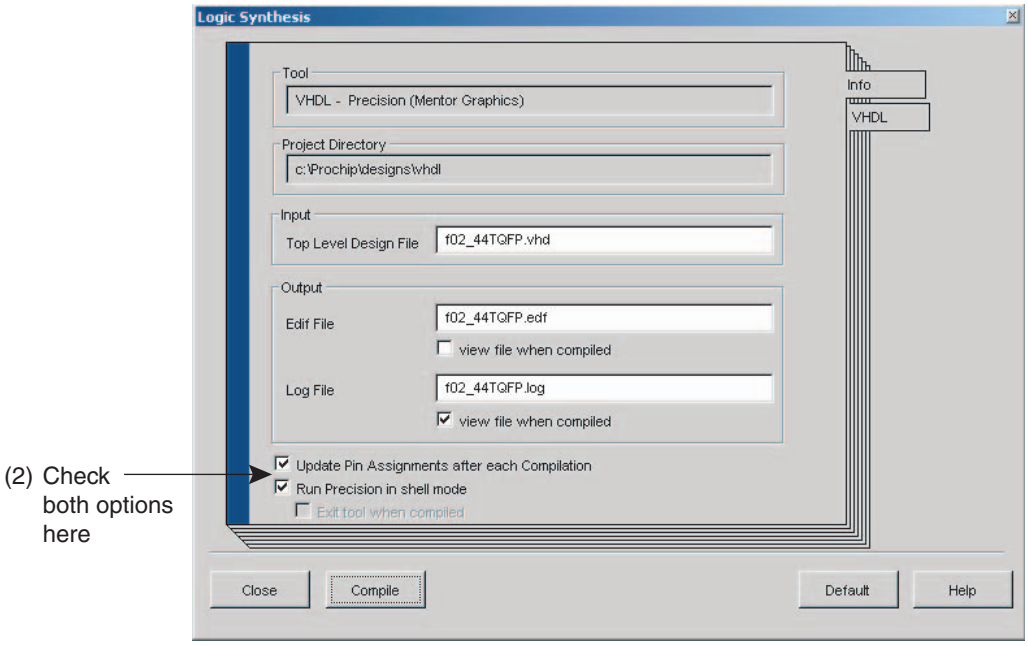
3.3 Synthesize the VHDL Design

In this part of the tutorial, the VHDL design code will be synthesized through the Mentor Graphics Precision Synthesis process into an EDIF netlist (*.EDF), which contains a set of optimized/minimized logic equations for the specified CPLD.

1. Click on the **VHDL - Precision** button in the Design Flow window to open the Logic Synthesis window.



2. In the Logic Synthesis window, check both options to **Update Pin Assignments after each Compilation** and also **Run Precision in shell mode**:



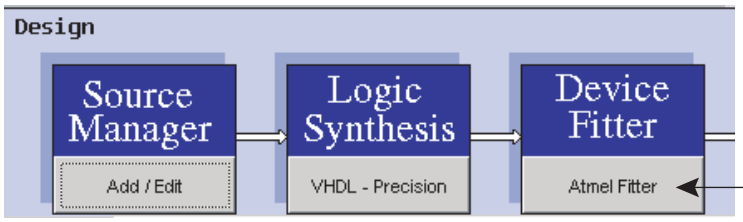
3. Click on the **Compile** button to start the compile process. Close the log file when the synthesis is done successfully.

Note: If you have encountered any syntax error during synthesis, the report file will pop up to indicate which line of the code contains problem. In such case, you must correct the syntax problem and save the file before synthesize the code again before proceeding to the next step.

3.4 Fit the Synthesized Design File

In Section 3.3, the logic synthesis portion of the CPLD design flow was completed. On successful compilation, the Precision tool will produce an EDIF output file (with .EDF extension). An EDIF file contains the netlist of the optimized and minimized logic equations. We now need to map this netlist into a specific Atmel CPLD architecture using the Atmel Fitter.

1. You can now proceed to the device fitter portion of the design flow by clicking on the **Atmel Fitter** button.

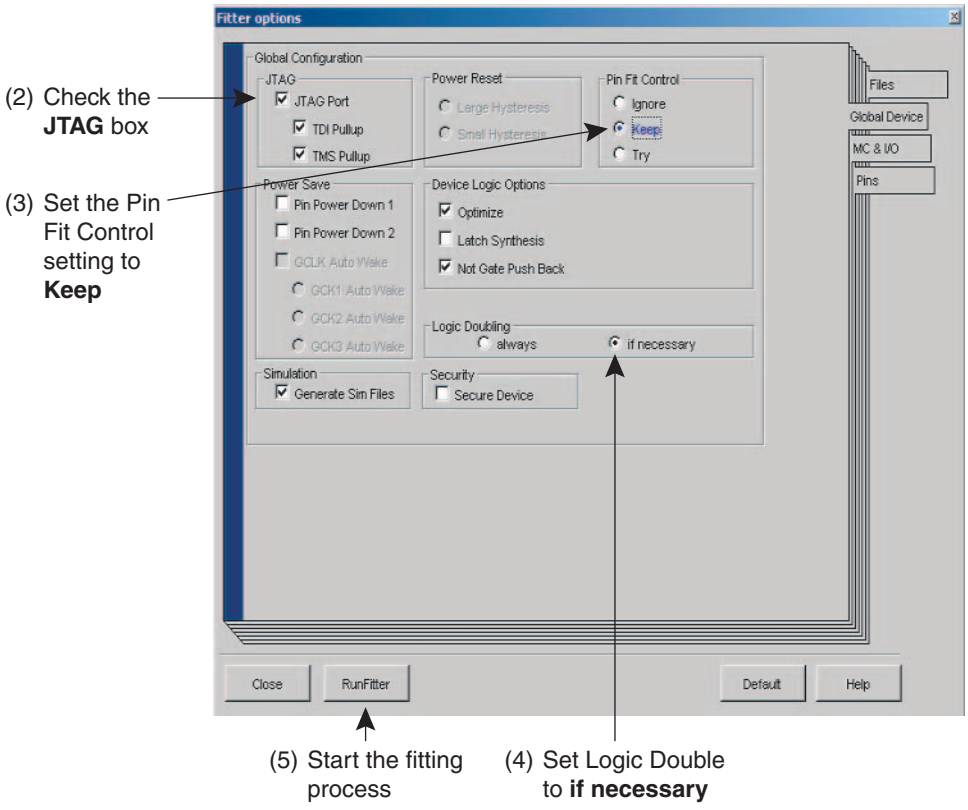


You can either use the default options or specify fitter properties. ProChip Designer will automatically select the EDIF file (*.EDF) associated to the current design project and the tool type. In this example, since our target device is an ATF1502BE, we will select the **FIT1502.EXE** device fitter.

The fitter creates the important JEDEC and Fit Report output files. They contain the data for programming the device (using in-system programming or on a third-party device programmer) and the pin assignments required for board layout respectively.

Please review the Global Device Parameters and Pin/Node Options as well. The help files also show the Device Pin_Node lists for each of the Atmel CPLDs.

2. Make sure the **JTAG** box is checked. This enables the JTAG port for ISP programming.
3. Make sure the Pin Fit Control setting is set to **Keep**. This will ensure that the pin assignments in the PLD file will be kept during the place-and-route process.
4. Make sure the Logic Double setting is set to **if necessary**.
5. When all the fitter options are set, click on the **Run Fitter** button to fit the design.



The above message will be displayed after the design is successfully fit the selected device.

If there are any error messages, you can review the exported *.FIT file or you can copy your *.EDF file to the C:\PROCHIP\PLDFIT\ directory, open the DOS command prompt, and then type the fit command that is starting from the second line of the *.FIT file to see more details about the fitter errors.

Parts of the fitter report (.FIT) file generated for this design is shown below.

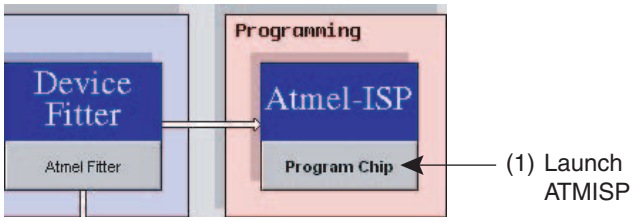
```
Total dedicated input used:   3/4     (75%)
Total I/O pins used           24/32   (75%)
Total Macro cells used        35/32   (109%)
Total Flip-Flop used          28/32   (87%)
Total Foldback logic used     15/32   (46%)
Total Nodes+FB/MCells         50/32   (156%)
Total cascade used            0
Total input pins              10
Total output pins             17
Total Pts                     93
Creating pla file c:\Prochip\designs\vhdl\f02_44TQFP.tt3 with 0 inputs 0
outputs, 0 pins 0 nodes and 0 pterms...

----------------  End fitter, Design FITS
$Device TQFP44 fits
FIT1502 completed in 0.00 seconds
```

3.5 Program and Verify Design

In this step of the tutorial, you will program an ATF1502BE 44-pin TQFP device on the Atmel ATF15xx-DK3 CPLD Development/Programmer Board through ISP. Then you will be able to verify the design by observing the four 7-segment displays and four LEDs on the CPLD Development/Programmer Board.

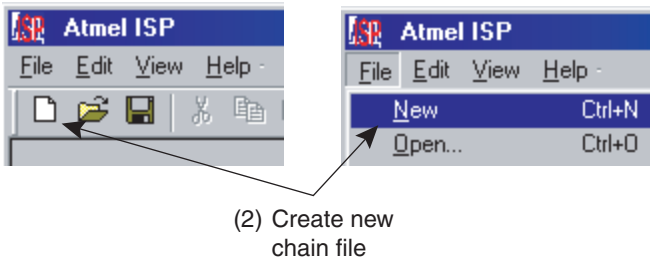
You will need to follow the steps below to setup the ATMISP software (V6.0 or latest version) in order to program the ATF1502BE 44-pin TQFP on the ATF15xx-DK3 CPLD Development/Programmer Board.

1. To create a new chain file, the ATMISP Software first needs to be launched either through the **Program Chip** button in the ProChip Designer window, the **ATMISP** desktop icon or the **Start** > **Programs** > **Atmel-ISP** menu.

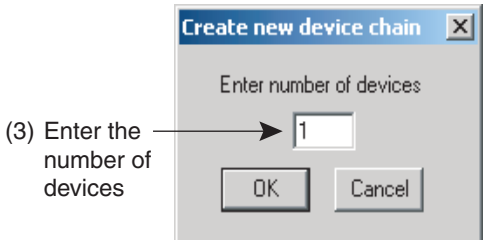


Note: If ATMISP is launched through ProChip Designer, then the appropriate chain (.CHN) file will be automatically created by ProChip Designer. Therefore, steps 2 through 6 can be skipped.

2. To create a new chain file, select the **New** command under the File menu or click on the **New** shortcut button.

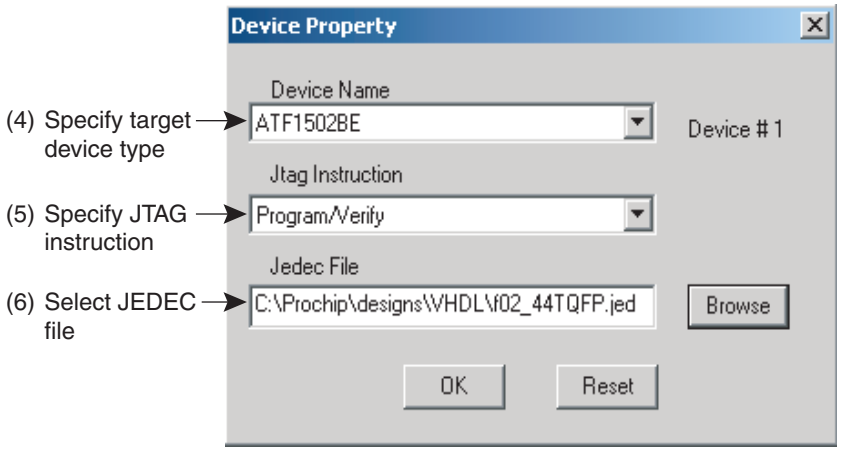


3. The first piece of information that the software asks for when creating a new chain is the number of devices in the JTAG chain. Therefore, enter “1” and then click **OK** since you will be programming a single-device JTAG chain.



4. Next you will need to specify the properties of each JTAG device in the Device Properties window. First, you will need to select the target device type of the first device in the JTAG chain. For this tutorial, please select **ATF1502BE** as the target device type.
5. In the JTAG Instruction field, you can specify which JTAG instruction to be executed on this device in the chain. Please select **Program/Verify** to program and verify the ATF1502BE.
6. The next step is to specify the JEDEC file to be programmed into the target device in the JEDEC File field. Click on the **Browse** button, change the directory to **..\PROCHIP\DESIGNS\VHDL** and then select **F02_44TQFP.JED** as the

JEDEC file. Click **OK** to close the JTAG Device Properties window when all properties are specified.



The next step requires you to setup the Atmel ATF15xx-DK3 CPLD Development/Programmer Board to program the ATF1502BE-7AU44 through the CPLD ISP cable.

7. Connect the DB25 side of the Atmel CPLD ISP MV cable (Revision 6) to the PC's parallel port and the 10-pin header side of the cable to the Atmel ATF15xx-DK3 CPLD Development Board as shown Figure 2-10 on page 2-14.
8. Connect a 9V AC/DC power supply to the power connector (JPower) of the Atmel ATF15xx-DK3 CPLD Development/Programmer Board.
9. Set the VCCIO Selector jumper to the 1.8V(BE) position for supplying the core voltage of the ATF1502BE device at 1.8V, then set the VCCINT Selector jumper to the 1.8V(BE) position for supplying the I/O pad voltage of the ATF1502BE device at 1.8V.

Note: Make sure the ICCINT and ICCIO jumpers are in their default positions. These two jumpers are only removed when you are connecting them from two poles of the digital multimeter to perform current measurement.

10. Set the JPCLK jumper to GCLK1 so that the output of the crystal oscillator will go to pin 37 (GCLK1) of the ATF1502BE. For this design, you can also set the JPCLK jumper to GCLK2 so that the output of the crystal oscillator will go to pin 40 (GCLK2) of the ATF1502BE for selecting another global clock source.
11. Set the JPJTAG Jumper ISP Cable position, which is toward the middle of the board.
12. Connect the 44-pin TQFP Socket Adapter Board onto the main development/programmer board.

Note: If a device in a different package type is to be programmed, then the appropriate Socket Adapter Board must be used.

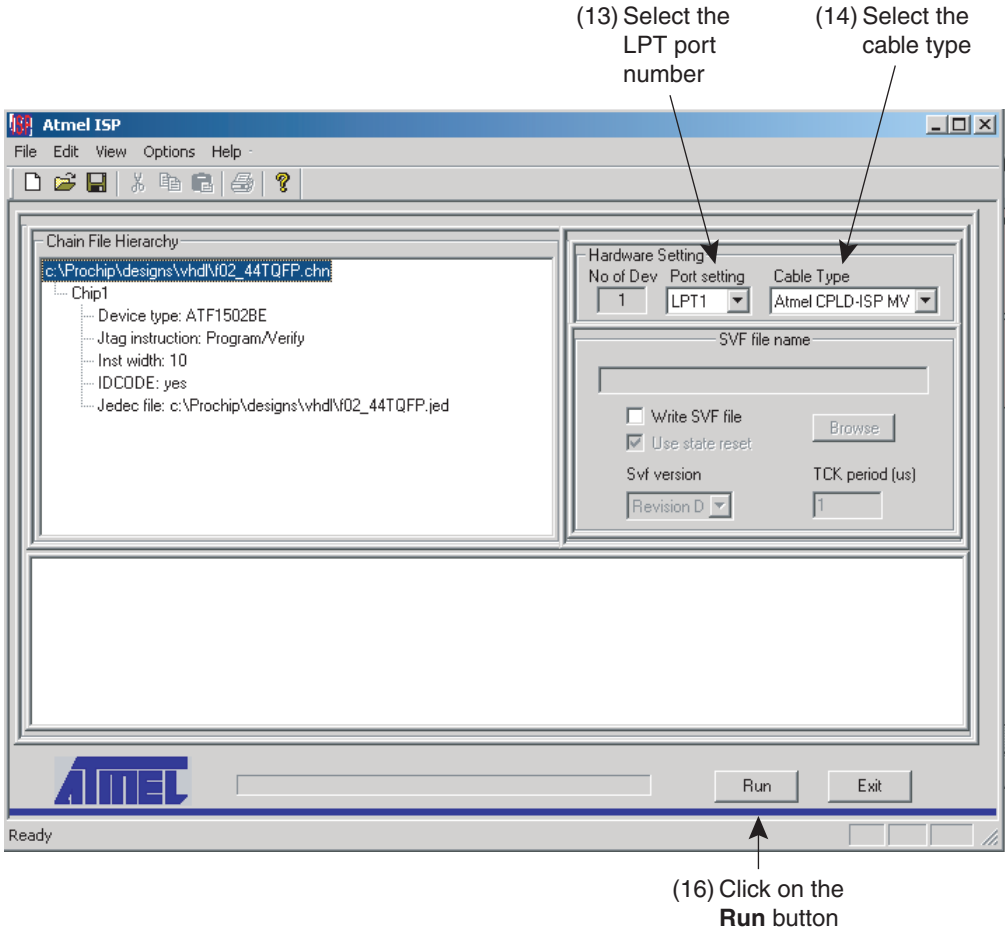
13. Select which LPT port is being used for Atmel CPLD ISP cable in the Port Setting field. LPT1 is the default port and it represents address 0x378.
14. Select the ISP download cable type in the Cable Type field. The default cable type is the "Atmel CPLD-ISP MV", which represents the Atmel CPLD ISP Cable Rev 6.0, but it can be changed to other cables that can be used for other devices.

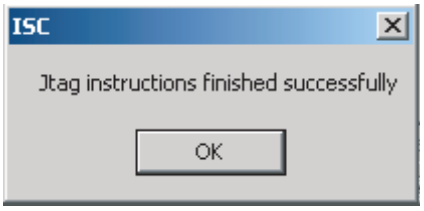
Note: The "Atmel CPLD-ISP" cable type represents the Atmel CPLD ISP Cable Rev 5.0 or older.

15. Switch the power switch to the ON position.

Now both your software and hardware are setup for ISP programming and you can execute the Program/Verify instruction to program the ATF1502BE on the Atmel ATF15xx-DK3 CPLD Development/Programmer Board.

16. Click on the **Run** button in the ATMISP main window to execute the JTAG instruction to program the ATF1502BE on ATF15xx-DK3 CPLD Development/Programmer Board.





If you do not see above message after programming of the device, please review the troubleshooting guide and FAQs from the Atmel-ISP software to debug the problem.

After successfully programming the ATF1502BE with the F02_144TQFP.JED file, the first and fourth 7-segment LED displays should show two rotating “0” characters. In addition, with the setting of the LED jumpers (JPL1, JPL2, JPL3, and JPL4) and push-button jumpers (JPS8, JPS7, JPS6, and JPS5), you can press SW8, SW7, SW6, or SW5 to light up LEDs 1-4.

If the result is displayed correctly on the ATF15xx-DK3 CPLD Development/Programmer Board, then you have successfully completed this tutorial.

Section 4

Schematic Diagrams and VHDL File

Figure 4-1. ATF15xx-D3 Development/Programmer Board Schematic Diagram

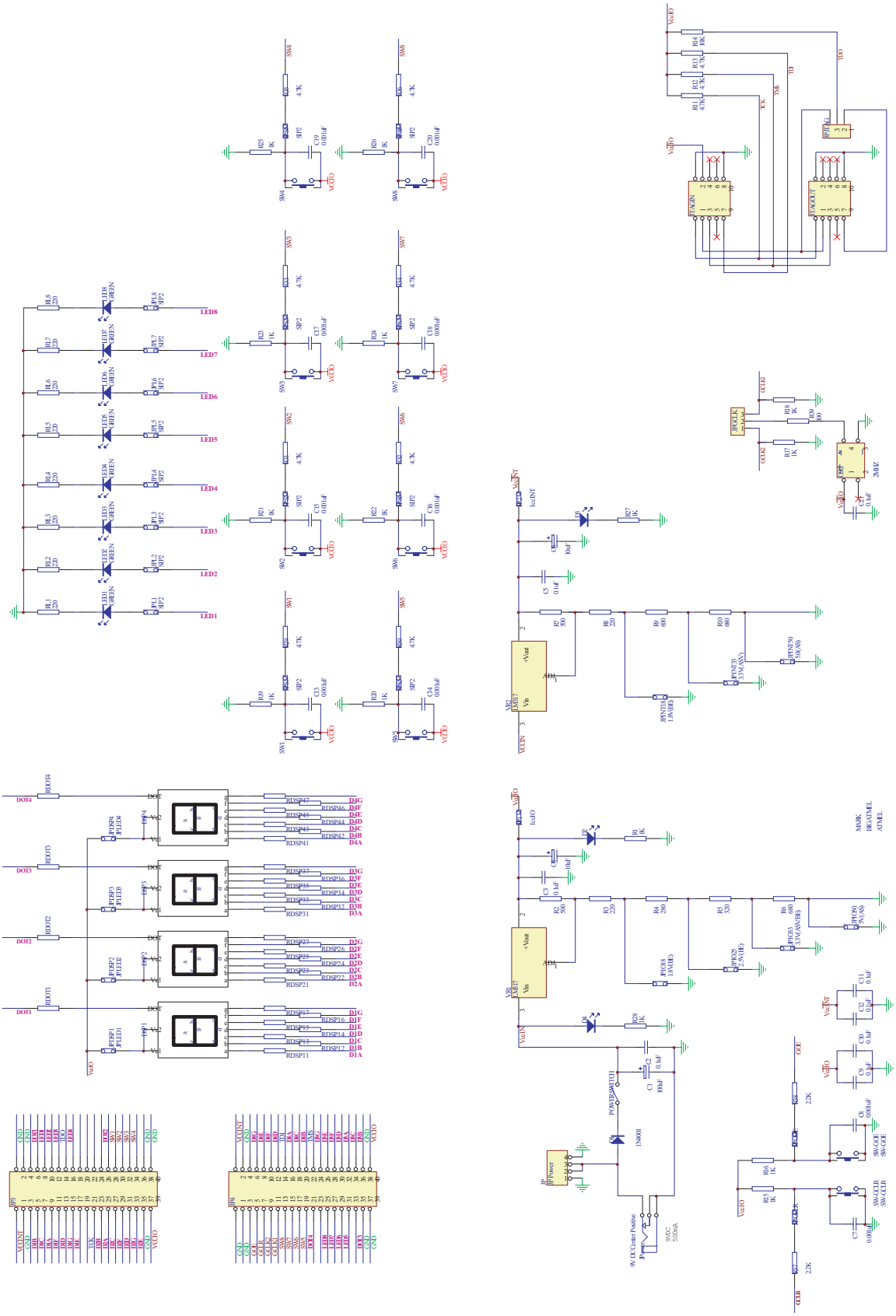


Figure 4-2. 44-pin TQFP Socket Adapter Board Schematic Diagram

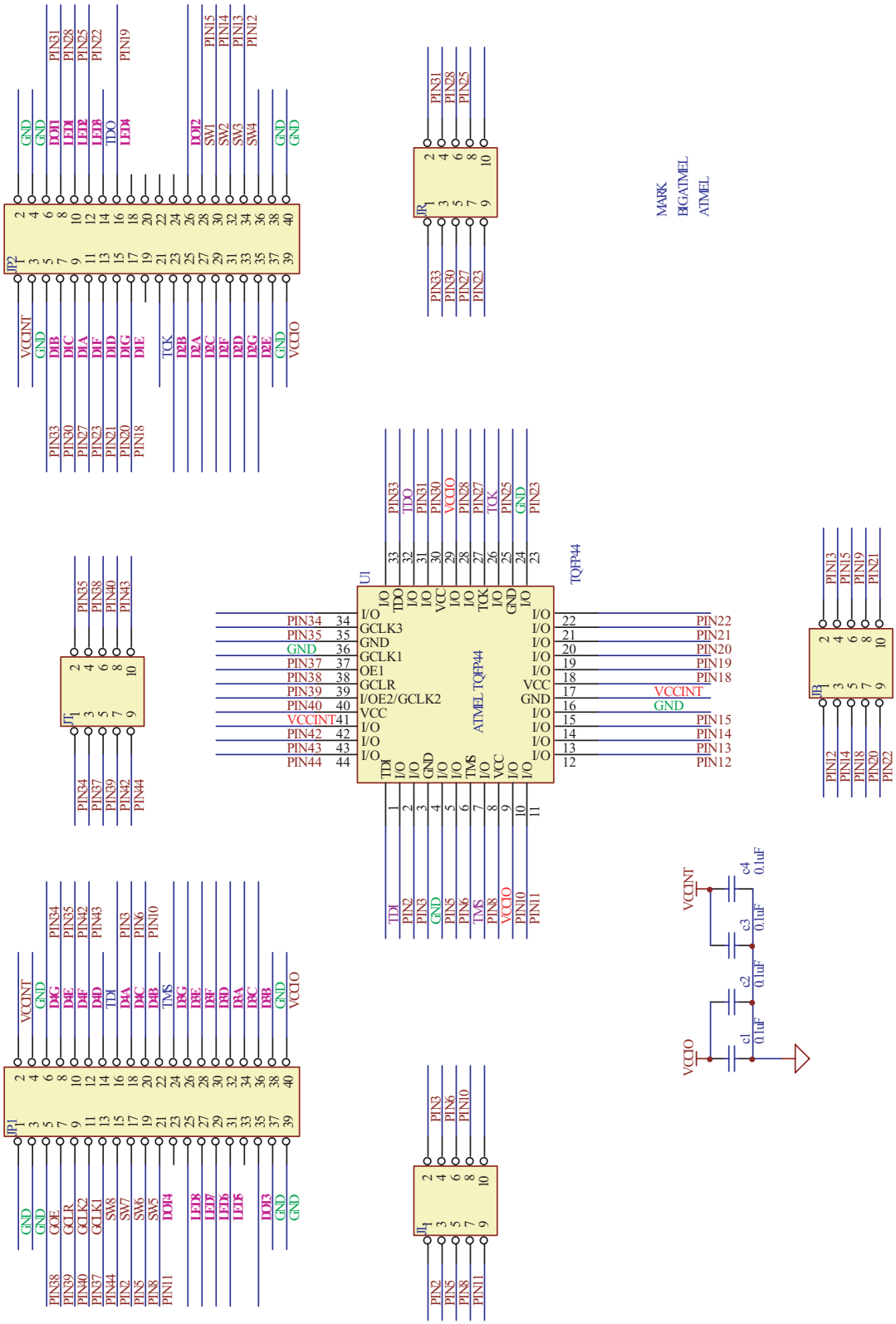


Figure 4-3. 44-pin PLCC Socket Adapter Board Schematic Diagram

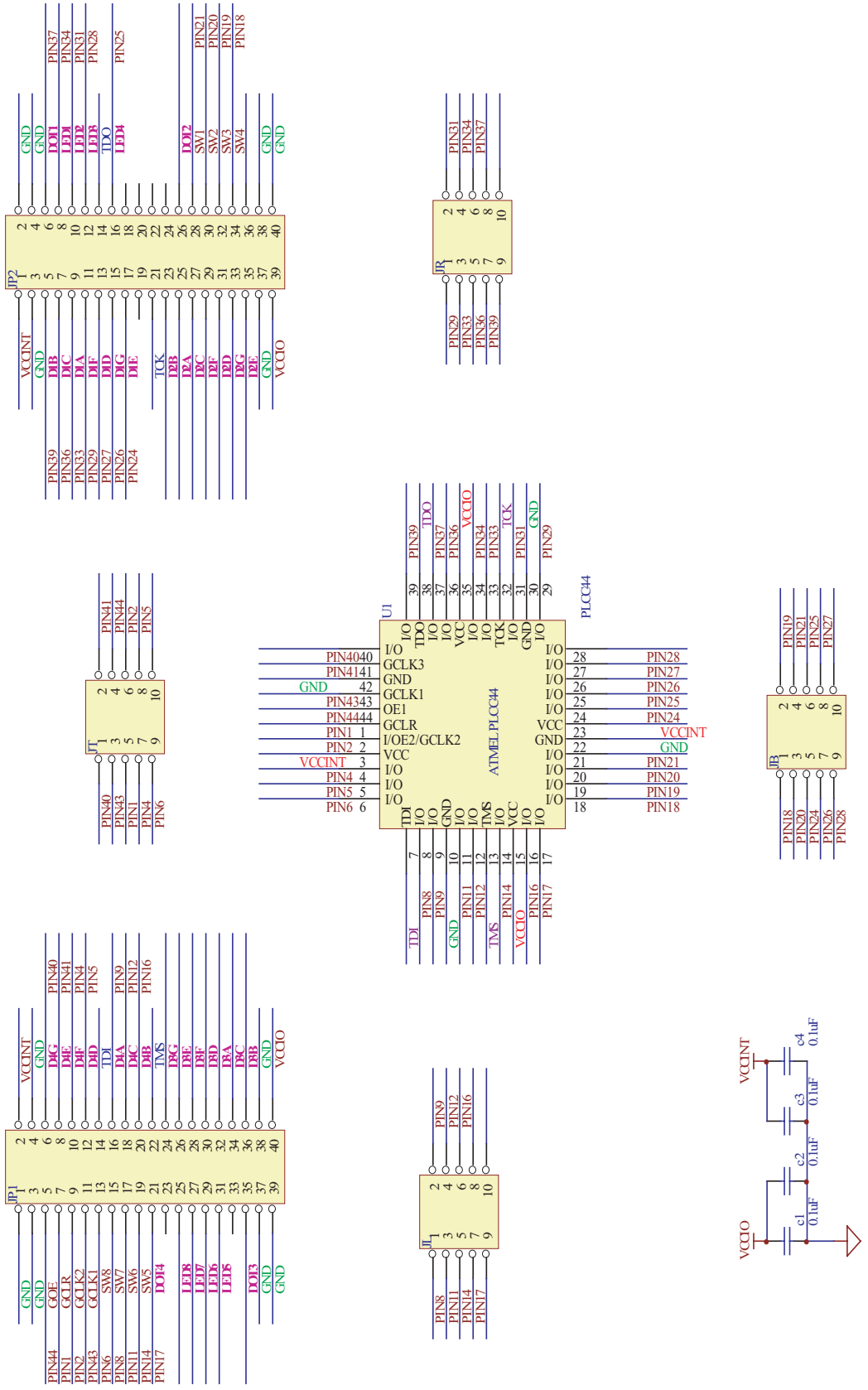


Figure 4-4. 84-pin PLCC Socket Adapter Board Schematic Diagram

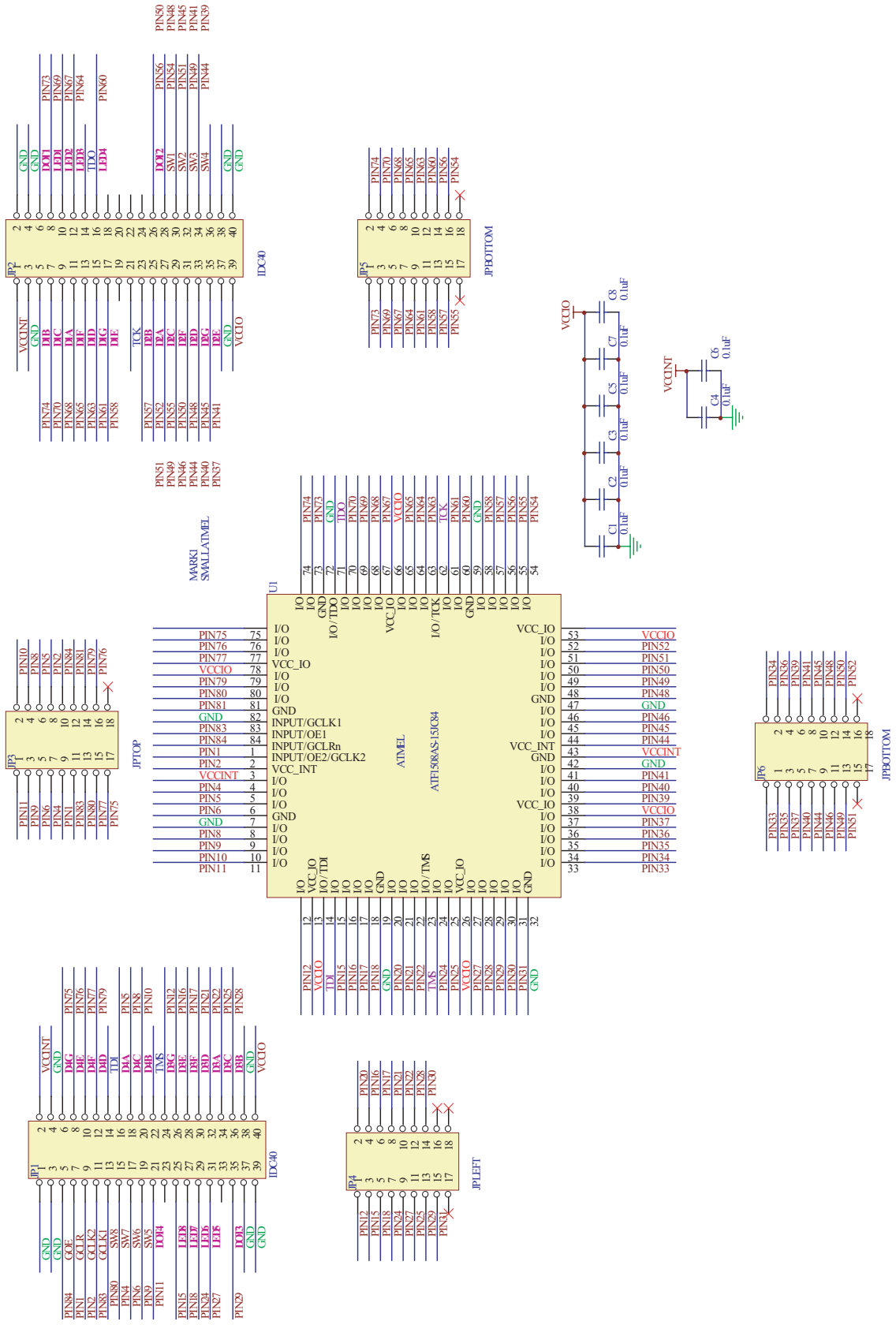
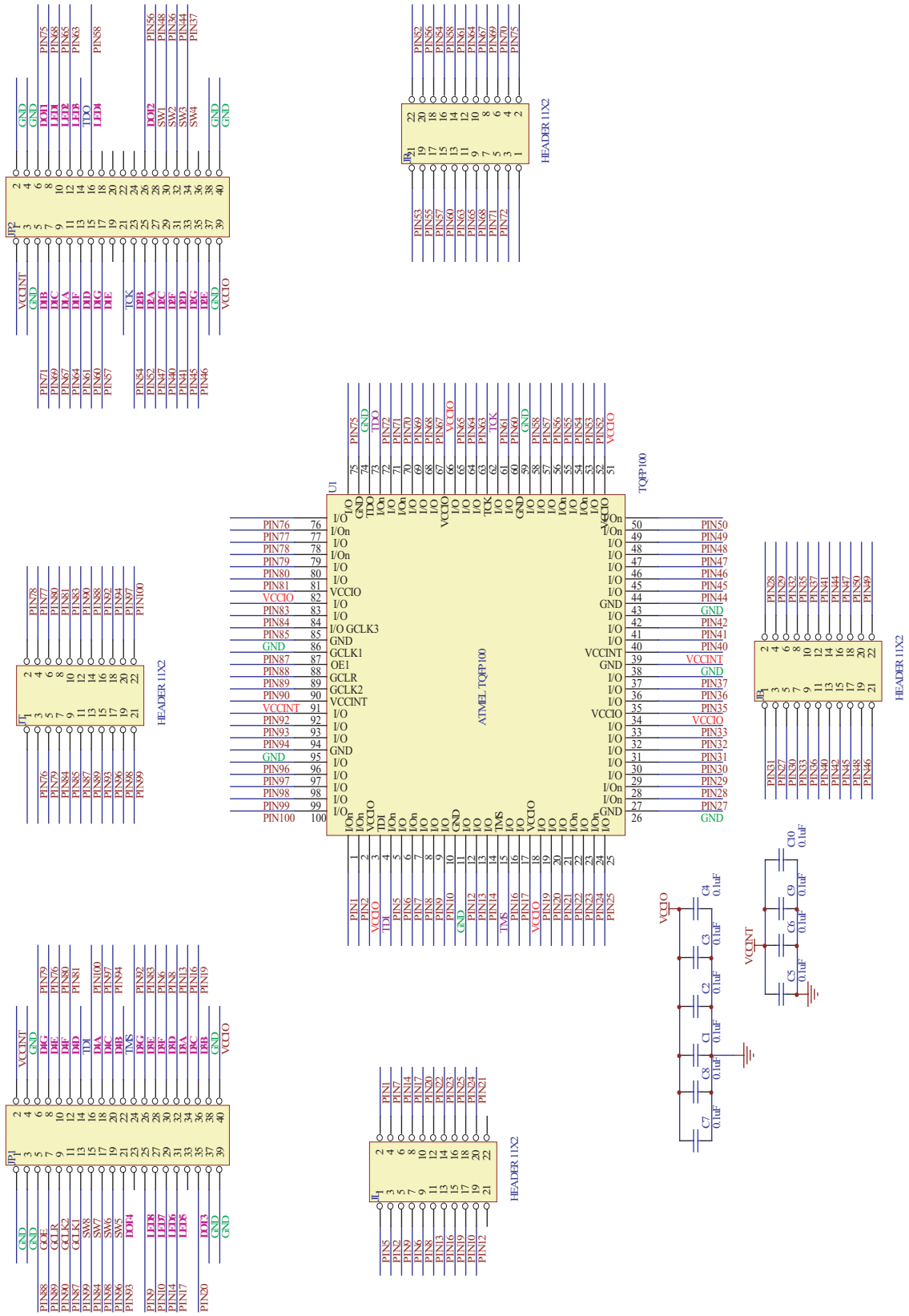


Figure 4-5. 100-pin TQFP Socket Adapter Board Schematic Diagram



```
--------------------------------------------------------------------------------
-- Library Declaration
--------------------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.all, IEEE.NUMERIC_STD.all;

--------------------------------------------------------------------------------
-- Entity Declaration
--------------------------------------------------------------------------------

entity f02_44TQFP is
    port
    (
        GCLK1   : in std_logic;                                 -- 2MHz clock (positive edge)
        GCLK2   : in std_logic;                                 -- 2MHz clock (negative edge)
        GCLR    : in std_logic;                                 -- Register reset
        SW          : in std_logic_vector(8 downto 5);-- Switches
        DSP1    : inout std_logic_vector(5 downto 0);-- 7-segment display LEDs (F to A)
        DSP4    : inout std_logic_vector(5 downto 0);-- 7-segment display LEDs (F to A)
        LED     : out std_logic_vector(4 downto 1)-- LEDs
    );

--------------------------------------------------------------------------------
-- Pin Assignment
--------------------------------------------------------------------------------

    attribute pinnum: string;
    attribute pinnum of GCLK1: signal is"37";
    attribute pinnum of GCLK2: signal is"40";
    attribute pinnum of GCLR: signal is"39";
    attribute pinnum of SW: signal is"12,13,14,15";
    attribute pinnum of DSP1: signal is"23,18,21,30,33,27";
    attribute pinnum of DSP4: signal is"42,35,43,6,10,3";
    attribute pinnum of LED: signal is"19,22,25,28";

end entity f02_44TQFP;

--------------------------------------------------------------------------------
-- Architecture
--------------------------------------------------------------------------------

architecture LOGIC of f02_44TQFP is

--------------------------------------------------------------------------------
-- Internal Signal Declaration
--------------------------------------------------------------------------------

    signal CNT1: unsigned(15 downto 0);
    signal iCLK : std_logic;
```

```
begin

    iCLK <= GCLK1 or GCLK2;

-------------------------------------------------------------------------------
-- Frequency Divider
-------------------------------------------------------------------------------

    FREQ_DIV1 : process (iCLK,GCLR)
    begin
        if (GCLR = '0') then
            CNT1 <= (others => '0');
        elsif (rising_edge(iCLK)) then
            CNT1 <= CNT1 + 1;
        end if;
    end process;

-------------------------------------------------------------------------------
-- LED Control
-------------------------------------------------------------------------------

    LED_CTL : process (SW)

    begin
            LED(1) <= SW(5);
            LED(2) <= SW(6);
            LED(3) <= SW(7);
            LED(4) <= SW(8);
    end process;

-------------------------------------------------------------------------------
-- DSP Control
-------------------------------------------------------------------------------

    DSP_CTL : process (CNT1(15), GCLR)

    begin
        if (GCLR = '0') then
            DSP1 <= (others => '0');
            DSP4 <= (others => '0');
        elsif rising_edge(CNT1(15)) then
            DSP1(0) <= not DSP1(5);
            DSP1(1) <= DSP1(0);
            DSP1(2) <= DSP1(1);
            DSP1(3) <= DSP1(2);
            DSP1(4) <= DSP1(3);
            DSP1(5) <= DSP1(4);

            DSP4(0) <= not DSP4(5);
```

```
            DSP4(1) <= DSP4(0);
            DSP4(2) <= DSP4(1);
            DSP4(3) <= DSP4(2);
            DSP4(4) <= DSP4(3);
            DSP4(5) <= DSP4(4);
        end if;
    end process;

end architecture LOGIC;
```

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