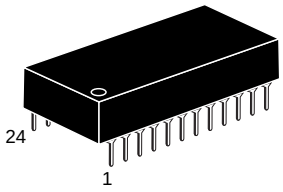
# M48Z02
# M48Z12

## 16 Kbit (2Kb x 8) ZEROPOWER® SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES ($V_{PFD}$ = Power-fail Deselect Voltage):
  - M48Z02: 4.50V ≤ $V_{PFD}$ ≤ 4.75V
  - M48Z12: 4.20V ≤ $V_{PFD}$ ≤ 4.50V
- SELF-CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs




PCDIP24 (PC)
Battery CAPHAT

### DESCRIPTION

The M48Z02/12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and functional compatible with the DS1220.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02/12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

The M48Z02/12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

**Table 1. Signal Names**

| | |
|---|---|
| A0-A10 | Address Inputs |
| DQ0-DQ7 | Data Inputs / Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 1. Logic Diagram**

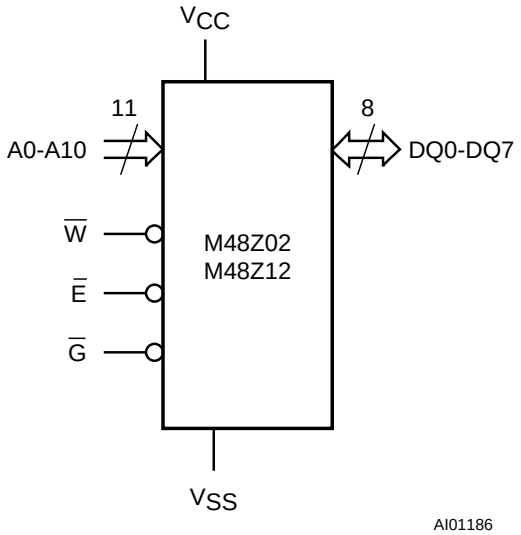


**Table 2. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | –40 to 85 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$ Off) | –40 to 85 | °C |
| $T_{SLD}$ (2) | Lead Solder Temperature for 10 seconds | 260 | °C |
| $V_{IO}$ | Input or Output Voltages | –0.3 to 7 | V |
| $V_{CC}$ | Supply Voltage | –0.3 to 7 | V |
| $I_O$ | Output Current | 20 | mA |
| $P_D$ | Power Dissipation | 1 | W |

**Notes:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

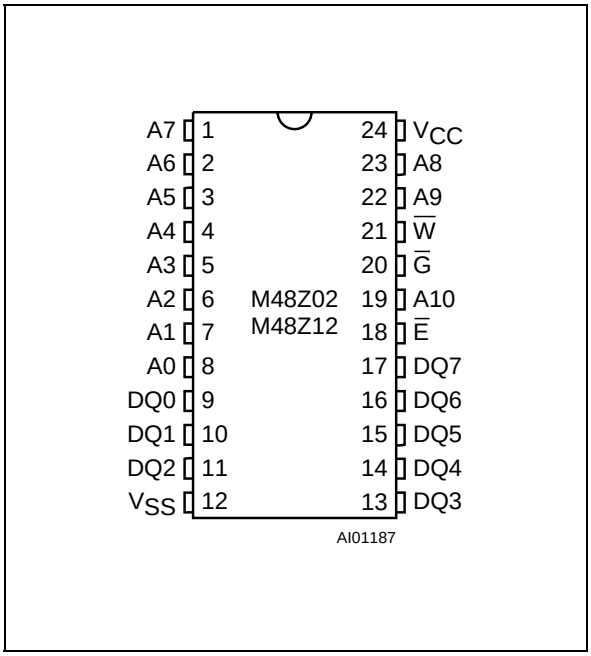
***CAUTION:*** *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

**Table 3. Operating Modes**

| Mode | $V_{CC}$ | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | DQ0-DQ7 | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.75V to 5.5V or 4.5V to 5.5V | $V_{IH}$ | X | X | High Z | Standby |
| Write | | $V_{IL}$ | X | $V_{IL}$ | $D_{IN}$ | Active |
| Read | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | Active |
| Read | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High Z | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min) | X | X | X | High Z | CMOS Standby |
| Deselect | $\leq V_{SO}$ | X | X | X | High Z | Battery Back-up Mode |

**Notes**: X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage.

**Figure 2. DIP Pin Connections**

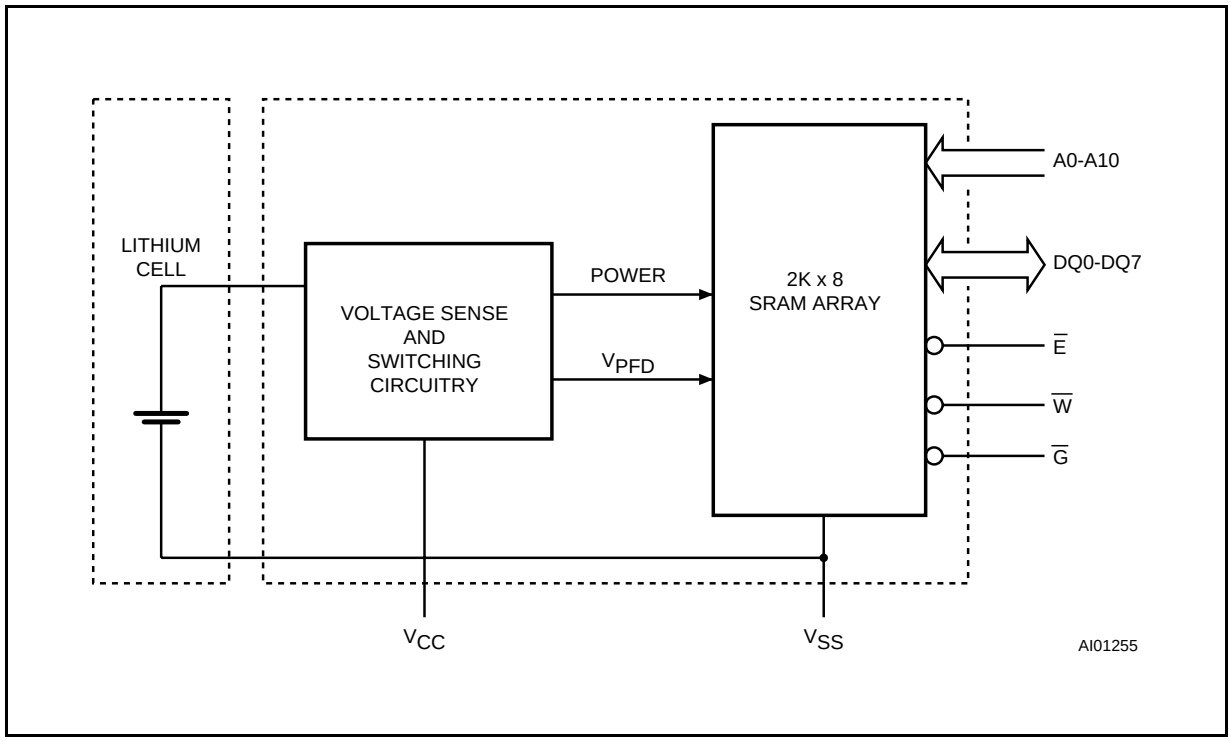



## DESCRIPTION (cont'd)

The M48Z02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z02/12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When $V_{CC}$ is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low $V_{CC}$. As $V_{CC}$ falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

**Figure 3. Block Diagram**




## READ MODE

The M48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time ($t_{AVQV}$) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time ($t_{ELQV}$) or Output Enable Access time ($t_{GLQV}$).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before $t_{AVQV}$, the data lines will be driven to an indeterminate state until $t_{AVQV}$. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time ($t_{AXQX}$) but will go indeterminate until the next Address Access.

**Table 4. AC Measurement Conditions**

| | |
|---|---|
| Input Rise and Fall Times | ≤ 5ns |
| Input Pulse Voltages | 0V to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Figure 4. AC Testing Load Circuit**

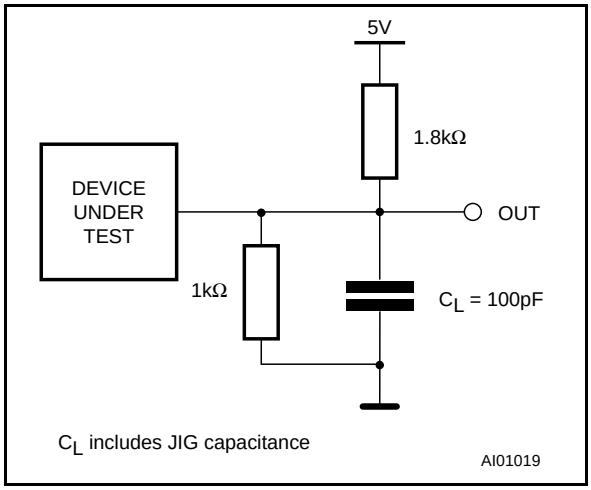


**Table 5. Capacitance (1)**
($T_A$ = 25 °C)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 10 | pF |
| $C_{IO}$ (2) | Input / Output Capacitance | $V_{OUT}$ = 0V | | 10 | pF |

**Notes:** 1. Effective capacitance measured with power supply at 5V.
2. Outputs deselected

**Table 6. DC Characteristics**
($T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.75V to 5.5V or 4.5V to 5.5V)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ (1) | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | ±1 | µA |
| $I_{LO}$ (1) | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | ±5 | µA |
| $I_{CC}$ | Supply Current | Outputs open | | 80 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | 3 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E} = V_{CC} - 0.2V$ | | 3 | mA |
| $V_{IL}$ (2) | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –1mA | 2.4 | | V |

**Notes:** 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per cycle.

**Table 7. Power Down/Up Trip Points DC Characteristics (1)**
($T_A$ = 0 to 70°C or –40 to 85°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage (M48Z02) | 4.5 | 4.6 | 4.75 | V |
| $V_{PFD}$ | Power-fail Deselect Voltage (M48Z12) | 4.2 | 4.3 | 4.5 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | | 3.0 | | V |
| $t_{DR}$ | Expected Data Retention Time | 10 | | | YEARS |

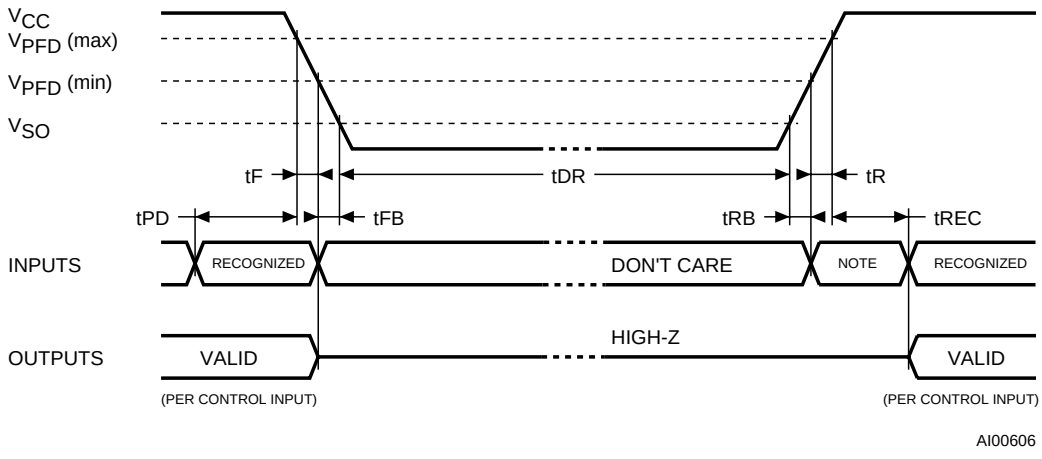
**Note:** 1. All voltages referenced to $V_{SS}$.

**Table 8. Power Down/Up Mode AC Characteristics**
($T_A$ = 0 to 70°C or –40 to 85°C)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PD}$ | $\overline{E}$ or $\overline{W}$ at $V_{IH}$ before Power Down | 0 | | µs |
| $t_F$ (1) | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | 300 | | µs |
| $t_{FB}$ (2) | $V_{PFD}$ (min) to $V_{SO}$ $V_{CC}$ Fall Time | 10 | | µs |
| $t_R$ | $V_{PFD}$(min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | 0 | | µs |
| $t_{RB}$ | $V_{SO}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | 1 | | µs |
| $t_{REC}$ | $\overline{E}$ or $\overline{W}$ at $V_{IH}$ after Power Up | 2 | | ms |

**Notes**: 1. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than $t_F$ may result in deselection/write protection not occurring until 50 µs after $V_{CC}$ passes $V_{PFD}$ (min).
2. $V_{PFD}$ (min) to $V_{SO}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.

**Figure 5. Power Down/Up Mode AC Waveforms**

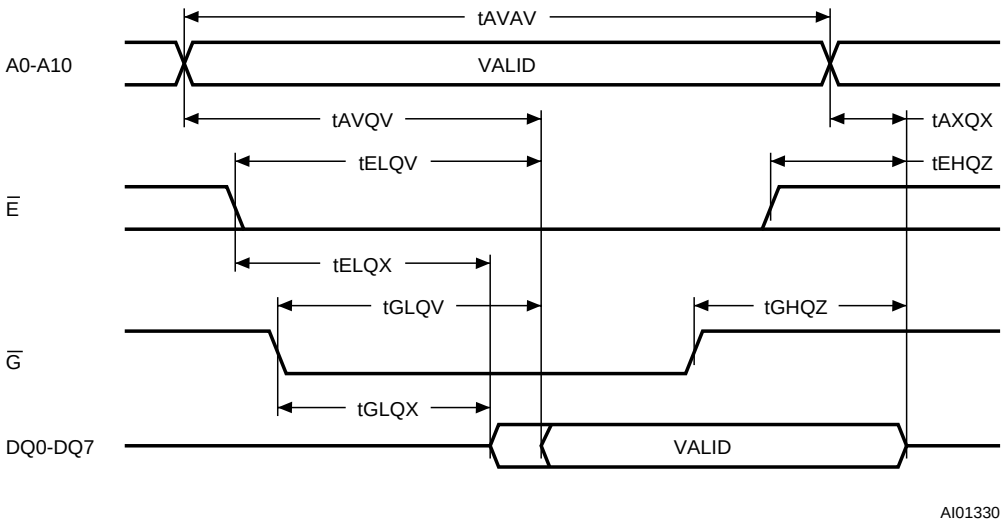



**Note:** Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as $V_{CC}$ rises past $V_{PFD}$(min). Some systems may perform inadvertent write cycles after $V_{CC}$ rises above $V_{PFD}$(min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.

**Table 9. Read Mode AC Characteristics**
($T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.75V to 5.5V or 4.5V to 5.5V)

| Symbol | Parameter | M48Z02 / M48Z12 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -70 | | -150 | | -200 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | Read Cycle Time | 70 | | 150 | | 200 | | ns |
| $t_{AVQV}$ | Address Valid to Output Valid | | 70 | | 150 | | 200 | ns |
| $t_{ELQV}$ | Chip Enable Low to Output Valid | | 70 | | 150 | | 200 | ns |
| $t_{GLQV}$ | Output Enable Low to Output Valid | | 35 | | 75 | | 80 | ns |
| $t_{ELQX}$ | Chip Enable Low to Output Transition | 5 | | 10 | | 10 | | ns |
| $t_{GLQX}$ | Output Enable Low to Output Transition | 5 | | 5 | | 5 | | ns |
| $t_{EHQZ}$ | Chip Enable High to Output Hi-Z | | 25 | | 35 | | 40 | ns |
| $t_{GHQZ}$ | Output Enable High to Output Hi-Z | | 25 | | 35 | | 40 | ns |
| $t_{AXQX}$ | Address Transition to Output Transition | 10 | | 5 | | 5 | | ns |

**Figure 6. Read Mode AC Waveforms**




**Note:** Write Enable ($\overline{W}$) = High.

**Table 10. Write Mode AC Characteristics**
($T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 4.75V to 5.5V or 4.5V to 5.5V)

| Symbol | Parameter | M48Z02 / M48Z12 | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -70 | | -150 | | -200 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | Write Cycle Time | 70 | | 150 | | 200 | | ns |
| $t_{AVWL}$ | Address Valid to Write Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{WLWH}$ | Write Enable Pulse Width | 50 | | 90 | | 120 | | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 55 | | 90 | | 120 | | ns |
| $t_{WHAX}$ | Write Enable High to Address Transition | 0 | | 10 | | 10 | | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 0 | | 10 | | 10 | | ns |
| $t_{DVWH}$ | Input Valid to Write Enable High | 30 | | 40 | | 60 | | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 30 | | 40 | | 60 | | ns |
| $t_{WHDX}$ | Write Enable High to Input Transition | 5 | | 5 | | 5 | | ns |
| $t_{EHDX}$ | Chip Enable High to Input Transition | 5 | | 5 | | 5 | | ns |
| $t_{WLQZ}$ | Write Enable Low to Output Hi-Z | | 25 | | 50 | | 60 | ns |
| $t_{AVWH}$ | Address Valid to Write Enable High | 60 | | 120 | | 140 | | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 60 | | 120 | | 140 | | ns |
| $t_{WHQX}$ | Write Enable High to Output Transition | 5 | | 10 | | 10 | | ns |

**WRITE MODE**

The M48Z02/12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of $t_{EHAX}$ from Chip Enable or $t_{WHAX}$ from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid $t_{DVWH}$ prior to the end of write and remain valid for $t_{WHDX}$ afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs $t_{WLQZ}$ after $\overline{W}$ falls.

**Figure 7. Write Enable Controlled, Write AC Waveforms**

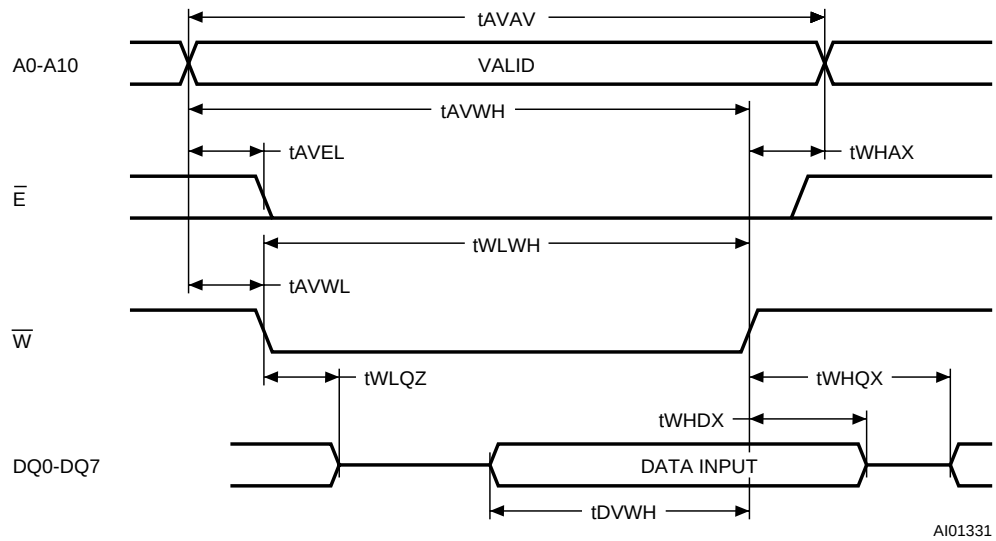
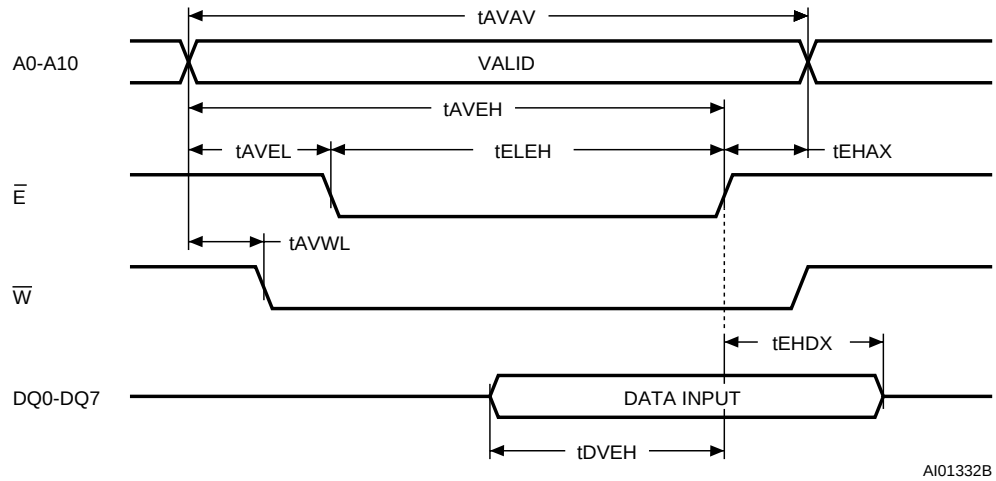



**Figure 8. Chip Enable Controlled, Write AC Waveforms**



## DATA RETENTION MODE

With valid $V_{CC}$ applied, the M48Z02/12 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when $V_{CC}$ falls within the $V_{PFD}$(max), $V_{PFD}$(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

**Note:** A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD}$(min), the user can be assured the memory will be in a write protected state, provided the $V_{CC}$ fall time is not less than $t_F$. The M48Z02/12 may respond to transient noise spikes on $V_{CC}$ that reach into the deselect window during the time the device is sampling $V_{CC}$. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external $V_{CC}$ to the RAM and disconnects the battery when $V_{CC}$ rises above $V_{SO}$. As $V_{CC}$ rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

## POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

$I_{CC}$ transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the $V_{CC}$ bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the $V_{CC}$ bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in Figure 10) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on $V_{CC}$ that drive it to values below $V_{SS}$ by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommeded to connect a schottky diode from $V_{CC}$ to $V_{SS}$ (cathode connected to $V_{CC}$, anode to $V_{SS}$). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Figure 9. Checking the $\overline{BOK}$ Flag Status**

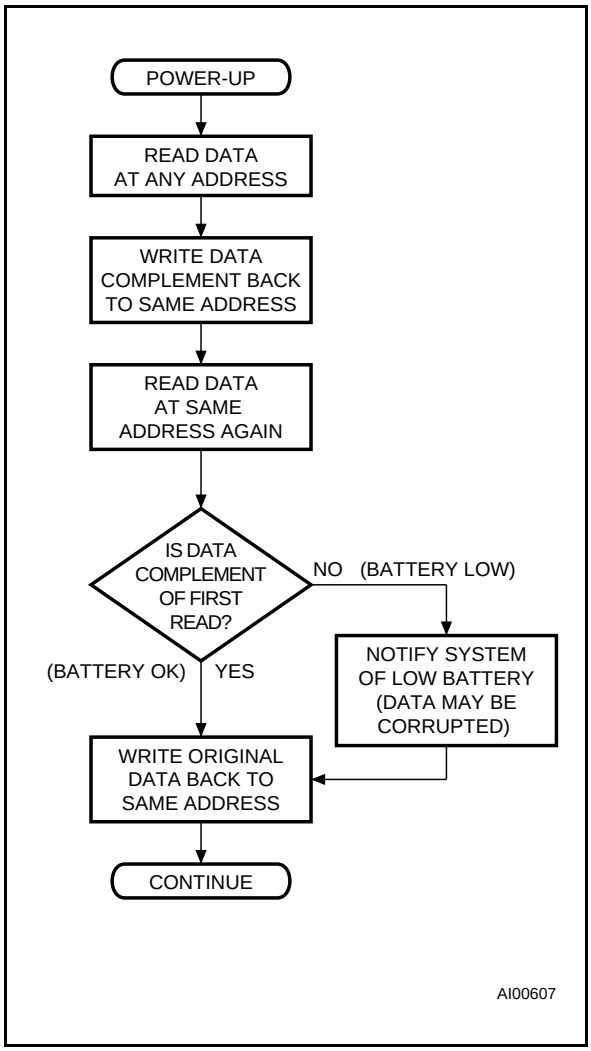
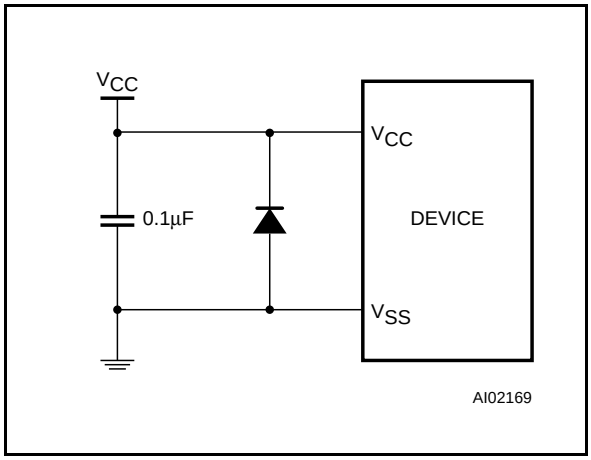
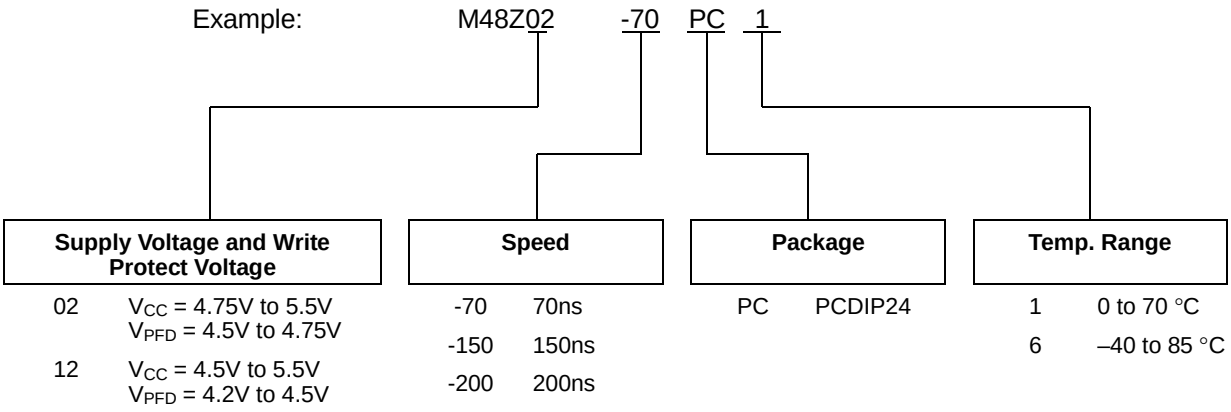



**Figure 10. Supply Voltage Protection**



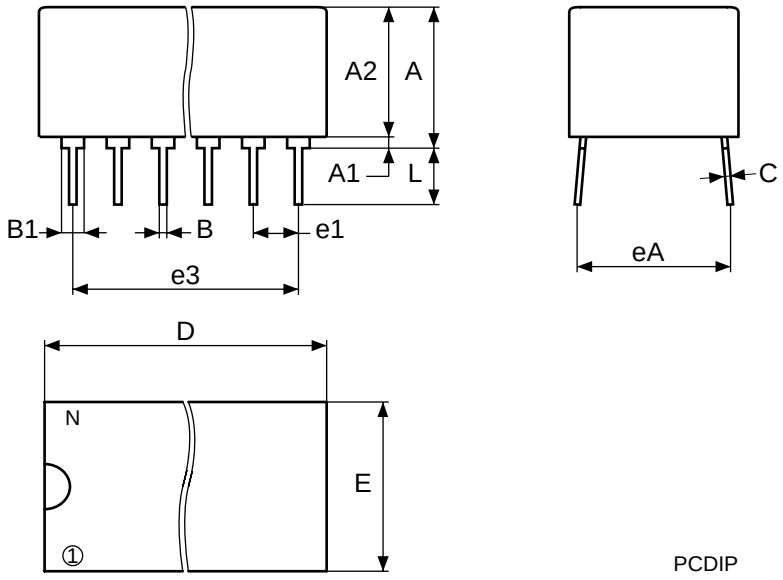
## ORDERING INFORMATION SCHEME




For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

## PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 8.89 | 9.65 | | 0.350 | 0.380 |
| A1 | | 0.38 | 0.76 | | 0.015 | 0.030 |
| A2 | | 8.38 | 8.89 | | 0.330 | 0.350 |
| B | | 0.38 | 0.53 | | 0.015 | 0.021 |
| B1 | | 1.14 | 1.78 | | 0.045 | 0.070 |
| C | | 0.20 | 0.31 | | 0.008 | 0.012 |
| D | | 34.29 | 34.80 | | 1.350 | 1.370 |
| E | | 17.83 | 18.34 | | 0.702 | 0.722 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | | 25.15 | 30.73 | | 0.990 | 1.210 |
| eA | | 15.24 | 16.00 | | 0.600 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| N | 24 | | | 24 | | |




PCDIP

Drawing is not to scale.