230 9361
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MOTOROLA
# SEMICONDUCTORS

**MC145026**
**MC145027**
**MC145028**

## Advance Information

**CMOS MSI**
(LOW-POWER COMPLEMENTARY MOS)

**REMOTE CONTROL ENCODER/DECODER PAIRS**



### MC145026 ENCODER, MC145027/MC145028 DECODERS

The MC145026 will encode nine bits of information and serially transmit this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0, 1, open) to allow $3^9$ (19,683) different codes.

Two decoders are presently available. Both use the same transmitter — the MC145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The MC145027 will interpret the first five transmitted bits as address and the last four bits as data. The MC145028 will treat all nine bits as address. If no errors are received, the MC145027 will output the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output will go high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

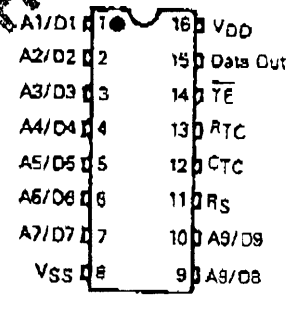
- May be Addressed in either Binary or Trinary
- Trinary Addressing Maximizes Number of Codes
- Interfaces with RF, Ultrasonic, or Infrared Transmission Medias
- Double Transmissions for Error Checking
- 4.5 V to 18 V Operation
- On-Chip R/C Oscillator; No Crystal Required
- High External Component Tolerance; Can Use 5% Components
- Standard B-Series Input and Output Characteristics

L SUFFIX
CERAMIC PACKAGE
CASE 620

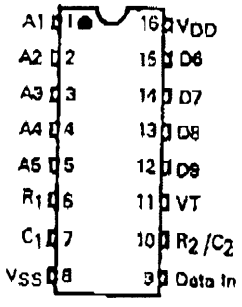
P SUFFIX
PLASTIC PACKAGE
CASE 648

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

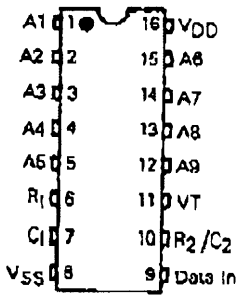
### PIN ASSIGNMENTS




MC145026
Encoder




MC145027
Decoder




MC145028
Decoder

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | −0.5 to +18 | V |
| Input Voltage, All Inputs | $V_{in}$ | −0.5 to $V_{DD}$ +0.5 | V |
| DC Current Drain Per Pin | I | 10 | mA |
| Operating Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS**

| Characteristic | Symbol | $V_{DD}$ V | −40°C Min | −40°C Max | 25°C Min | 25°C Typ | 25°C Max | 85°C Min | 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage — "0" Level, $V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | V |
| | | 10 | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | 15 | | 0.05 | | 0 | 0.05 | | 0.05 | |
| "1" Level, $V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | V |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage — "0" Level, ($V_O$ = 4.5 or 0.5 V) | $V_{IL}$ | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | V |
| ($V_O$ = 9.0 or 1.0 V) | | 10 | | 3.0 | | 4.50 | 3.0 | | 3.0 | |
| ($V_O$ = 13.5 or 1.5 V) | | 15 | | 4.0 | | 6.25 | 4.0 | | 4.0 | |
| "1" Level, ($V_O$ = 0.5 or 4.5 V) | $V_{IH}$ | 5.0 | 3.5 | — | 2.75 | — | 3.5 | — | — | V |
| ($V_O$ = 1.0 or 9.0 V) | | 10 | 7.0 | | 5.50 | | 7.0 | | | |
| ($V_O$ = 1.5 or 13.5 V) | | 15 | 11.0 | | 8.25 | | 11.0 | | | |
| Output Drive Current — Source, ($V_{OH}$ = 2.5 V) | $I_{OH}$ | 5.0 | −2.1 | — | −4.2 | — | −1.7 | — | — | mA |
| ($V_{OH}$ = 4.6 V) | | 10 | −0.44 | | −0.88 | | −0.36 | | | |
| ($V_{OH}$ = 9.5 V) | | 10 | −1.1 | | −2.25 | | −0.9 | | | |
| ($V_{OH}$ = 13.5 V) | | 15 | −3.0 | | −6.8 | | −2.4 | | | |
| ($V_{OL}$ = 0.4 V) — Sink | $I_{OL}$ | 5.0 | 0.52 | | 0.44 | 0.88 | — | 0.36 | — | mA |
| ($V_{OL}$ = 0.5 V) | | 10 | 1.3 | | 1.1 | 2.25 | | 0.9 | | |
| ($V_{OL}$ = 1.5 V) | | 15 | 3.6 | | 3.0 | 6.8 | | 2.4 | | |
| Input Current — TE (MC145026) Pullup Device | $I_{in}$ | 5.0 | — | — | 3.0 | 4.0 | 7.0 | — | — | µA |
| | | 10 | | | 15 | 20 | 26 | | | |
| | | 15 | | | 36 | 46 | 65 | | | |
| Input Current — RS (MC145028), Data In (MC145027, MC145028) | $I_{in}$ | 15 | — | ±0.3 | — | ±0.00001 | ±0.1 | — | ±1.0 | µA |
| Input Current — A1/D1-A9/D9 (MC145026), A1-A8 (MC145027), A1-A9 (MC145028) | $I_{in}$ | 5.0 | — | — | — | ±55 | ±80 | — | — | µA |
| | | 10 | | | | ±300 | ±340 | | | |
| | | 15 | | | | ±650 | ±725 | | | |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current — MC145026 | $I_{DD}$ | 5.0 | — | — | — | 0.0050 | 0.10 | — | — | µA |
| | | 10 | | | | 0.0100 | 0.20 | | | |
| | | 15 | | | | 0.0150 | 0.30 | | | |
| Quiescent Current — MC145027, MC145028 | $I_{DD}$ | 5.0 | — | — | — | 30 | 50 | — | — | µA |
| | | 10 | | | | 60 | 100 | | | |
| | | 15 | | | | 90 | 150 | | | |
| Total Supply Current — MC145026 ($f_c$ = 20 kHz) | $I_T$ | 5.0 | — | — | — | 100 | 200 | — | — | µA |
| | | 10 | | | | 200 | 400 | | | |
| | | 15 | | | | 300 | 600 | | | |
| Total Supply Current — MC145027, MC145028 ($f_c$ = 20 kHz) | $I_T$ | 5.0 | — | — | — | 200 | 400 | — | — | µA |
| | | 10 | | | | 400 | 800 | | | |
| | | 15 | | | | 600 | 1200 | | | |

**SWITCHING CHARACTERISTICS** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$ $t_{THL}$ | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Data In Rise and Fall Time (MC145027, MC145028) | $t_{TLH}$ $t_{THL}$ | 5.0 | – | – | 15 | µs |
| | | 10 | – | – | 15 | |
| | | 15 | – | – | 15 | |
| Encoder Clock Frequency | $f_{cl}$ | 5.0 | 0 | – | 2 | kHz |
| | | 10 | 0 | – | 5 | |
| | | 15 | 0 | – | 10 | |
| Maximum Decoder Frequency (Referenced to Encoder Clock) (See Figure 9) | $f_{cl}$ | 5.0 | – | – | [illegible] | kHz |
| | | 10 | – | – | [illegible]10 | |
| | | 15 | – | – | [illegible]0 | |
| $\overline{TE}$ Pulse Width | $t_{WL}$ | 5.0 | 85 | – | – | ns |
| | | 10 | [illegible] | – | – | |
| | | 15 | [illegible] | – | – | |
| System Propagation Delay ($\overline{TE}$ to Valid Transmission) | – | | – | 182 | – | Clock Cycles |
| Tolerance on Timing Components ($\Delta R_{TC} + \Delta C_{TC} + \Delta R_1 + \Delta C_1$) | – | – | – | – | ±25 | % |
| ($\Delta R_2 + \Delta C_2$) | | – | – | – | ±25 | |



## OPERATING CHARACTERISTICS

### MC145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0, 1, open) allowing $3^9 = 19683$ possible codes. The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low and then high. If only a high state results from the two tests, the input is assumed to be hard wired to $V_{DD}$. If only a low state is obtained, the input is assumed to be hard wired to $V_{SS}$. If both a high and a low can be forced at the input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high, the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

### MC145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. If this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

### MC145028

This receiver operates in the same manner as the MC145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the MC145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2 \times 3^8 = 13,122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

### DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figures 7 and 8.

## PIN DESCRIPTION

**MC145026 Encoder**

**A1/D1-A9/D9** — These inputs will be encoded and the data serially output from the encoder.

**VSS** — The most negative supply (usually ground).

**RS, CTC, RTC** — These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the CTC pin and the RTC and CTC pins should be left open.

**TE** — This Transmit Enable (active low) input will initiate transmission which forced low. A pullup device will keep this input high normally.

**Data Out** — This is the output of the encoder that will present the serially encoded signals.

**VDD** — The most positive supply.

**MC145027 Decoder**

**A1-A5** — These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in order for the decoder to output data.

**D6 D9** — These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9. Note: only binary data will be acknowledged. A binary open will be decoded as logic one.

**R1, C1** — These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant $R_1 \times C_1$ should be set to 1.72 transmit clock periods. $R_1C_1 = 3.96\ R_{TC}C_{TC}$.

**R2/C2** — This pin accepts a resistor to VSS and a capacitor to VSS that are used to detect both the end of an encoded word and the end of transmission. The time constant $R_2 \times C_2$ should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks for a voltage equivalent two data bit times (0.4 $R_2C_2$) to detect the dead time between transmitted words. $R_2C_2 = 77\ R_{TC}C_{TC}$.

**Valid Transmission, VT** — This output will go high when the following conditions are satisfied:

1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received.

VT will remain high until either a mismatch is received, or no input signal is received for four data bit times.

**VDD** — The most positive supply.

**VSS** — The most negative supply (usually ground).

FIGURE 1 — ENCODER BLOCK DIAGRAM MC145026

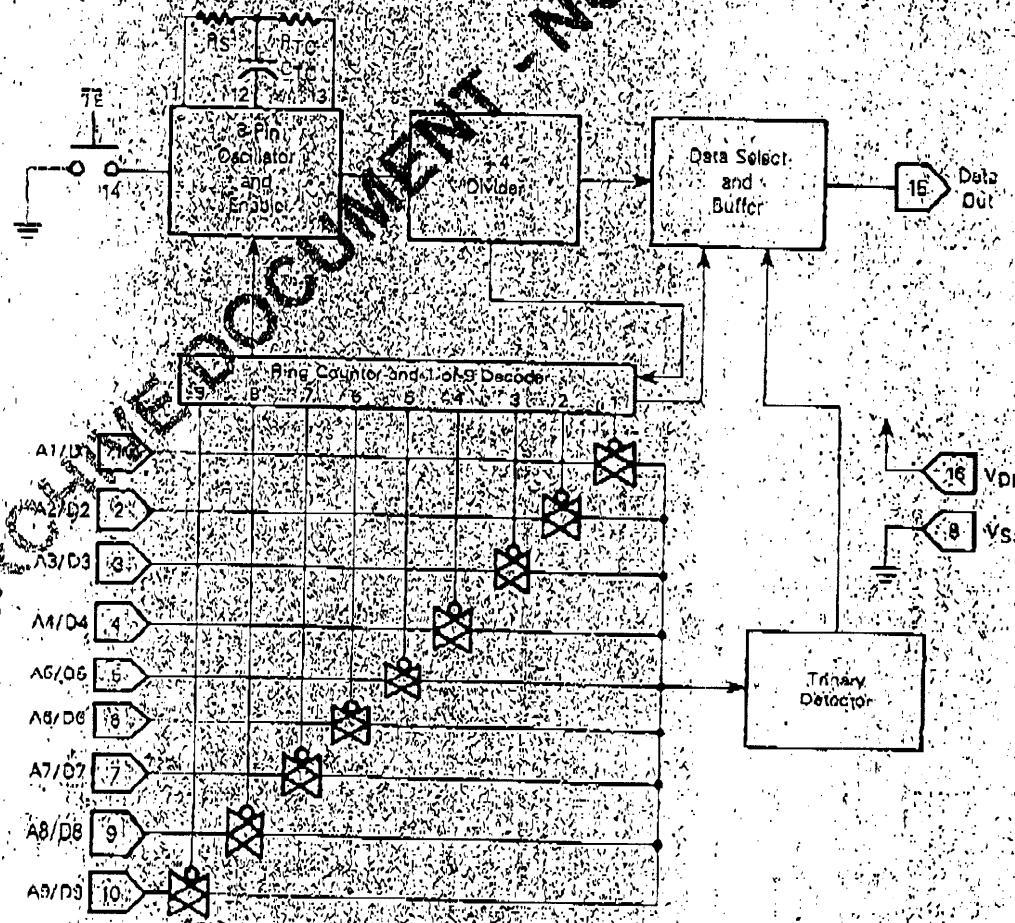


FIGURE 2 — DECODER BLOCK DIAGRAM MC145027

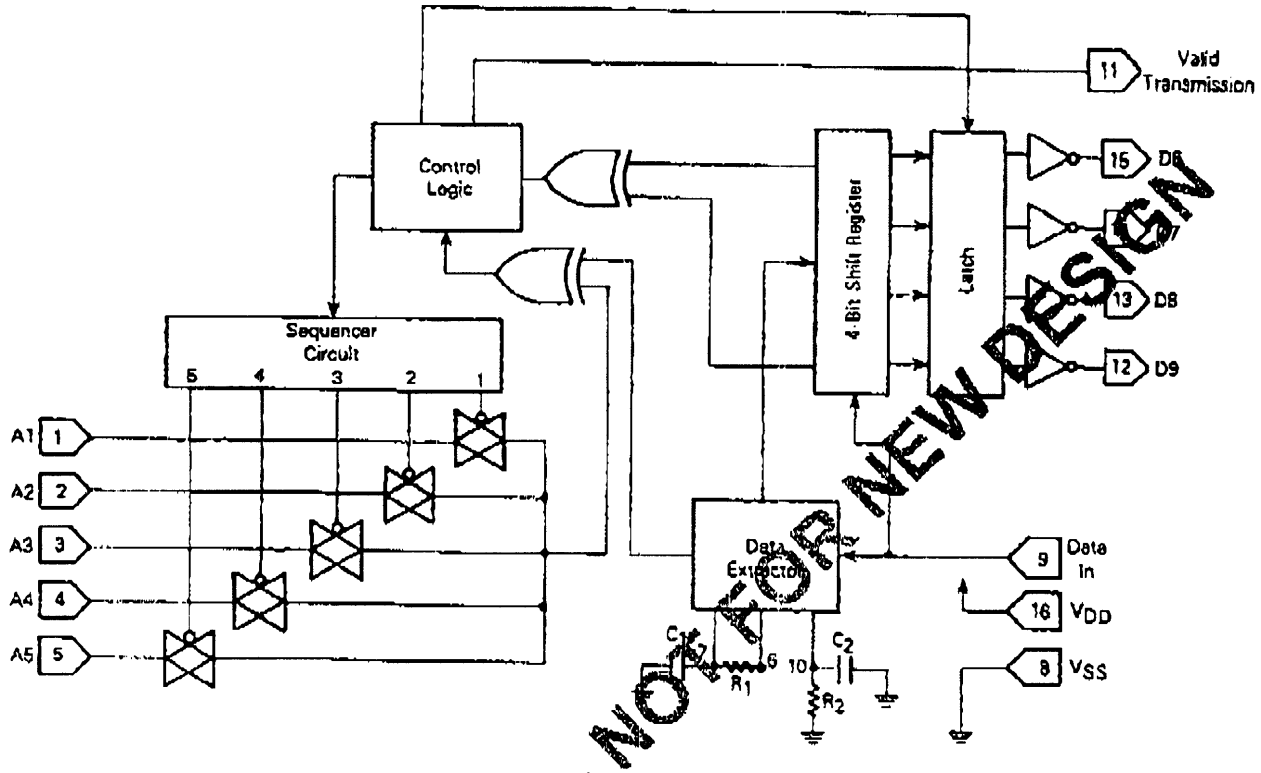





FIGURE 3 — DECODER BLOCK DIAGRAM MC145028

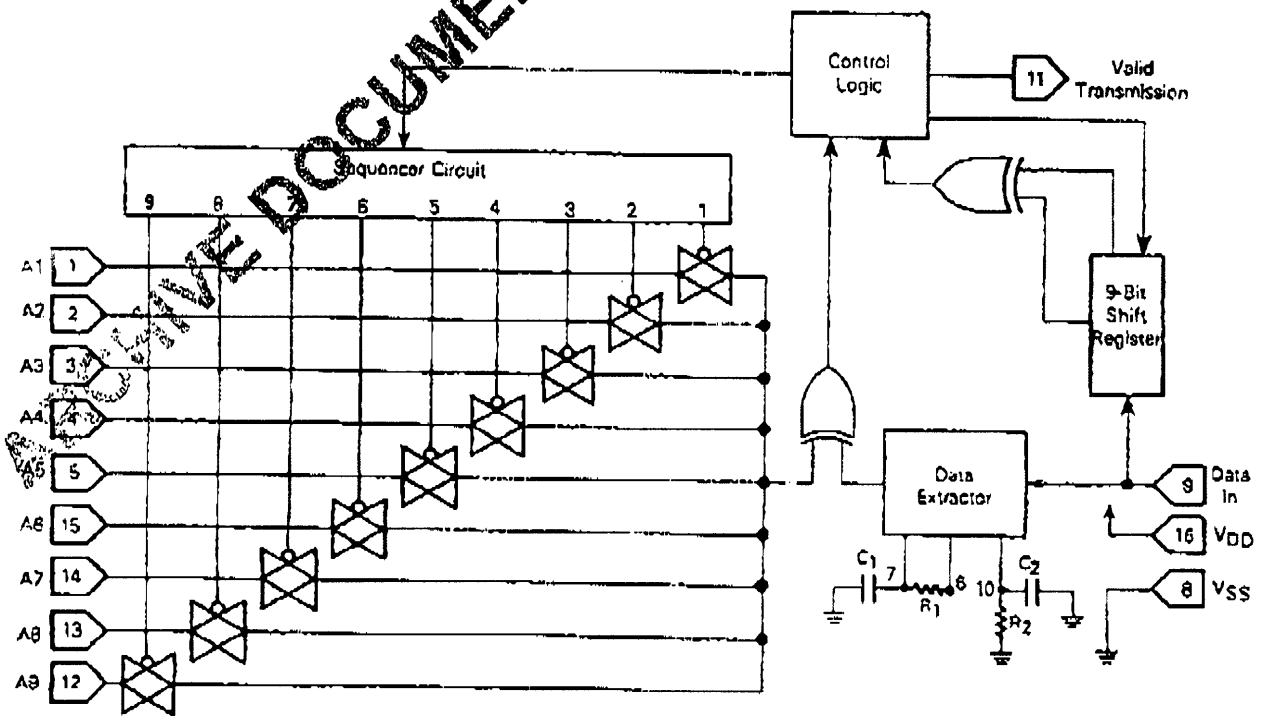
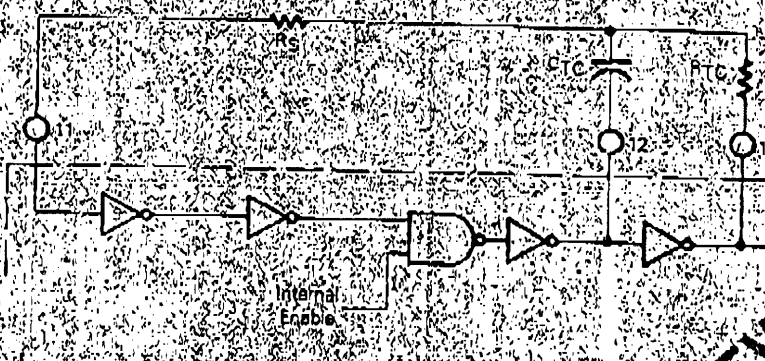


FIGURE 4 — ENCODER OSCILLATOR INFORMATION




This oscillator will operate at a frequency determined by the external RC network:

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC}}\ (Hz)$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC} = C_{TC}$ + Dayout + 12 pF

$R_S = 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF ≤ $C_{TC}$ ≤ 10 nF

The value for $R_S$ should be chosen to be about 2 times $R_{TC}$. This range will ensure that current through $R_S$ is insignificant compared to current through $R_{TC}$. The upper limit for $R_S$ must ensure that $R_S \times 5$ pF (input capacitance) is small compared to $R_{TC} \times C_{TC}$.

For frequencies outside the indicated range, the formula will be less accurate. The active oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

FIGURE 5 — ENCODER/DECODER TIMING DIAGRAM

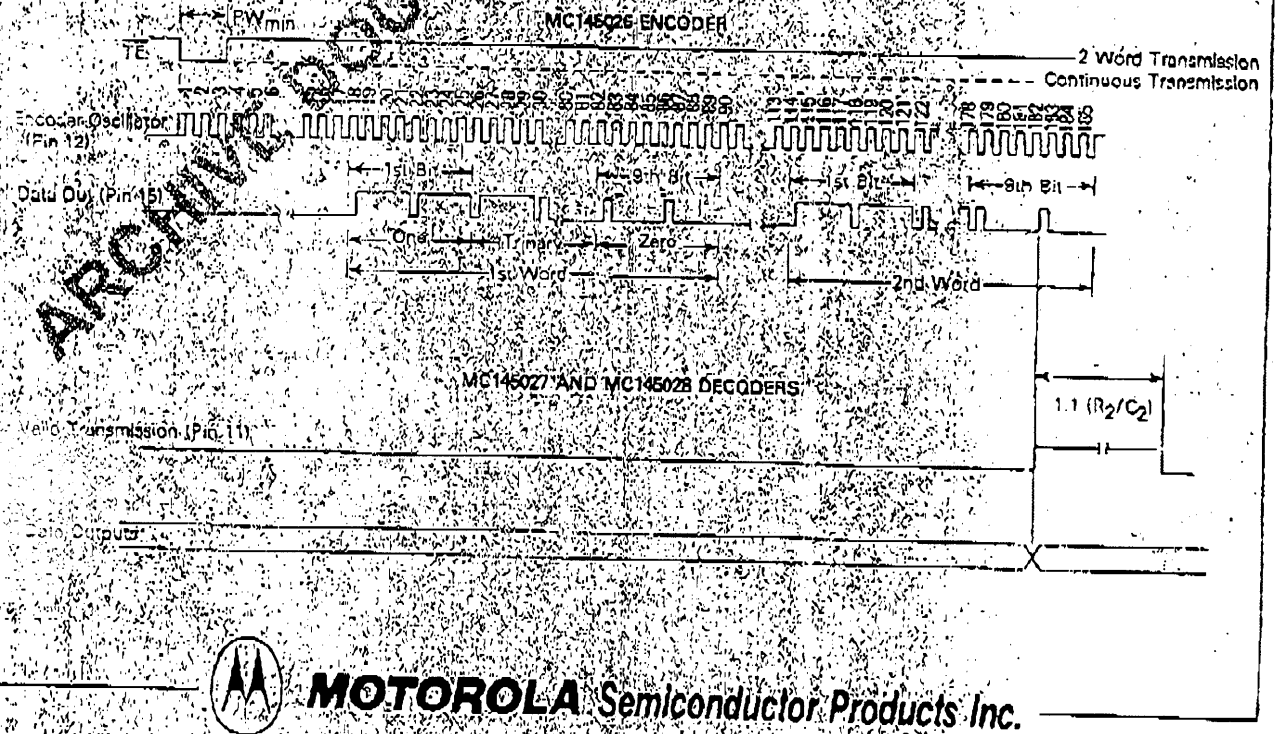
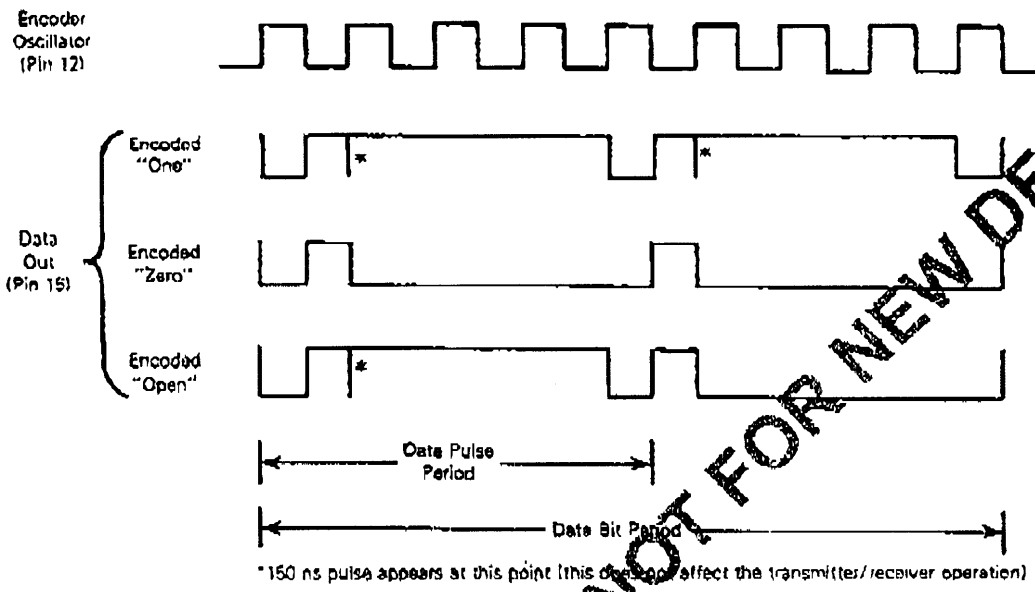


FIGURE 6 — ENCODER DATA WAVEFORMS (MC145026)




*150 ns pulse appears at this point (this does not affect the transmitter/receiver operation)

FIGURE 7 – MC145027 FLOWCHART

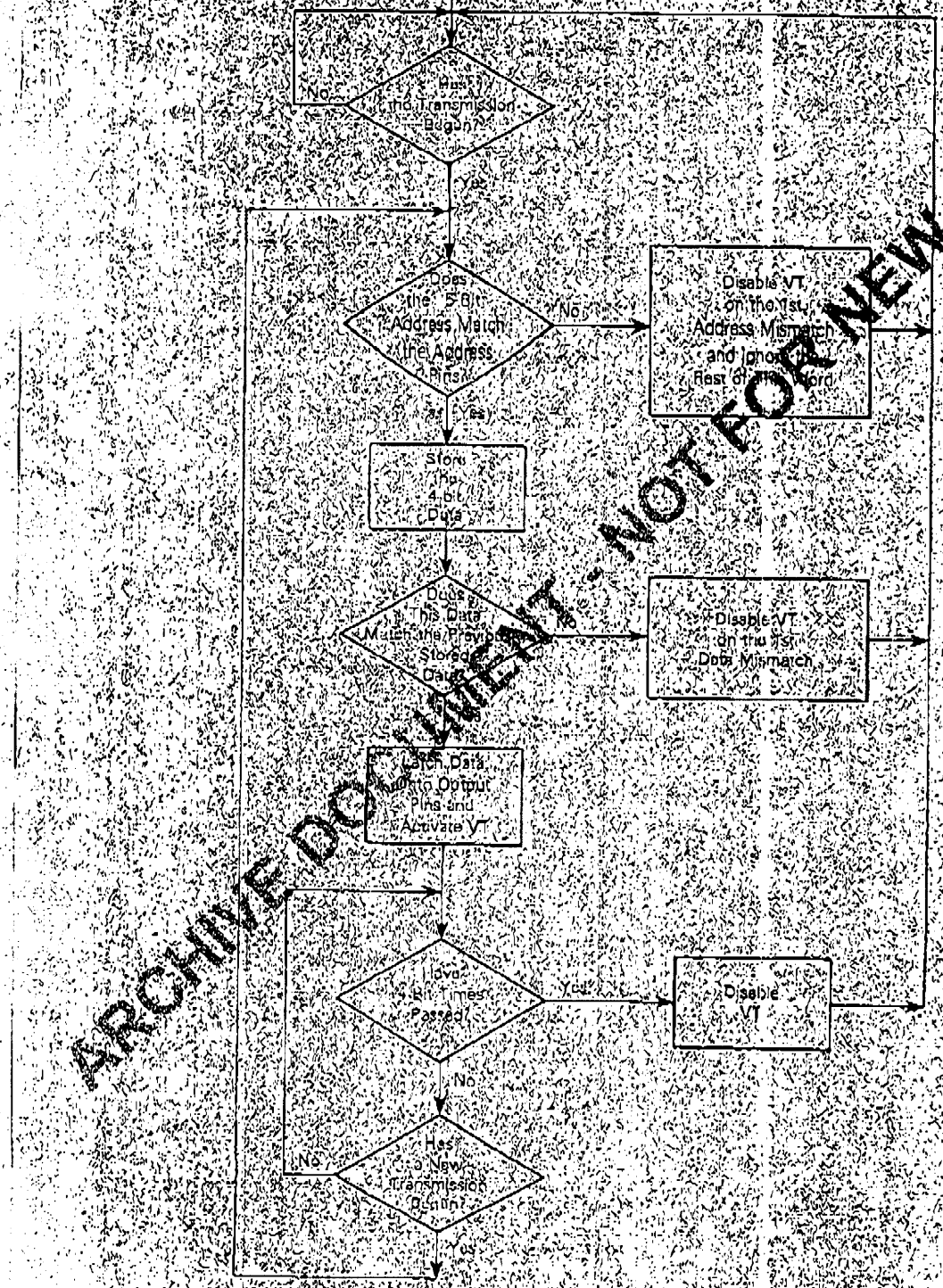
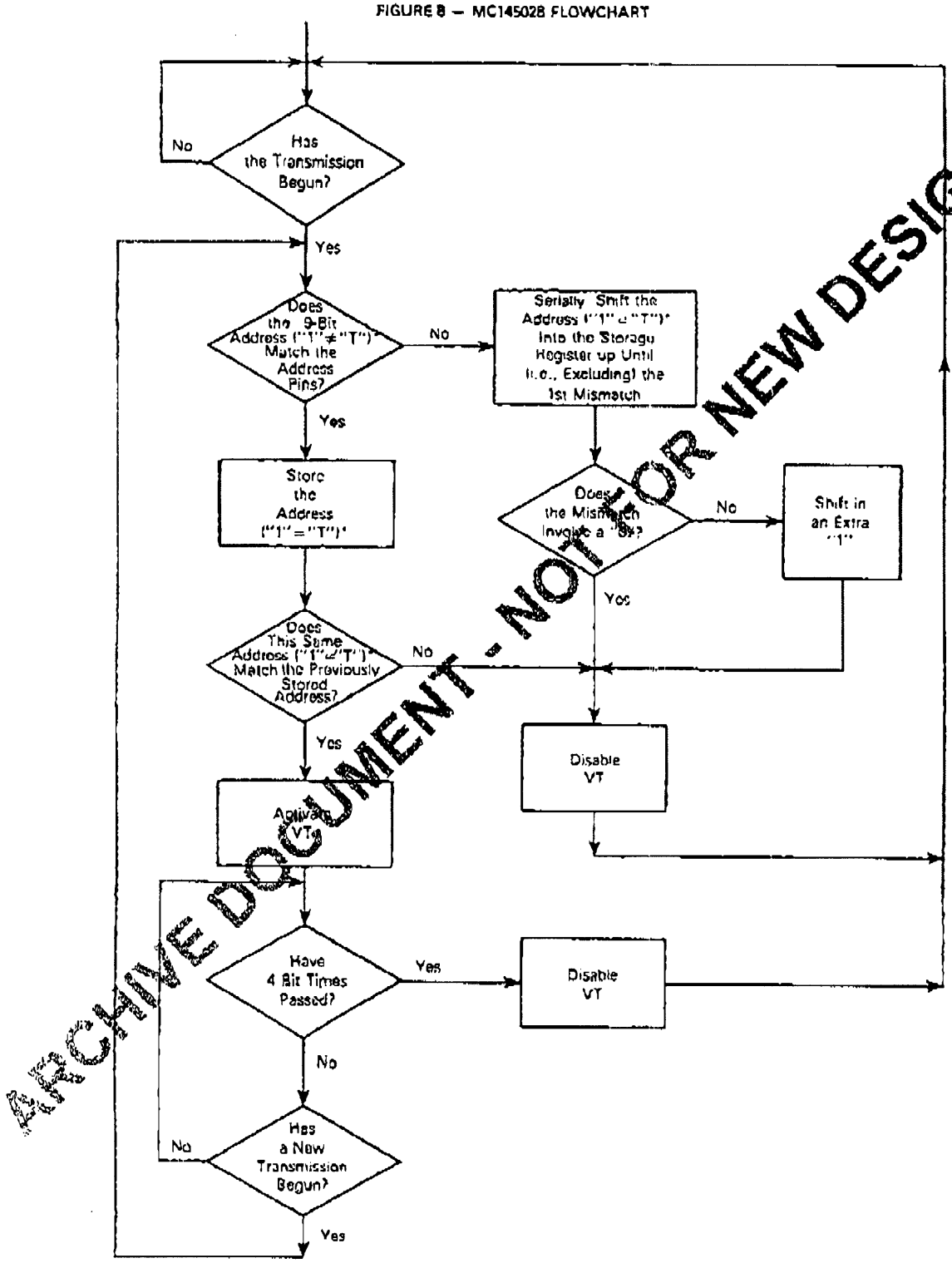
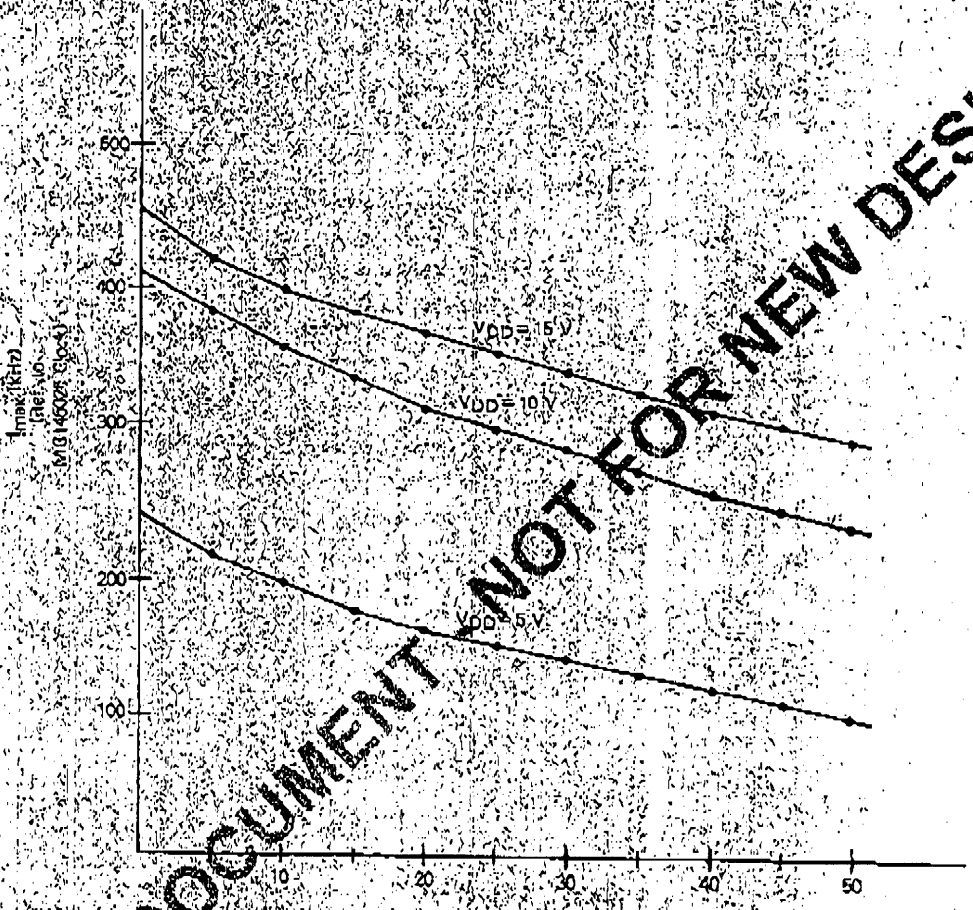


FIGURE 8 — MC145028 FLOWCHART




*For shift register comparisons, a "T" is stored as a "1".

FIGURE 9 — MC145027/MC145028 $f_{max}$ vs $C_{layout}$



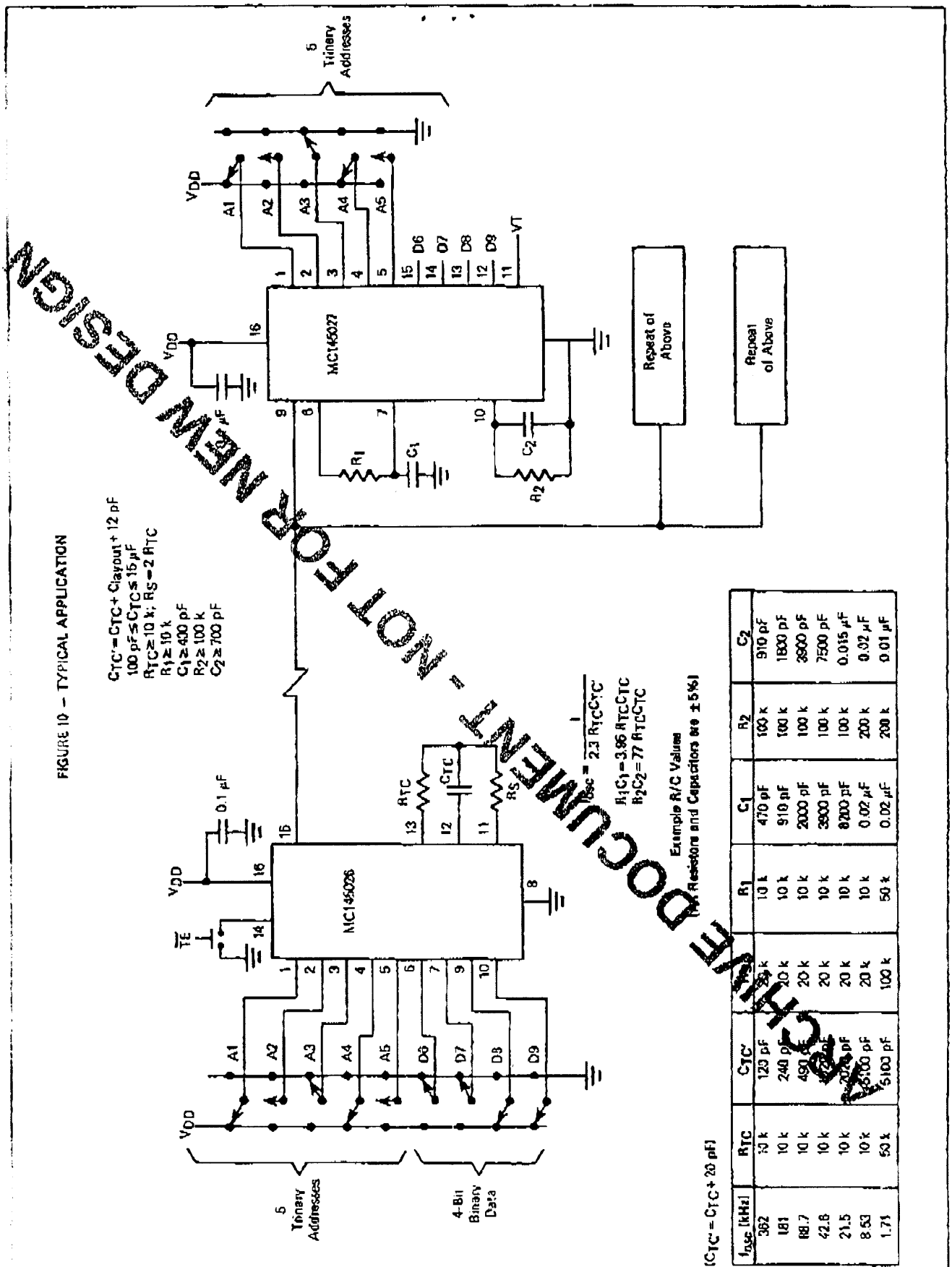



FIGURE 10 – TYPICAL APPLICATION

$C_{TC'} = C_{TC} + C_{layout} + 12$ pF
100 pF ≤ $C_{TC}$ ≤ 15 µF
$R_{TC} \geq 10$ k; $R_S = 2\,R_{TC}$
$R_1 \geq 10$ k
$C_1 \geq 430$ pF
$R_2 \geq 100$ k
$C_2 \geq 700$ pF

$$f_{osc} = \frac{1}{2.3\,R_{TC}C_{TC'}}$$

$R_1C_1 = 3.86\,R_{TC}C_{TC}$
$R_2C_2 = 77\,R_{TC}C_{TC}$

Example R/C Values
(Resistors and Capacitors are ±5%)

| $f_{osc}$ [kHz] | $R_{TC}$ | $C_{TC'}$ ($C_{TC'} = C_{TC} + 20$ pF) | $R_1$ | $C_1$ | $R_2$ | $C_2$ |
|---|---|---|---|---|---|---|
| 362 | 10 k | 120 pF | 10 k | 470 pF | 100 k | 910 pF |
| 181 | 10 k | 240 pF | 10 k | 910 pF | 100 k | 1800 pF |
| 88.7 | 10 k | 491 pF | 10 k | 2000 pF | 100 k | 3600 pF |
| 42.8 | 10 k | 1020 pF | 10 k | 3900 pF | 100 k | 7500 pF |
| 21.5 | 10 k | 2030 pF | 10 k | 8200 pF | 100 k | 0.015 µF |
| 8.53 | 10 k | 5100 pF | 10 k | 0.02 µF | 200 k | 0.02 µF |
| 1.71 | 50 k | 5100 pF | 50 k | 0.02 µF | 200 k | 0.01 µF |