MAX809 Series, MAX810 Series

Very Low Supply Current 3-Pin Microprocessor Reset Monitors

The MAX809 and MAX810 are cost−effective system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 10 μsec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a minimum of 140 msec after V_{CC} rises above the reset threshold. The MAX810 has an active−high RESET output while the MAX809 has an active−low $\overline{\text{RESET}}$ output. Both devices are available in a SOT−23 package.

The MAX809/810 are optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 1.0 μA (V_{CC} = 3.2 V) makes these devices suitable for battery powered applications.

Features

- Precision V_{CC} Monitor for 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.6 V to 4.9 V Available in 100 mV Steps
- 140 msec Guaranteed Minimum $\overline{\text{RESET}}$ Output Duration
- Compatible with Hot Plug Applications
- Low Supply Current
- V_{CC} Transient Immunity
- Small SOT−23 Package
- No External Components
- Wide Operating Temperature: −40°C to 105°C
- Pb−Free Packages are Available

Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical Microprocessor Power Supply Monitoring

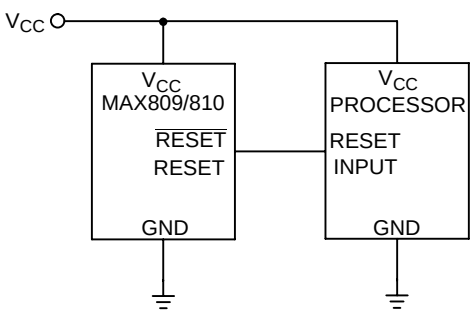
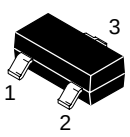


Figure 1. Typical Application Diagram

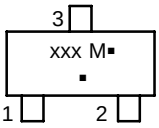
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

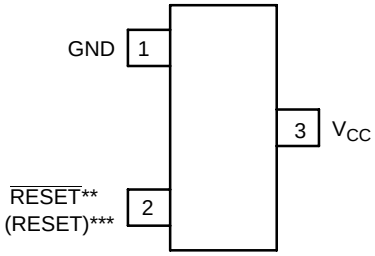


SOT−23 (TO−236) CASE 318



xxx = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION



SOT−23*
(Top View)

*SOT−23 is equivalent to JEDEC (TO−236)
** $\overline{\text{RESET}}$ is for MAX809
*** RESET is for MAX810

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{\text{RESET}}$ (MAX809)	$\overline{\text{RESET}}$ output remains low while V_{CC} is below the reset voltage threshold, and for 240 msec (Typ) after V_{CC} rises above reset threshold
2	RESET (MAX810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for 240 msec (Typ) after V_{CC} rises above reset threshold
3	V_{CC}	Supply Voltage (Typ)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to GND)	V_{CC}	6.0	V
$\overline{\text{RESET}}$		−0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}		20	mA
Output Current, $\overline{\text{RESET}}$		20	mA
dV/dt (V_{CC})		100	V/μsec
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	491	°C/W
Operating Temperature Range	T_A	−40 to +105	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{sol}	+260	°C
Latchup performance: Positive Negative	$I_{Latchup}$	 200 200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 350 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

ELECTRICAL CHARACTERISTICS T_A = −40°C to +105°C unless otherwise noted. Typical values are at T_A = +25°C. (Note 3)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Range T_A = 0°C to +70°C T_A = −40°C to +105°C		 1.0 1.2	 − −	 5.5 5.5	V
Supply Current V_{CC} = 3.3 V T_A = −40°C to +85°C T_A = 85°C to +105°C V_{CC} = 5.5 V T_A = −40°C to +85°C T_A = 85°C to +105°C	I_{CC}	 − − − −	 0.5 − 0.8 −	 1.2 2.0 1.8 2.5	μA

3. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) T_A = −40°C to +105°C unless otherwise noted. Typical values are at T_A = +25°C. (Note 4)

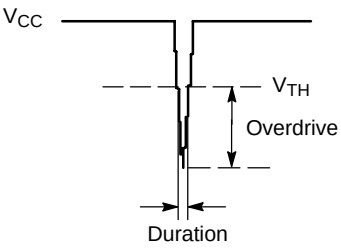
Characteristic	Symbol	Min	Typ	Max	Unit
Reset Threshold (Note 5)	V_{TH}				V
MAX809SN490					
T_A = +25°C		4.83	4.9	4.97	
T_A = −40°C to +85°C		4.78	−	5.02	
T_A = +85°C to +105°C		4.66	−	5.14	
MAX8xxLTR					
T_A = +25°C		4.56	4.63	4.70	
T_A = −40°C to +85°C		4.50	−	4.75	
T_A = +85°C to +105°C		4.40	−	4.86	
MAX809HTR					
T_A = +25°C		4.48	4.55	4.62	
T_A = −40°C to +85°C		4.43		4.67	
T_A = +85°C to +105°C		4.32		4.78	
MAX8xxMTR					
T_A = +25°C		4.31	4.38	4.45	
T_A = −40°C to +85°C		4.27		4.49	
T_A = +85°C to +105°C		4.16		4.60	
MAX809JTR					
T_A = +25°C		3.94	4.00	4.06	
T_A = −40°C to +85°C		3.90	−	4.10	
T_A = +85°C to +105°C		3.80	−	4.20	
MAX8xxTTR					
T_A = +25°C		3.04	3.08	3.11	
T_A = −40°C to +85°C		3.00	−	3.16	
T_A = +85°C to +105°C		2.92	−	3.24	
MAX8xxSTR					
T_A = +25°C		2.89	2.93	2.96	
T_A = −40°C to +85°C		2.85	−	3.00	
T_A = +85°C to +105°C		2.78	−	3.08	
MAX8xxRTR					
T_A = +25°C		2.59	2.63	2.66	
T_A = −40°C to +85°C		2.56	−	2.70	
T_A = +85°C to +105°C		2.49	−	2.77	
MAX809SN232					
T_A = +25°C		2.28	2.32	2.35	
T_A = −40°C to +85°C		2.25	−	2.38	
T_A = +85°C to +105°C		2.21	−	2.45	
MAX809SN160					
T_A = +25°C		1.58	1.6	1.62	
T_A = −40°C to +85°C		1.56	−	1.64	
T_A = +85°C to +105°C		1.52	−	1.68	
Reset Temperature Coefficient		−	30	−	ppm/°C
V_{CC} to Reset Delay V_{CC} = V_{TH} to (V_{TH} − 100 mV)		−	10	−	μsec
Reset Active TimeOut Period		140	240	460	msec
$\overline{RESET}$ Output Voltage Low V_{CC} = V_{TH} − 0.2 V 1.6 V ≤ V_{TH} ≤ 2.0 V, I_{SINK} = 0.5 mA 2.1 V ≤ V_{TH} ≤ 4.0 V, I_{SINK} = 1.2 mA 4.1 V ≤ V_{TH} ≤ 4.9 V, I_{SINK} = 3.2 mA	V_{OL}	−	−	0.3	V
$\overline{RESET}$ Output Voltage High V_{CC} = V_{TH} + 0.2 V 1.6 V ≤ V_{TH} ≤ 2.4 V, I_{SOURCE} = 200 μA 2.5 V ≤ V_{TH} ≤ 4.9 V, I_{SOURCE} = 500 μA	V_{OH}	0.8 V_{CC}	−	−	V

4. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.
5. Contact your ON Semiconductor sales representative for other threshold voltage options.

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The MAX809 provides accurate V_{CC} monitoring and reset timing during power−up, power−down, and brownout/sag conditions, and rejects negative−going transients (glitches) on the power supply line. Figure 2 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies **under** the curve will **not** generate a reset signal. Combinations above the curve are detected as a brownout or power−down. Typically, transient that goes 100 mV below the reset threshold and lasts 5.0 μs or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the V_{CC} pin of the MAX809.



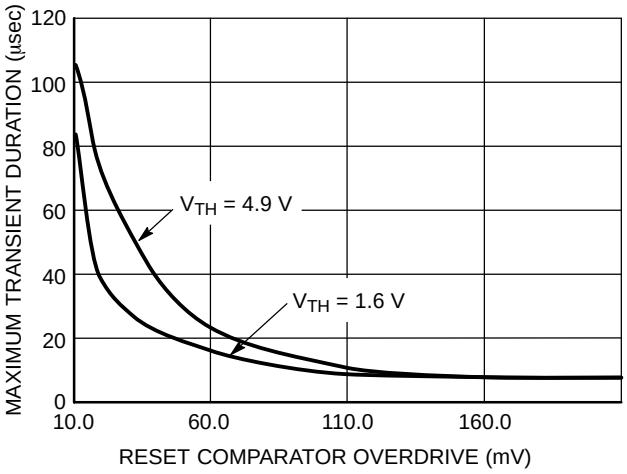


Figure 2. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

$\overline{\text{RESET}}$ Signal Integrity During Power−Down

The MAX809 $\overline{\text{RESET}}$ output is valid to V_{CC} = 1.0 V. Below this voltage the output becomes an “open circuit” and does not sink current. This means CMOS logic inputs to the Microprocessor will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0 V, a pull−down resistor must be connected from $\overline{\text{RESET}}$ to ground to discharge stray capacitances and hold the output low (Figure 3). This resistor value, though not critical, should be chosen such that it does not appreciably load $\overline{\text{RESET}}$ under normal operation (100 kΩ will be suitable for most applications).

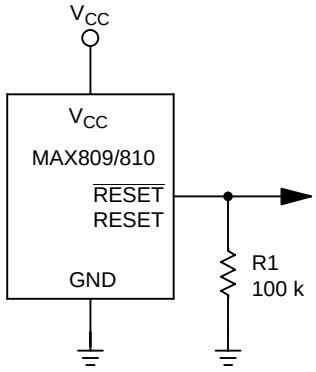


Figure 3. Ensuring RESET Valid to V_{CC} = 0 V

Processors With Bidirectional I/O Pins

Some Microprocessor’s have bidirectional reset pins. Depending on the current drive capability of the processor pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a 4.7 kΩ resistor in series with the output of the MAX809 (Figure 4). If there are other components in the system which require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the Microprocessor, the buffer should be connected as shown with the solid line.

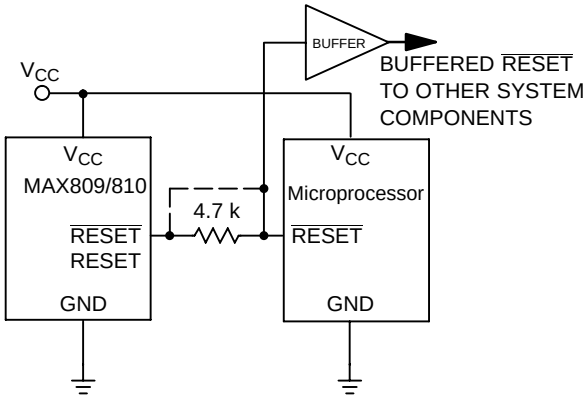


Figure 4. Interfacing to Bidirectional Reset I/O

TYPICAL CHARACTERISTICS

The following data is given for MAX809 threshold levels: 1.60 V, 2.32 V, 2.93 V, 4.63 V and 4.90 V.

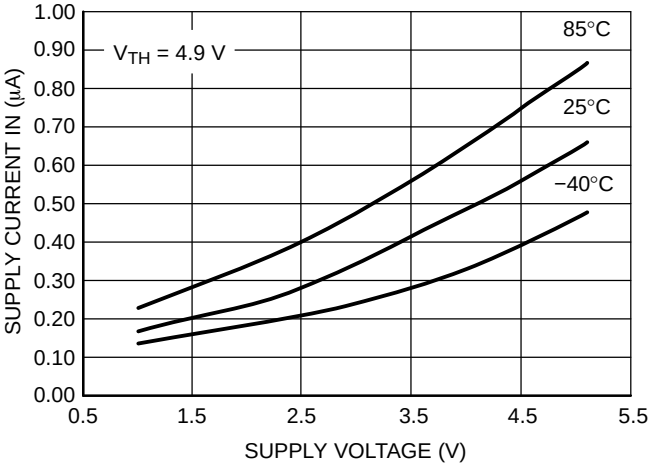


Figure 5. Supply Current vs. Supply Voltage

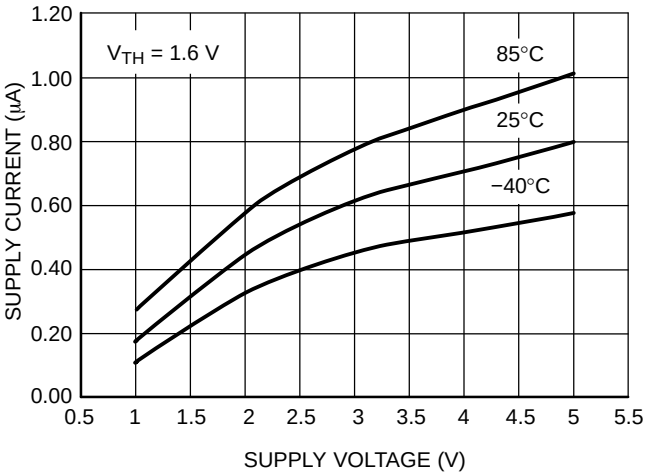


Figure 6. Supply Current vs. Supply Voltage

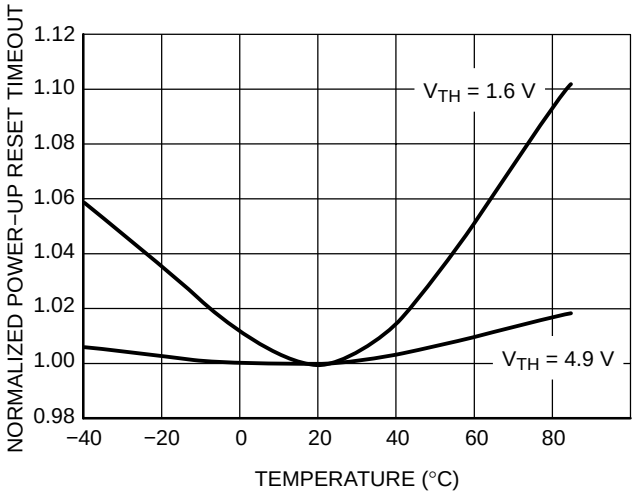


Figure 7. Normalized Power−Up Reset vs. Temperature

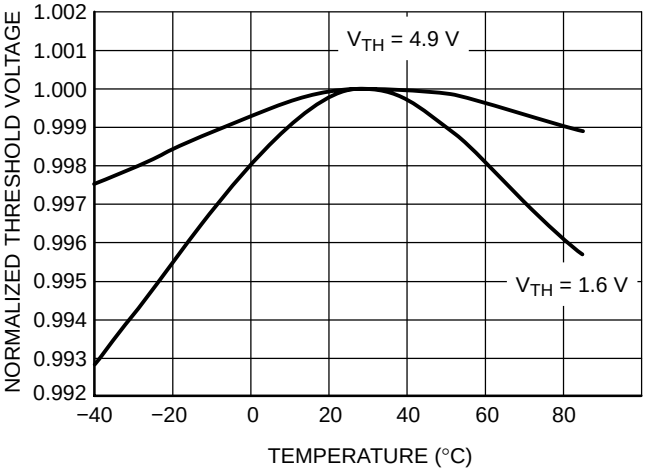


Figure 8. Normalized Reset Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS

The following data is given for MAX809 threshold levels: 2.63 V, 3.08 V, 4.00 V and 4.38 V;
MAX810 threshold levels: 2.63 V, 2.93 V, 3.08 V, 4.38 V and 4.63 V.

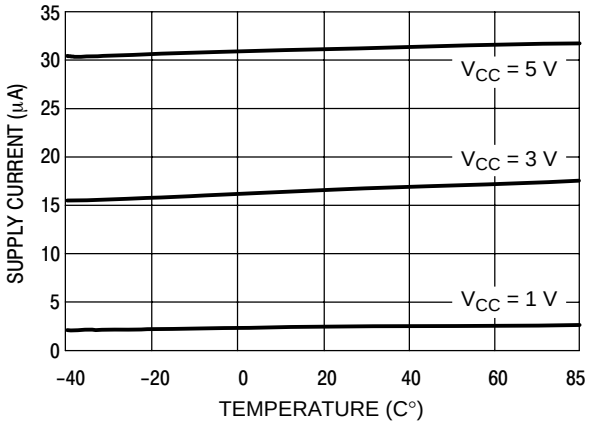


Figure 9. Supply Current vs. Temperature (No Load, MAX8xxR/T, MAX810S)

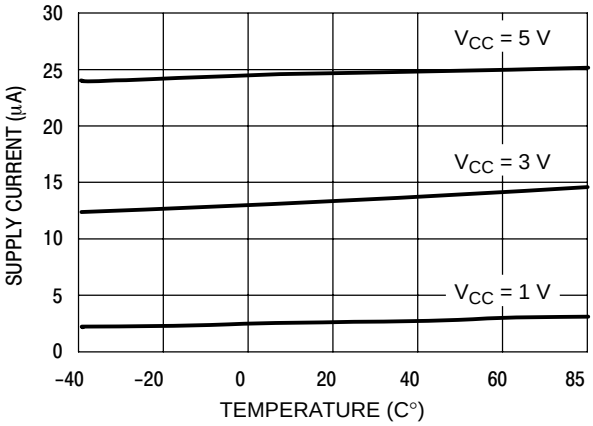


Figure 10. Supply Current vs. Temperature (No Load, MAX8xxM/MAX809J, MAX810L)

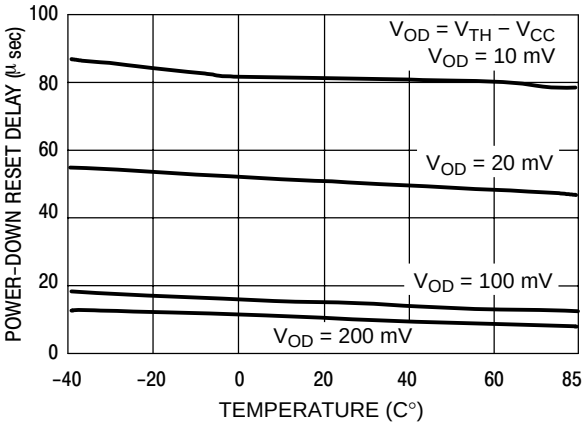


Figure 11. Power−Down Reset Delay vs. Temperature and Overdrive (MAX8xxR/T, MAX810S)

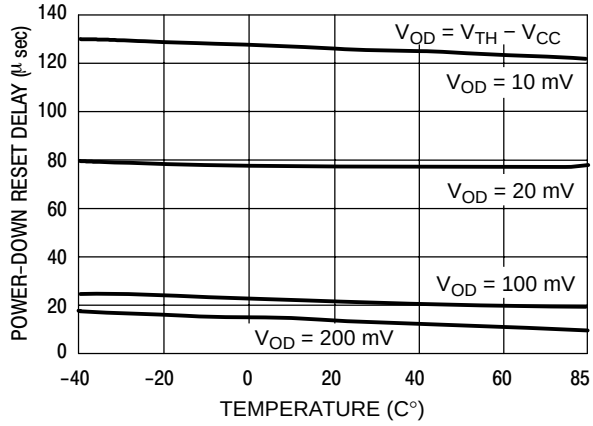


Figure 12. Power−Down Reset Delay vs. Temperature and Overdrive (MAX8xxM/MAX809J, MAX810L)

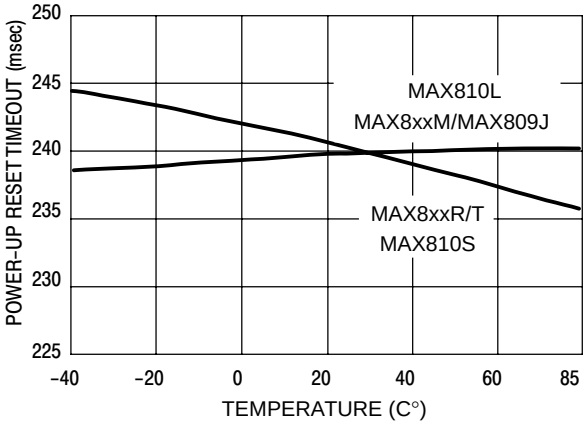


Figure 13. Power−Up Reset TimeOut vs. Temperature

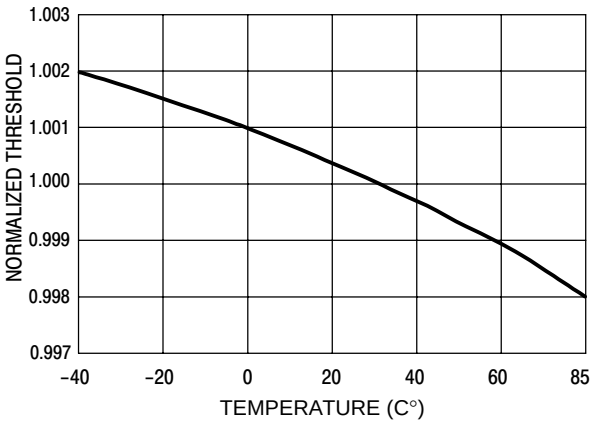


Figure 14. Normalized Reset Threshold vs. Temperature

ORDERING, MARKING AND THRESHOLD INFORMATION

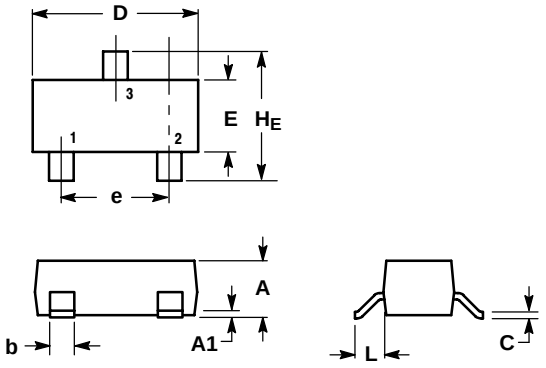
Device	V_{TH}*	Description	Marking	Package	Shipping†
MAX809SN160T1	1.60	Push−Pull $\overline{\text{RESET}}$	SAA	SOT−23	3000 Tape/Reel
MAX809SN160T1G	1.60		SAA	SOT−23 (Pb−Free)	
MAX809SN232T1	2.32		SQP	SOT−23	
MAX809SN232T1G	2.32		SQP	SOT−23 (Pb−Free)	
MAX809STR	2.93		SPT	SOT−23	
MAX809STRG	2.93		SPT	SOT−23 (Pb−Free)	
MAX809LTR	4.63		SPW	SOT−23	
MAX809LTRG	4.63		SPW	SOT−23 (Pb−Free)	
MAX809HTR	4.55		SBD	SOT−23	
MAX809HTRG	4.55		SBD	SOT−23 (Pb−Free)	
MAX809SN490T1	4.90		SBH	SOT−23	
MAX809SN490T1G	4.90		SBH	SOT−23 (Pb−Free)	
MAX809MTR	4.38		SPV	SOT−23	
MAX809MTRG	4.38		SPV	SOT−23 (Pb−Free)	
MAX809TTR	3.08		SPU	SOT−23	
MAX809TTRG	3.08		SPU	SOT−23 (Pb−Free)	
MAX809RTR	2.63		SPS	SOT−23	
MAX809RTRG	2.63		SPS	SOT−23 (Pb−Free)	
MAX809JTR	4.00		SPR	SOT−23	
MAX809JTRG	4.00		SPR	SOT−23 (Pb−Free)	
MAX810MTR	4.38	Push−Pull RESET	SQA	SOT−23	
MAX810MTRG	4.38		SQA	SOT−23 (Pb−Free)	
MAX810TTR	3.08		SPZ	SOT−23	
MAX810TTRG	3.08		SPZ	SOT−23 (Pb−Free)	
MAX810RTR	2.63		SPX	SOT−23	
MAX810RTRG	2.63		SPX	SOT−23 (Pb−Free)	
MAX810LTR	4.63		SQB	SOT−23	
MAX810LTRG	4.63		SQB	SOT−23 (Pb−Free)	
MAX810STR	2.93		SPY	SOT−23	
MAX810STRG	2.93		SPY	SOT−23 (Pb−Free)	

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact your ON Semiconductor sales representative for other threshold voltage options.

PACKAGE DIMENSIONS

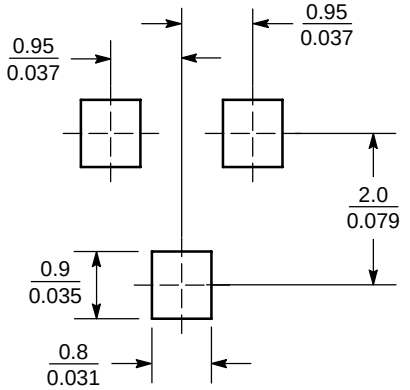
SOT−23 (TO236)
CASE 318−08
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.