General Purpose CMOS Rail-to-Rail Amplifiers

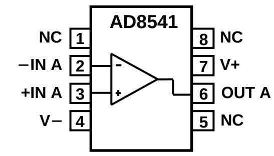
AD8541/AD8542/AD8544

FEATURES
- **Single Supply Operation: +2.7 V to +5.5 V**
- **Low Supply Current: 45 μA/Amplifier**
- **Wide Bandwidth: 1 MHz**
- **No Phase Reversal**
- **Low Input Currents: 4 pA**
- **Unity Gain Stable**
- **Rail-to-Rail Input and Output**

APPLICATIONS
- **ASIC Input or Output Amplifier**
- **Sensor Interface**
- **Piezo Electric Transducer Amplifier**
- **Medical Instrumentation**
- **Mobile Communication**
- **Audio Output**
- **Portable Systems**

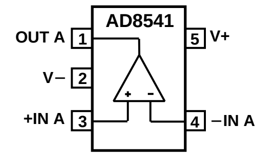
PIN CONFIGURATIONS

SO-8

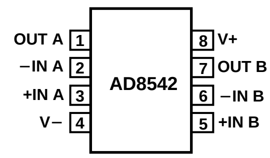


NC = NO CONNECT

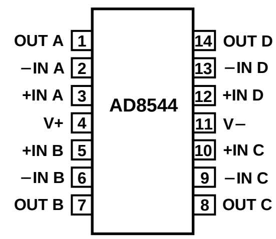
SOT-23-5 (RT)



SO-8 (R) and RU-8



SO-14 and RU-14



GENERAL DESCRIPTION

The AD8541/AD8542/AD8544 are single, dual and quad rail-to-rail input and output single supply amplifiers featuring very low supply current and 1 MHz bandwidth. All are guaranteed to operate from a +2.7 V single supply as well as a +5 V supply. These parts provide 1 MHz bandwidth at low current consumption of 45 μA per amplifier.

Very low input bias currents enable the AD8541/AD8542/AD8544 to be used for integrators, photodiode amplifiers, piezo electric sensors and other applications with high source impedance. Supply current is only 45 μA per amplifier, ideal for battery operation.

Rail-to-rail inputs and outputs are useful to designers buffering ASICs in single supply systems. The AD8541/AD8542/AD8544 are optimized to maintain high gains at lower supply voltages, making them useful for active filters and gain stages.

The AD8541/AD8542/AD8544 are specified over the extended industrial (–40°C to +125°C) temperature range. The AD8541 is available in 8-lead SO and 5-lead SOT-23 packages. The AD8542 is available in 8-lead SO and 8-lead TSSOP surface mount packages. The AD8544 is available in 14-lead narrow SO-14 and 14-lead TSSOP surface mount packages. All TSSOP and SOT versions are available in tape and reel only.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD8541/AD8542/AD8544–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +2.7 V, V_{CM} = +1.35 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD8541, AD8542	V_{OS}			1	6	mV
		–40°C ≤ T_A ≤ +125°C			7	mV
Input Bias Current	I_B			4	60	pA
		–40°C ≤ T_A ≤ +85°C			100	pA
		–40°C ≤ T_A ≤ +125°C			1,000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		–40°C ≤ T_A ≤ +85°C			50	pA
		–40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		+2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +2.7 V	40	45		dB
		–40°C ≤ T_A ≤ +125°C	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ , V_O = +0.5 V to +2.2 V	100	500		V/mV
		–40°C ≤ T_A ≤ +85°C	50			V/mV
		–40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	–40°C ≤ T_A ≤ +85°C		100		fA/°C
		–40°C ≤ T_A ≤ +125°C		2,000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	+2.575	+2.65		V
		–40°C ≤ T_A ≤ +125°C	+2.550			V
Output Voltage Low	V_{OL}	I_L = 1 mA		35	100	mV
		–40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}	V_{OUT} = V_S – 1 V		15		mA
	$\pm I_{SC}$			±20		mA
Closed Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +6 V	65	76		dB
		–40°C ≤ T_A ≤ +125°C	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		38	55	µA
		–40°C ≤ T_A ≤ +125°C			75	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ	0.4	0.75		V/µs
Settling Time	t_S	To 0.1% (1 V Step)		5		µs
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	Φo			63		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		40		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = +3.0 V, V_{CM} = +1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD8541, AD8542	V_{OS}			1	6	mV
		–40°C ≤ T_A ≤ +125°C			7	mV
Input Bias Current	I_B			4	60	pA
		–40°C ≤ T_A ≤ +85°C			100	pA
		–40°C ≤ T_A ≤ +125°C			1,000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		–40°C ≤ T_A ≤ +85°C			50	pA
		–40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +3 V	40	45		dB
		–40°C ≤ T_A ≤ +125°C	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ , V_O = +0.5 V to +2.2 V	100	500		V/mV
		–40°C ≤ T_A ≤ +85°C	50			V/mV
		–40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	–40°C ≤ T_A ≤ +85°C		100		fA/°C
		–40°C ≤ T_A ≤ +125°C		2,000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	+2.875	+2.955		V
		–40°C ≤ T_A ≤ +125°C	+2.850			V
Output Voltage Low	V_{OL}	I_L = 1 mA		32	100	mV
		–40°C ≤ T_A ≤ +125°C			125	mV
Output Current	I_{OUT}	V_{OUT} = V_S – 1 V		18		mA
	$\pm I_{SC}$			±25		mA
Closed Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +6 V	65	76		dB
		–40°C ≤ T_A ≤ +125°C	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		40	60	µA
		–40°C ≤ T_A ≤ +125°C			75	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ	0.4	0.8		V/µs
Settling Time	t_S	To 0.01% (1 V Step)		5		µs
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	Φo			64		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

Specifications subject to change without notice.

AD8541/AD8542/AD8544–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD8541, AD8542	V_{OS}			1	6	mV
		$-40°C \le T_A \le +125°C$			7	mV
Input Bias Current	I_B			4	60	pA
		$-40°C \le T_A \le +85°C$			100	pA
		$-40°C \le T_A \le +125°C$			1,000	pA
Input Offset Current	I_{OS}			0.1	30	pA
		$-40°C \le T_A \le +85°C$			50	pA
		$-40°C \le T_A \le +125°C$			500	pA
Input Voltage Range			0		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +5 V	40	48		dB
		$-40°C \le T_A \le +125°C$	38			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ , V_O = +0.5 V to +2.2 V	20	40		V/mV
		$-40°C \le T_A \le +85°C$	10			V/mV
		$-40°C \le T_A \le +125°C$	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +125°C$		4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	$-40°C \le T_A \le +85°C$		100		fA/°C
		$-40°C \le T_A \le +125°C$		2,000		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40°C \le T_A \le +125°C$		25		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	+4.9	+4.965		V
		$-40°C \le T_A \le +125°C$	+4.875			V
Output Voltage Low	V_{OL}	I_L = 1 mA		25	100	mV
		$-40°C \le T_A \le +125°C$			125	mV
Output Current	I_{OUT}	$V_{OUT} = V_S - 1$ V		30		mA
	$\pm I_{SC}$			±60		mA
Closed Loop Output Impedance	Z_{OUT}	f = 200 kHz, A_V = 1		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +6 V	65	76		dB
		$-40°C \le T_A \le +125°C$	60			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		45	65	µA
		$-40°C \le T_A \le +125°C$			85	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 200 pF	0.45	0.92		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		70		kHz
Settling Time	t_S	To 0.1% (1 V Step)		6		µs
Gain Bandwidth Product	GBP			1,000		kHz
Phase Margin	Φo			67		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
	e_n	f = 10 kHz		38		nV/√Hz
Current Noise Density	i_n			<0.1		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage(V_S) . . . . +6 V
Input Voltage . . . . GND to V_S
Differential Input Voltage[2] . . . . ±6 V
Storage Temperature Range
  R, RT, RU Packages . . . . –65°C to +150°C
Operating Temperature Range
  AD8541/AD8542/AD8544 . . . . –40°C to +125°C
Junction Temperature Range
  R, RT, RU Packages . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]For supplies less than +6 V, the differential input voltage is equal to $\pm V_S$.

PACKAGE INFORMATION

Package Type	θ_{JA}[1]	θ_{JC}	Units
5-Lead SOT-23 (RT)	256	81	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

NOTE

[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered onto a circuit board for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8541AR	–40°C to +125°C	8-Lead SOIC	SO-8
AD8541ART[1,2]	–40°C to +125°C	5-Lead SOT-23	RT-5
AD8542AR	–40°C to +125°C	8-Lead SOIC	SO-8
AD8542ARU[3]	–40°C to +125°C	8-Lead TSSOP	RU-8
AD8544AR	–40°C to +125°C	14-Lead SOIC	SO-14
AD8544ARU[3]	–40°C to +125°C	14-Lead TSSOP	RU-14

NOTES

[1]Available in 2,500 piece reels only.

[2]AD8541ART is marked A4A.

[3]Available in 3,500 or 10,000 piece reels.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8541/AD8542/AD8544 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

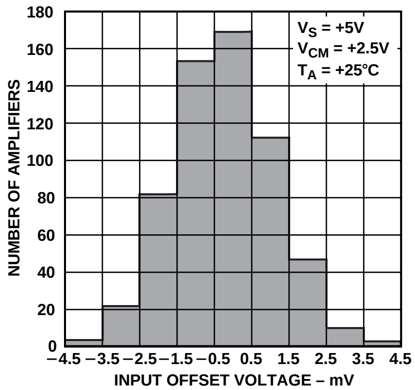


Figure 1. Input Offset Voltage Distribution

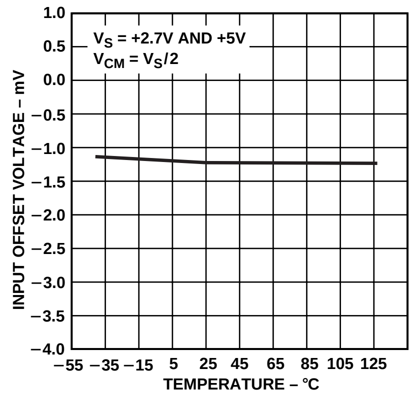


Figure 2. Input Offset Voltage vs. Temperature

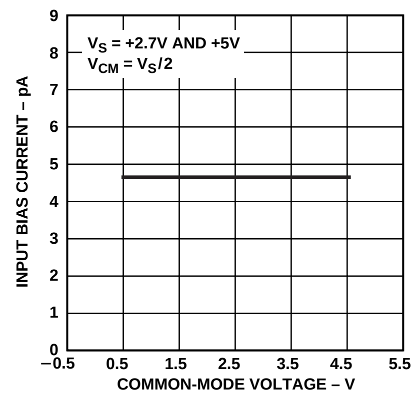


Figure 3. Input Bias Current vs. Common-Mode Voltage

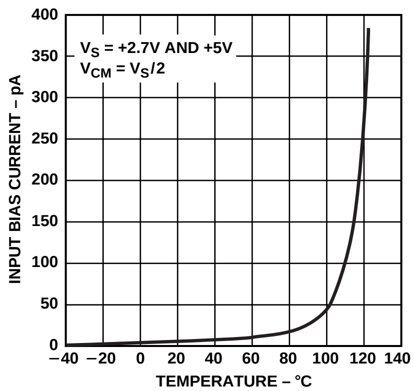


Figure 4. Input Bias Current vs. Temperature

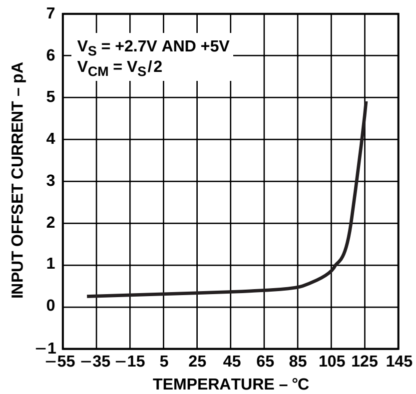


Figure 5. Input Offset Current vs. Temperature

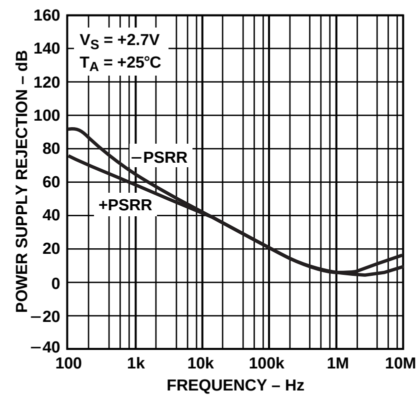


Figure 6. Power Supply Rejection Ratio vs. Frequency

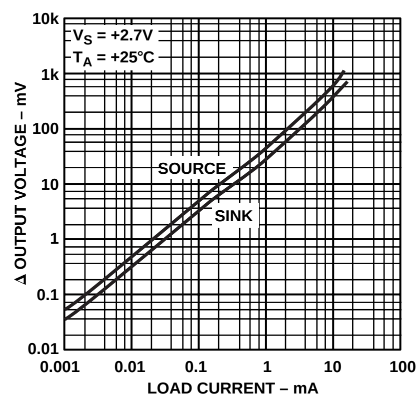


Figure 7. Output Voltage to Supply Rail vs. Load Current

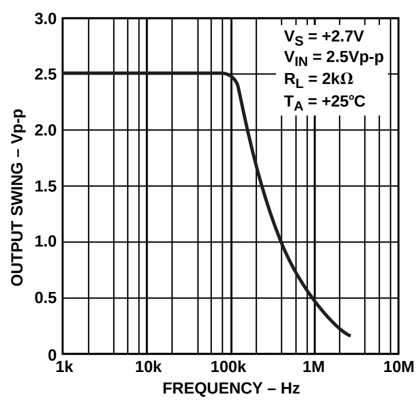


Figure 8. Closed-Loop Output Voltage Swing vs. Frequency

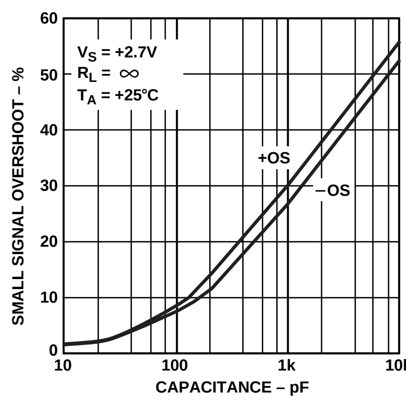


Figure 9. Small Signal Overshoot vs. Load Capacitance

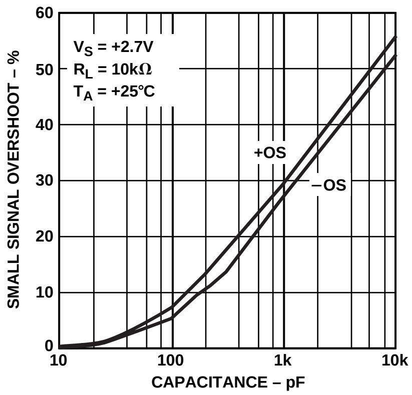


Figure 10. Small Signal Overshoot vs. Load Capacitance

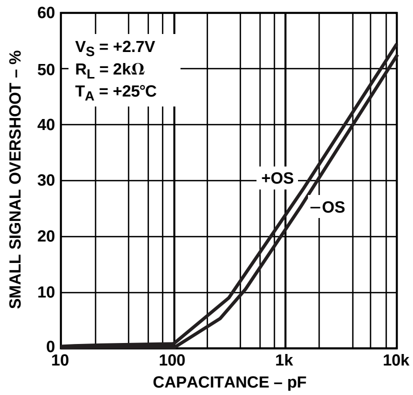


Figure 11. Small Signal Overshoot vs. Load Capacitance

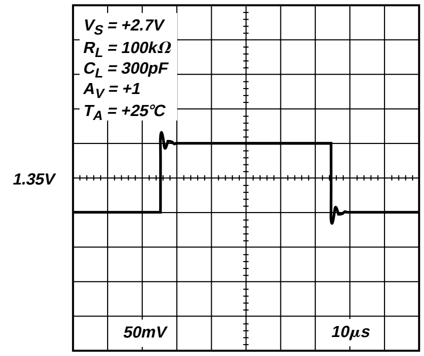


Figure 12. Small Signal Transient Response

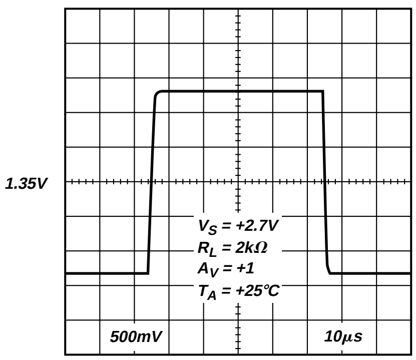


Figure 13. Large Signal Transient Response

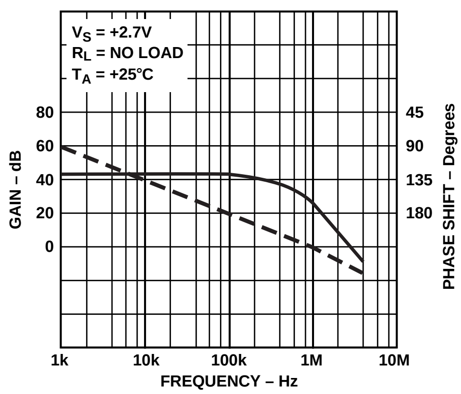


Figure 14. Open-Loop Gain and Phase vs. Frequency

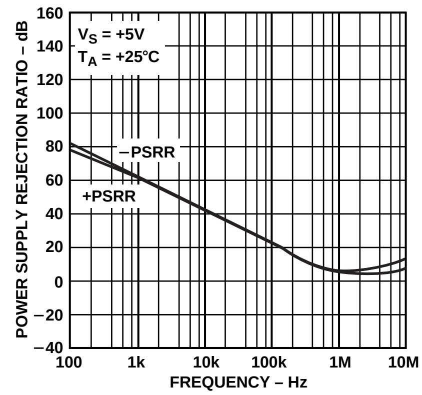


Figure 15. Power Supply Rejection Ratio vs. Frequency

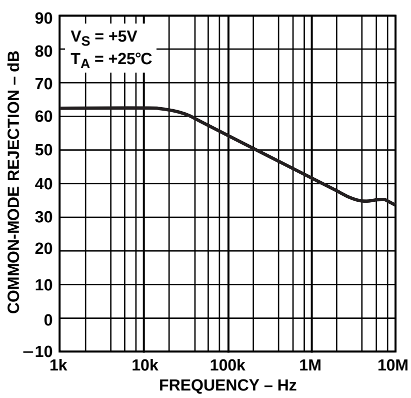


Figure 16. Common-Mode Rejection Ratio vs. Frequency

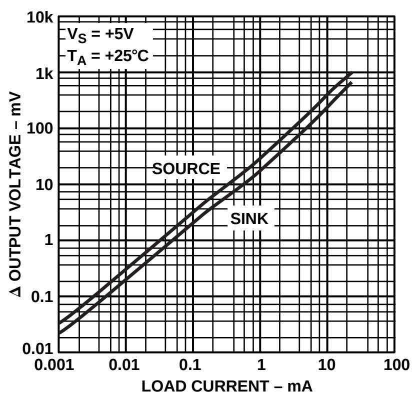


Figure 17. Output Voltage to Supply Rail vs. Frequency

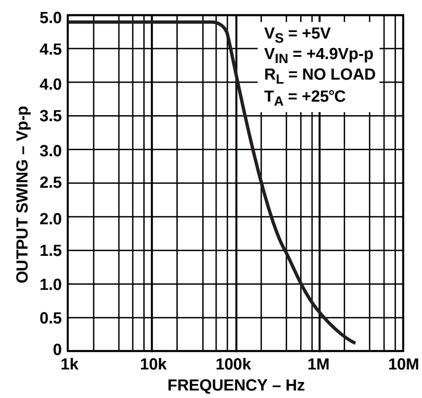


Figure 18. Closed Loop Output Voltage Swing vs. Frequency

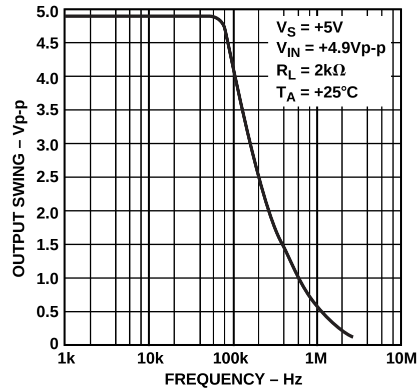


Figure 19. Closed-Loop Output Voltage Swing vs. Frequency

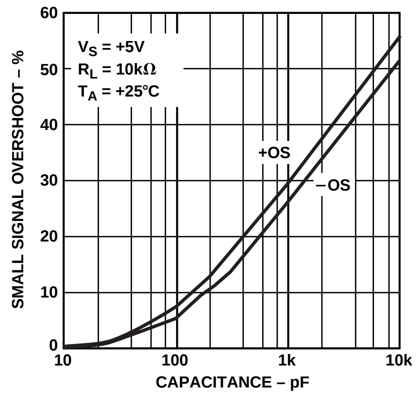


Figure 20. Small Signal Overshoot vs. Load Capacitance

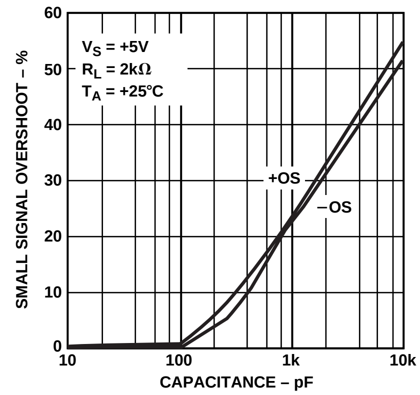


Figure 21. Small Signal Overshoot vs. Load Capacitance

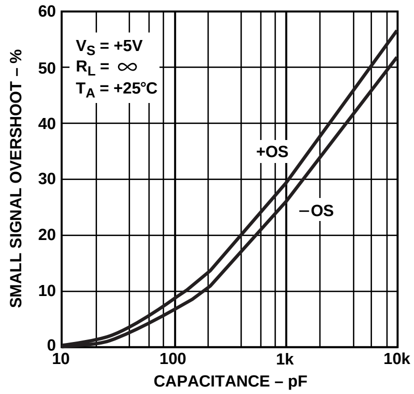


Figure 22. Small Signal Overshoot vs. Load Capacitance

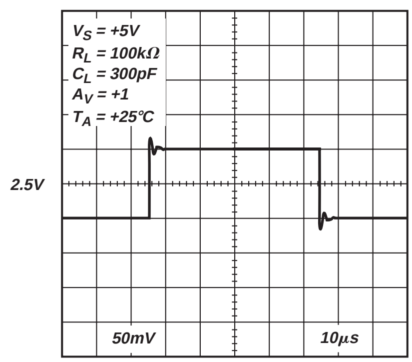


Figure 23. Small Signal Transient Response

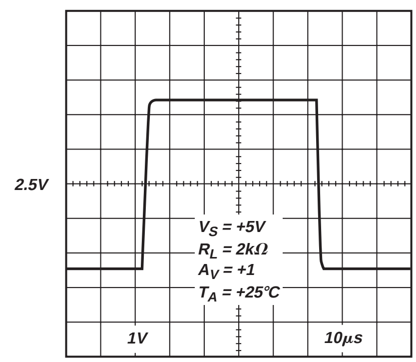


Figure 24. Large Signal Transient Response

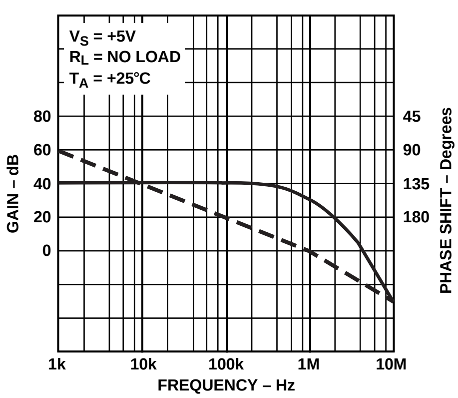


Figure 25. Open-Loop Gain & Phase vs. Frequency

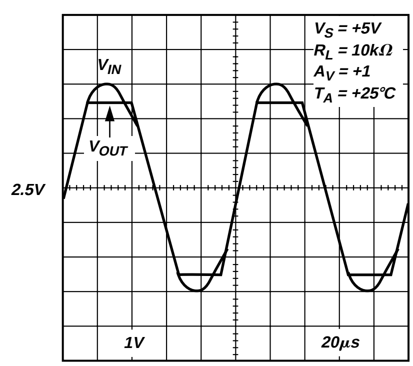


Figure 26. No Phase Reversal

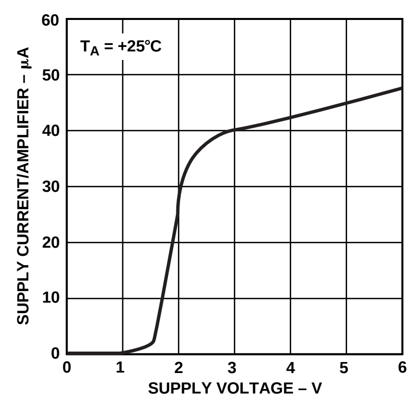


Figure 27. Supply Current per Amplifier vs. Supply Voltage

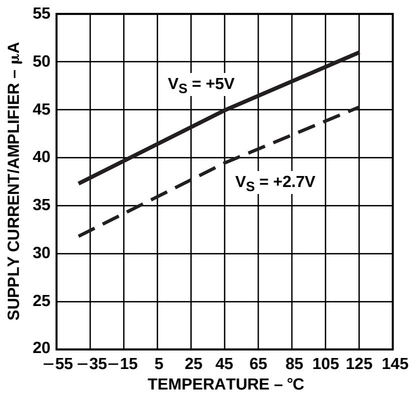


Figure 28. Supply Current per Amplifier vs. Temperature

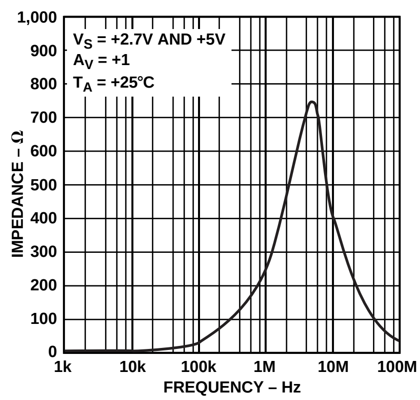


Figure 29. Closed-Loop Output Impedance vs. Frequency

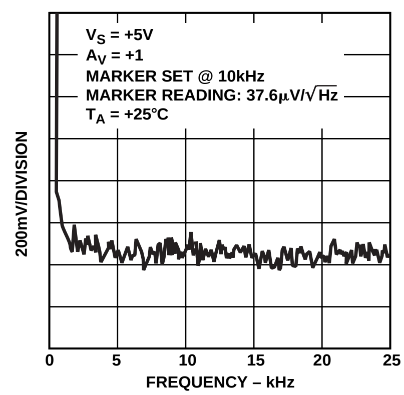


Figure 30. Voltage Noise

NOTES ON THE AD854x AMPLIFIERS

The AD8541/AD8542/AD8544 amplifiers are improved performance general purpose operational amplifiers. Performance has been improved over previous amplifiers in several ways.

Lower Supply Current for 1 MHz Gain Bandwidth

The AD854x series typically uses 45 microamps of current per amplifier. This is much less than the 200 µA to 700 µA used in earlier generation parts with similar performance. This makes the AD854x series a good choice for upgrading portable designs for longer battery life. Alternatively, additional functions and performance can be added at the same current drain.

Higher Output Current

At +5 V single supply, the short circuit current is typically 60 µA. Even 1 V from the supply rail, the AD854x amplifiers can provide 30 mA, sourcing or sinking.

Sourcing and sinking is strong at lower voltages, with 15 mA available at +2.7 V, and 18 mA at 3.0 V. For even higher output currents, please see the Analog Devices AD8531/AD853/AD8534 parts, with output currents to 250 mA. Information on these parts is available from your Analog Devices representative, and datasheets are available at the Analog Devices website at www.analog.com.

Better Performance at Lower Voltages

The AD854x family parts have been designed to provide better ac performance, at 3.0 V and 2.7 V, than previously available parts. Typical gain-bandwidth product is close to 1 MHz at 2.7 V. Voltage gain at 2.7 V and 3.0 V is typically 500,000. Phase margin is typically over +60°C, making the part easy to use.

APPLICATIONS

Notch Filter

The AD8542 has very high open loop gain (especially with supply voltage below 4 V), which makes it useful for active filters of all types. For example, Figure 31 illustrates the AD8542 in the classic Twin-T Notch Filter design. The Twin-T Notch is desired for simplicity, low output impedance and minimal use of op amps. In fact, this notch filter may be designed with only one op amp if Q adjustment is not required. Simply remove U2 as illustrated in Figure 32. However, a major drawback to this circuit topology is ensuring that all the Rs and Cs closely match. The components must closely match or notch frequency offset and drift will cause the circuit to no longer attenuate at the ideal notch frequency. To achieve desired performance, 1% or better component tolerances or special component screens are usually required. One method to desensitize the circuit-to-component mismatch is to increase R2 with respect to R1, which lowers Q. A lower Q increases attenuation over a wider frequency range, but reduces attenuation at the peak notch frequency.

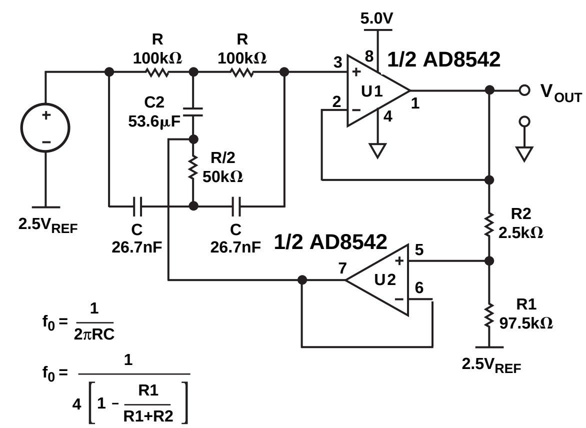


Figure 31. 60 Hz Twin-T Notch Filter, Q = 10

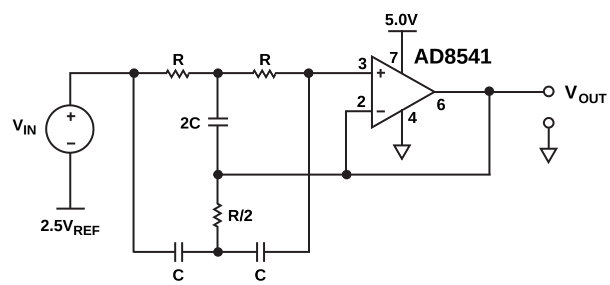


Figure 32. 60 Hz Twin-T Notch Filter, Q = ∞ (Ideal)

Figure 33 diagrams another example of the AD8542 in a notch filter circuit. The FNDR notch filter has several unique features as compared to the Twin-T Notch including: less critical matching requirements; Q is directly proportional to a single resistor R1. While matching component values is still important, it is also much easier and/or less expensive to accomplish in the FNDR circuit. For example, the Twin-T Notch uses three capacitors with two unique values, whereas the FNDR circuit uses only two capacitors, which may be of the same value. U3 is simply a buffer that is added to lower the output impedance of the circuit.

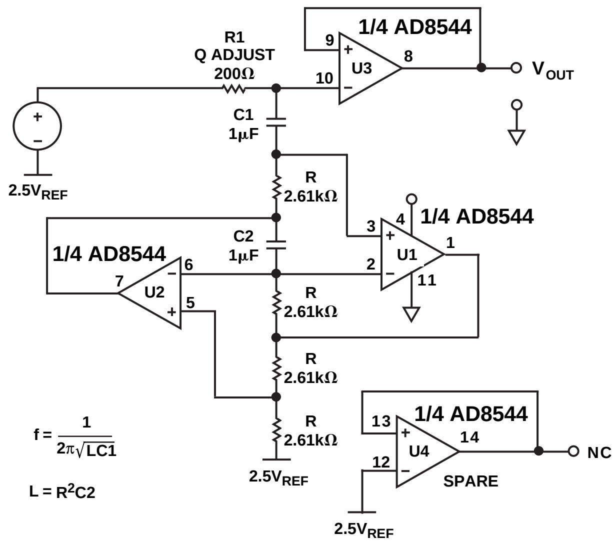


Figure 33. FNDR 60 Hz Notch Filter with Output Buffer

Comparator Function

A comparator function is a common application for a spare op amp in a quad package. Figure 34 illustrates 1/4 of the AD8544 as a comparator in a standard overload detection application. Unlike so many op amps, the AD854x family can double as comparator because this op amp family has rail-to-rail differential input range, rail-to-rail output, and a great speed vs. power ratio. R2 is used to introduce hysteresis. The AD854x when used as comparators have 5 μs propagation delay @ 5 V and 5 μs overload recovery time.

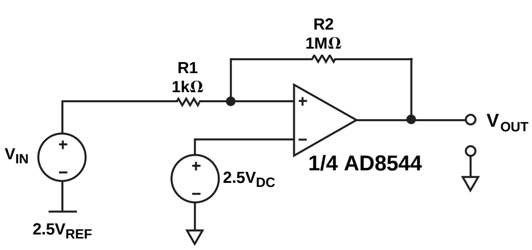


Figure 34. The AD854x Comparator Application–Overload Detector

Photodiode Application

The AD854x family has very high impedance with input bias current typically around 4 pA. This characteristic allows the AD854x op amps to be used in photodiode applications and other applications that require high input impedance. Note that the AD854x has significant voltage offset, which can be removed by capacitive coupling or software calibration.

Figure 35, illustrates a photodiode or current measurement application. The feedback resistor is limited to 10 MΩ to avoid excessive output offset. Also note that a resistor is not needed on the noninverting input to cancel bias current offset, because the bias current related output offset is not significant when compared to the voltage offset contribution. For the best performance follow the standard high impedance layout techniques including: shield circuit, clean circuit board, put a trace connected to the noninverting input around the inverting input, and use separate analog and digital power supplies.

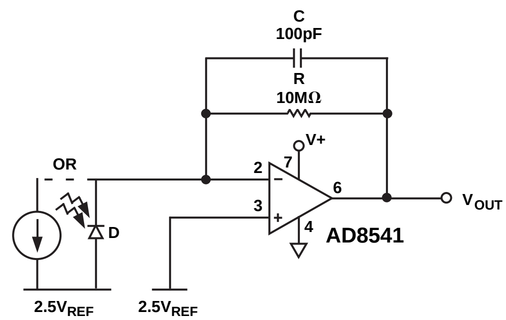


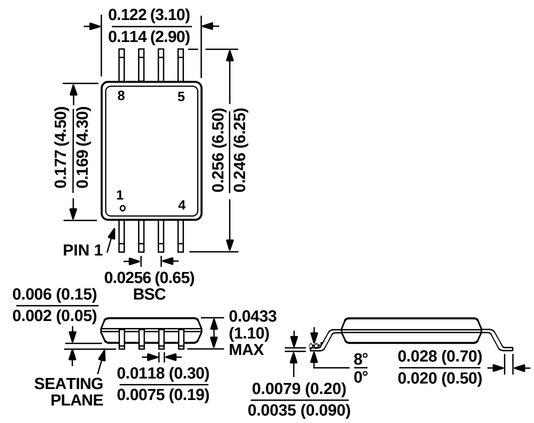
Figure 35. High Input Impedance Application–Photodiode Amplifier

```
* AD8542 SPICE Macro-model Typical Values
* 6/98, Ver. 1
* TAM / ADSC
*
* Copyright 1998 by Analog Devices
*
* Refer to “README.DOC” file for License State-
 ment.  Use of this
* model indicates your acceptance of the terms
 and provisions in
* the License Statement.
*
* Node Assignments
*                  noninverting input
*                  |   inverting input
*                  |   |    positive supply
*                  |   |    |   negative supply
*                  |   |    |   |   output
*                  |   |    |   |   |
*                  |   |    |   |   |
.SUBCKT AD8542     1   2   99  50  45
*
* INPUT STAGE
*
M1   4  1 8 8 PIX L=0.6E-6 W=16E-6
M2   6  7 8 8 PIX L=0.6E-6 W=16E-6
M3  11  1 10 10 NIX L=0.6E-6 W=16E-6
M4  12  7 10 10 NIX L=0.6E-6 W=16E-6
RC1  4 50 20E3
RC2  6 50 20E3
RC3 99 11 20E3
RC4 99 12 20E3
C1   4  6 1.5E-12
C2  11 12 1.5E-12
I1  99  8 1E-5
I2  10 50 1E-5
V1  99  9 0.2
V2  13 50 0.2
D1   8  9 DX
D2  13 10 DX
EOS  7  2 POLY(3) (22,98) (73,98) (81,0) 1E-3 1 1
 1
IOS  1  2 2.5E-12
*
* CMRR 64dB, ZERO AT 20kHz
*
ECM1 21 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 21 22 79.6E3
CCM1 21 22 100E-12
RCM2 22 98 50
*
* PSRR=90dB, ZERO AT 200Hz
*
RPS1 70  0 1E6
RPS2 71  0 1E6
CPS1 99 70 1E-5
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 1.59E6
CPS3 72 73 500E-12
RPS4 73 98 25
*
* VOLTAGE NOISE REFERENCE OF 35nV/rt(Hz)
*
VN1 80 0 0
RN1 80 0 16.45E-3
HN  81 0 VN1 35
RN2 81 0 1
*
* INTERNAL VOLTAGE REFERENCE
*
VFIX 90 98 DC 1
S1   90 91 (50,99) VSY_SWITCH
VSN1 91 92 DC 0
RSY  92 98 1E3
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 POLY(1) (99,50) 0 3.7E-6
*
* ADAPTIVE GAIN STAGE
* AT Vsy>+4.2, AVol=45  V/mv
* AT Vsy<+3.8, AVol=450 V/mv
*
G1  98 30 POLY(2) (4,6) (11,12) 0 2.5E-5 2.5E-5
VR1 30 31 DC 0
H1  31 98 POLY(2) VR1 VSN1 0 5.45E6 0 0 49.05E9
CF  45 30 10E-12
D3  30 99 DX
D4  50 30 DX
*
* OUTPUT STAGE
*
M5  45 46 99 99 POX L=0.6E-6 W=375E-6
M6  45 47 50 50 NOX L=0.6E-6 W=500E-6
EG1 99 46 POLY(1) (98,30) 1.05 1
EG2 47 50 POLY(1) (30,98) 1.04 1
*
* MODELS
*
.MODEL POX PMOS (LEVEL=2,KP=20E-6,VTO=-
 +1,LAMBDA=0.067)
.MODEL NOX NMOS (LEVEL=2,KP=20E-
 +6,VTO=1,LAMBDA=0.067)
.MODEL PIX PMOS (LEVEL=2,KP=20E-6,VTO=-
 +0.7,LAMBDA=0.01,KF=1E-31)
.MODEL NIX NMOS (LEVEL=2,KP=20E-
 +6,VTO=0.7,LAMBDA=0.01,KF=1E-31)
.MODEL DX D(IS=1E-14)
.MODEL VSY_SWITCH VSWITCH(ROFF=100E3,RON=1,VOFF=-
 +4.2,VON=-3.5)
.ENDS AD8542
```

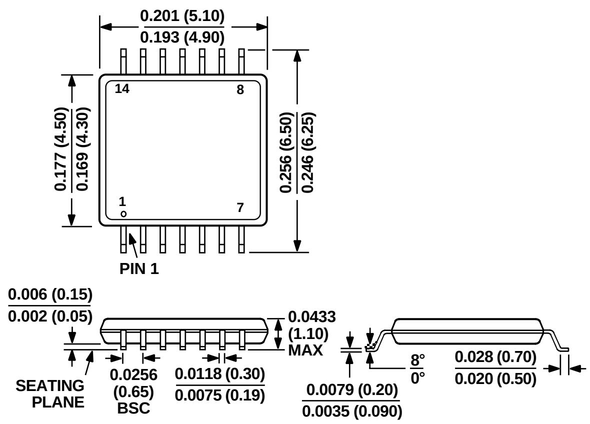
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

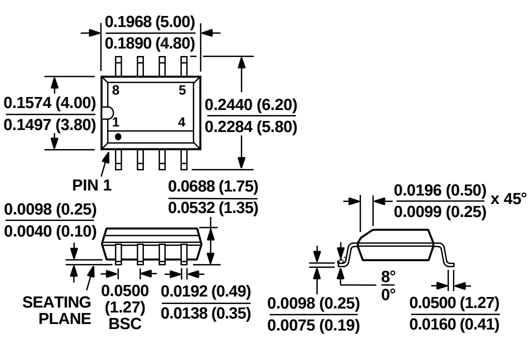
8-Lead TSSOP (RU-08)



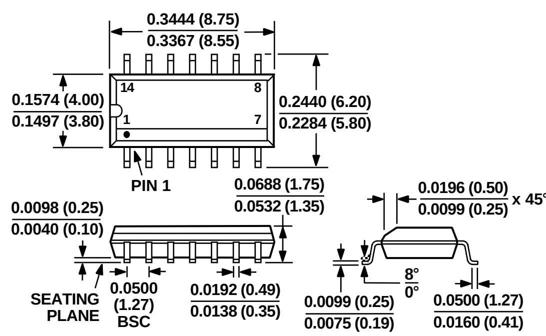
14-Lead TSSOP (RU-14)



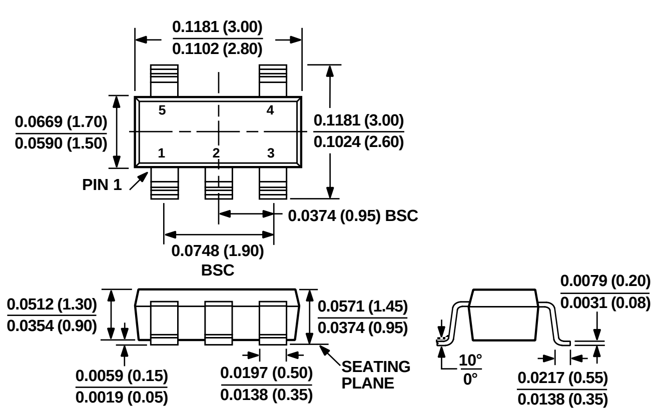
8-Lead SOIC (SO-8)



14-Lead SOIC (SO-14)



5-Lead SOT-23 (RT Suffix)



C3414–8–9/98

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