Comlinear
A National Semiconductor Company

Serial Digital Cable Driver with Adjustable Outputs

CLC006

APPLICATIONS:

- Digital video routers, DAs, switchers
- $4f_{SC}$, 4:2:2 and 360Mbps serial digital video interfaces
- Lower power replacement for GS9008 in most applications
- Cable driver for digital data transmission

FEATURES:

- No external pull-down resistors required
- Two amplitude-adjustable outputs
- 650ps rise and fall times
- Operates from single +5V or -5.2V supply
- Low power dissipation
- DC to >400Mbps

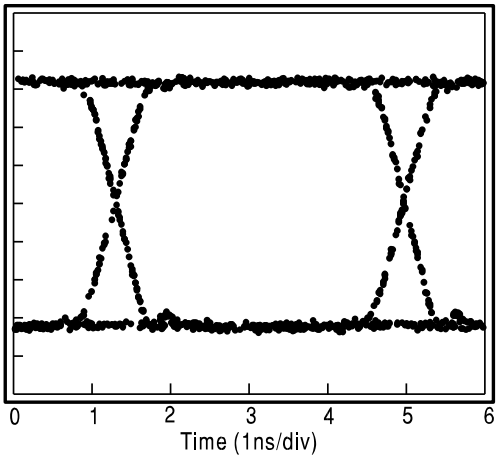
DESCRIPTION

The CLC006 is a monolithic cable driver, designed to conform to the SMPTE 259M standard for the transmission of serial digital video signals. The CLC006 operates at data rates from DC to over 400Mbps, with nominal rise and fall times of 650ps. An internal bandgap reference defines an accurate, low drift, $1.6V_{pp}$ output swing at each of two outputs. When used with a back-matching resistor to drive a terminated cable, the result is a $0.8V_{pp}$ swing at the load. With the addition of one external resistor the output swing may be adjusted from the nominal $1.6V_{pp}$ down to $0.7V_{pp}$. With three external resistors the output swing can be adjusted from $0.7V_{pp}$ to greater than $2V_{pp}$.

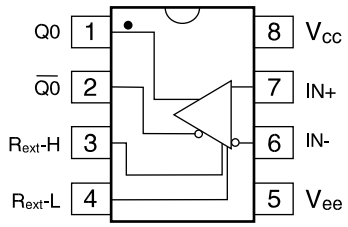
The CLC006 draws less quiescent current than other solutions, and requires no external pull-down resistors to bias the outputs. The result is low power dissipation (185mW with both outputs loaded) and less board space used. The DC coupled differential inputs may be driven with ECL level signals or with DC-shifted ECL signals. Additionally, high voltage gain allows operation with input signal swings that are substantially smaller than ECL swings. As a result, the CLC006 makes an excellent general-purpose, high-speed driver for digital applications.

The CLC006 is packaged in an 8-pin SOIC package and operates from a single +5V or -5.2V power supply.

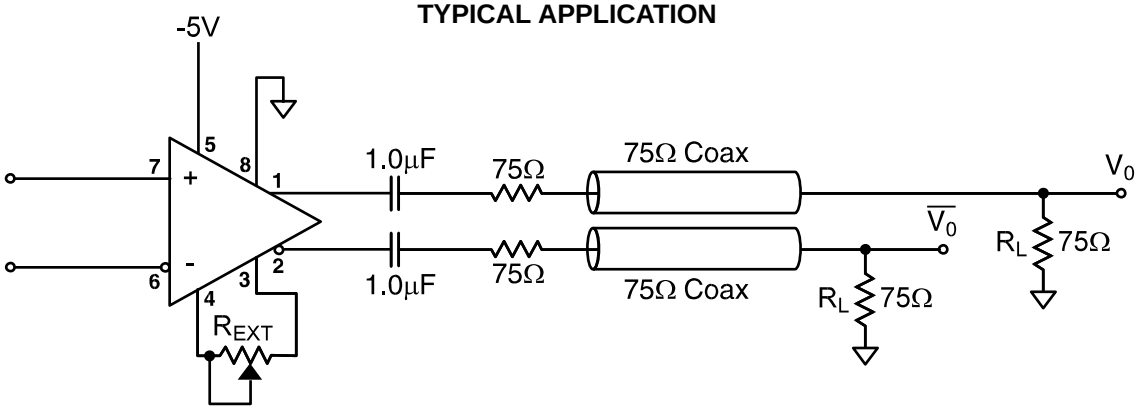
270Mbps Eye Pattern



PINOUT
SOIC



TYPICAL APPLICATION



CLC006 Electrical Characteristics (V_{cc} = 0V, V_{ee} = - 5V; unless specified)

Parameters	Conditions	Typ	Guaranteed MIN/MAX			Units	Notes
Ambient Temperature	CLC006AJE	+25˚C	+25˚C	0 to 70˚C	-40 to 85˚C		
STATIC DC PERFORMANCE							
supply current	no load	34	37	39	39	mA	
supply current	driving 2 loads	37				mA	
input bias current		10	30	50	50	µA	
output HIGH voltage		-1.7				V	
output LOW voltage		-3.3				V	
output amplitude	at the load, R_{EXT} = ∞	800	750/850	750/850	750/850	mV_{pp}	1
output amplitude	at the load, R_{EXT} = 10kΩ	610				mV_{pp}	1
common mode input range upper limit		-0.7	-0.8	-0.8	-0.8	V	
common mode input range lower limit		-2.6	-2.5	-2.5	-2.5	V	
minimum differential input amplitude		200	200	200	200	mV	
power supply rejection ratio	V_{ee} supply	26	20	20	20	dB	
AC PERFORMANCE							
output rise & fall time		650	425/825	400/850	400/850	ps	
overshoot		5				%	
propagation delay		1.0				ns	
duty cycle distortion		50				ps	2
residual jitter		25				ps_{pp}	3
MISCELLANEOUS PERFORMANCE							
input capacitance		1.0				pF	
output resistance		5				Ω	
output inductance		6				nH	

Absolute Maximum Ratings

voltage supply	6V
common-mode input voltage	V_{ee} to V_{cc}
differential-mode input voltage	±5V
continuous output current	30mA

Ordering Information

Model	Temperature Range	Description
CLC006AJE	-40˚C to +85˚C	8-pin SOIC

Notes

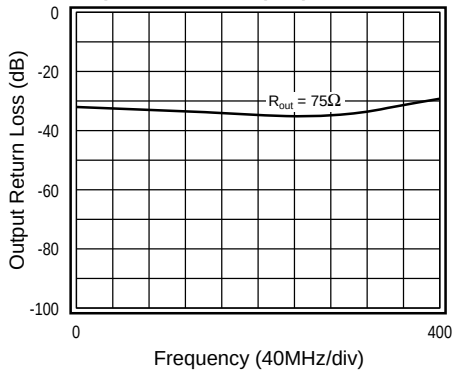
1) Voltage swing at the load as in Figure 2.
2) t_{pd} (low to high) – t_{pd} (high to low).
3) Noise plus pattern-induced components.

CLC006 OPERATION

Device Description

The CLC006 serial digital cable driver is an ECL-compatible buffer designed to meet the requirements of SMPTE 259M. The device drives over 300m of cable (Belden 1505 or 8281) and delivers full ECL swing to a matched 75Ω load up to 400Mbits/s. The CLC006 has two adjustable outputs. The logic swing can be adjusted with external resistors. The output pins of the CLC006 swing twice the load peak-to-peak logic level; the impedance matching network (load and backmatching resistor) cuts this in half. The output resistance is nominally 5Ω.

Output Return Loss (S22)



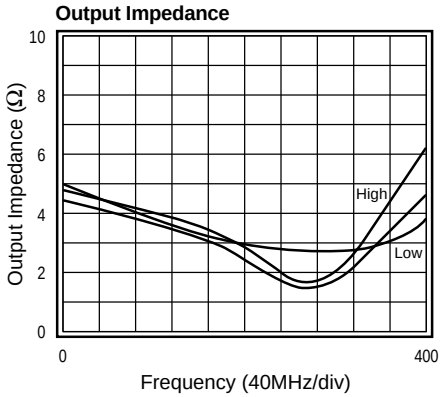
Adding a 75Ω resistor in series with the output yields return loss in compliance with SMPTE standards.

The CLC006 output stage is self-biasing, unlike standard ECL devices. The output stage is a complementary bipolar emitter follower, similar to an op-amp; it does not require a pull-down resistor. Considerable power and cost savings result from this class AB output topology. Typical ECL (class A emitter follower) devices require an emitter load resistor and termination voltage (50Ω & -2V or 150Ω & -5V). The CLC006 cable driver gives full output swing without this added expense. The CLC006 consumes significantly less system power than other cable drivers. The device operates with AC or DC coupled outputs.

Output Interfacing

As with any amplifier, the output impedance is a function of the bias condition of the output transistors. The plot for output impedance shows output impedance in three states; output high, low, alternating high and low. A pull-down (logic high, continuous stream of ones) and a pull-up (logic low, continuous stream of zeros) resistor on the output forces the correct load current for a real measurement of output impedance as a function of logic state. The output impedance graphs also show a curve without a pull-

up/down. While the device would never operate in this DC condition, it does simulate the average output impedance midway between extremes; a continuous stream of alternating zero and one.



Input Interfacing

The CLC006 was designed to be driven directly from ECL outputs. The electrical specifications are guaranteed with differential drive. You may use a single-ended source if you can tolerate some degradation from specified jitter performance at high bit rates. In either case the source must provide bias current to the driven input. Bias the static input with a resistive divider (total resistance 1kΩ) to V_{cc} -1.3V. The following caution on PECL operation is especially important for single-ended drive.

Positive ECL (PECL) Operation

The CLC006 can be used with positive ECL (PECL: V_{cc} = +5V, V_{ee} = 0V) supplies (Figure 1). Due to the AC coupling capacitors on the output, the same ECL peak-to-peak swing levels will appear at the load. ECL output levels are referenced to the positive supply. Keeping clean ground is usually easier than any other voltage. The CLC006 logic internal reference levels are derived from the positive supply, V_{cc}. The PSRR to V_{cc} is low (about 0.5dB). As with any ECL device, PECL operation requires care in bypassing the positive supply. Use 3 bypass capacitors (6.8µF, 0.1µF, 100pF). A choke in series with V_{cc} further reduces supply noise coupling. Keep in mind that the inputs must have a source of bias current. A resistive divider between the supplies set to 3.7V (5V - 1.3V) will both bias the inputs and set the logic threshold. A resistive divider (total series resistance about 1kΩ) at 1.3V below the more positive supply works well.

Output Amplitude Adjustment

The CLC006 needs no external components to drive a 75Ω load to 800mV peak-to-peak. Adding external resistors allows adjustment of the output amplitude. The simplest circuit to reduce the output to <800mV is Figure 2.

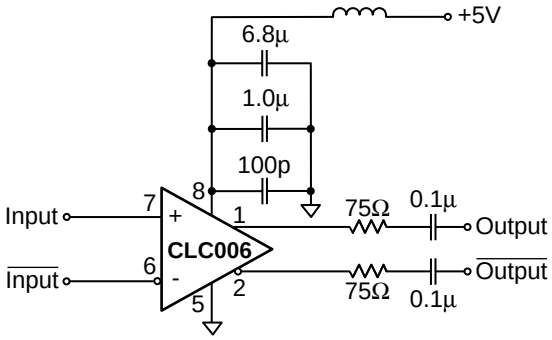
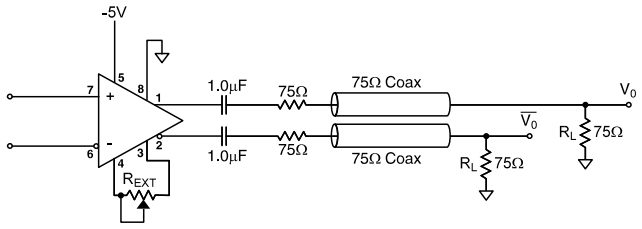


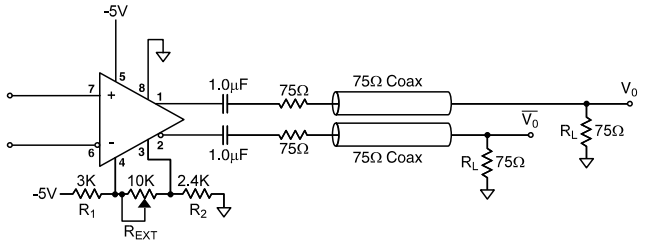
Figure 1. Positive ECL Circuit

One resistor between pins 3 and 4 trims the output from 800mV to a more optimal value to drive some serial digital video receivers. This resistor can be fixed or variable. Find typical resistor/output voltage values in the tables under the suggested schematics. Add bypass capacitors on pins 3 and 4 to reduce output coupling to the reference pins. Omitting them slightly degrades jitter performance from the datasheet specifications. Adding two more resistors (Figure 3) allows the freedom to adjust the output to >800mV, as well as <800mV. With fixed R_1, R_2 (3kΩ, 2.4kΩ, respectively) the table in Figure 3 shows R vs. typical output voltage. For maximum output voltage, R = ∞, R_1 = R_2 = 2.2kΩ. For reduced output only, consider Figure 2 for its simplicity and power supply rejection.



R	Output Voltage (V_{pp} into 75Ω)
open	800mV
30kΩ	755
20k	690
10k	610
5k	550
2k	460
1k	405
0	340

Figure 2. Reduced Output



R	Output Voltage (V_{pp} into 75Ω)
10kΩ	1.02V
5k	905mV
2.6k	755
2k	725
1k	585
0	350

Figure 3. Increasing and Decreasing Output

NOTE: Bypassing pin 3 to ground (0.01µF) may improve transient response in some circuit layouts.

CLC006 Evaluation Board Components

Component	006 used	006 not used
75Ω BNC[1]	V_{in} + ,V_{in} - ,Q_0 $\overline{Q_0}$	Q_1 $\overline{Q_1}$
0.01µF 1206	C_7	
0.1µF 1206	C_1 C_2 C_8	C_3 C_4
33pF[2]	C_5 C_6	
6.8µF 5032 (Digikey #PCT3685)	C_9	
Banana Jack	GND V_{ee}	
deltaV_{out} resistors	See Text	
75Ω 1206	R_7	R_8 R_9
ECL (50Ω/-2V) input termination: R_1, R_3 = 82.5Ω 1206 R_4, R_5 = 127Ω 1206		75Ω input termination: R_1, R_3 = 75Ω 1206 R_4, R_5 not used

[1]Amphenol 31-5329-72RFX.
[2]As required, see text.

Evaluation Board

Comlinear provides a free evaluation board, part number 730056. This board offers provisions to experiment with interfacing and output level adjustment. This board is used by both CLC006 and CLC007 (fixed outputs). The general schematic is Figure 4. Component values for the CLC006 are in the table above. For proper ECL device termination, the inputs must look like 50Ω at -2V. Figure 4 shows how. R2 is for differential input termination. This is most useful for twisted pair termination. Use simple 75Ω input termination to ground for bench testing.

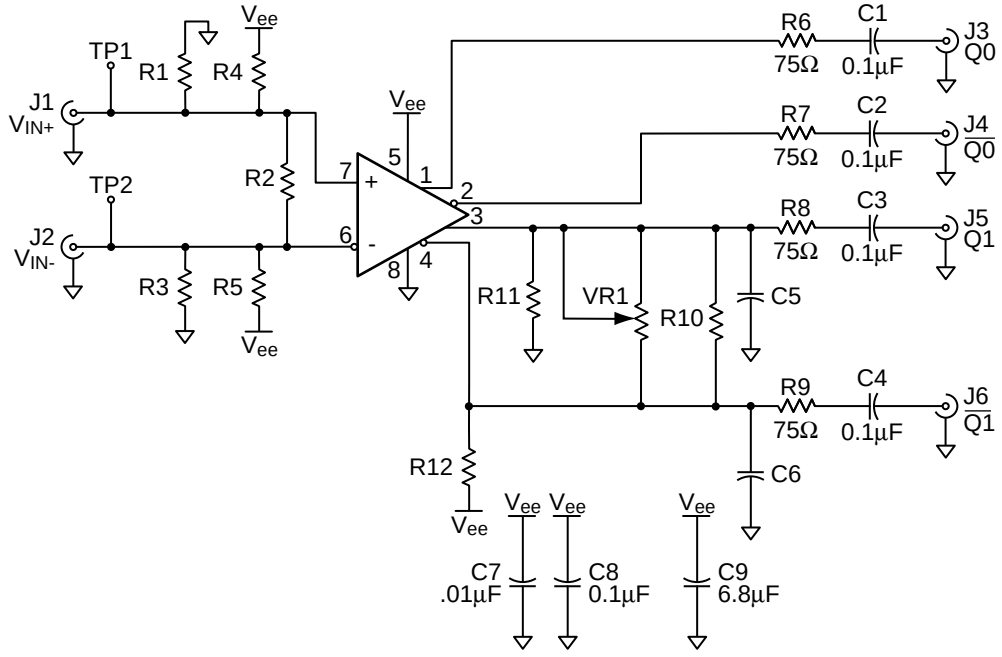


Figure 4. Cable Driver Evaluation Board Schematic

Customer Design Applications Support

Together, Comlinear and National Semiconductor are committed to design excellence. For sales, literature and technical support call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.