National Semiconductor

DS16F95, DS36F95

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December 15, 2009

EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets both EIA-485 and EIA-422A standards.

The DS16F95/DS36F95 offers improved performance due to the use of L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by minimizing gate delay times. Thus, the DS16F95 and DS36F95 consume less power, and feature an extended temperature range as well as improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

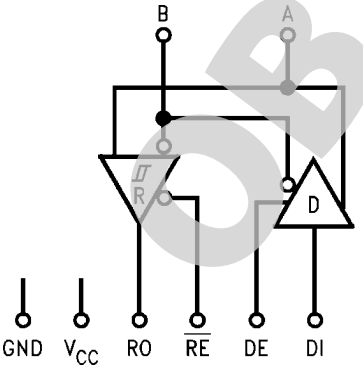
The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHZ) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A
- Military temperature range available
- Qualified for MIL-STD 883C
- Standard Military Drawings (SMD) available
- Available in DIP (J), SOIC (M), LCC (E), and Flatpak (W) packages

Logic Diagram



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Function Tables

Driver

Driver Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A–B	**$\overline{RE}$**	**RO**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

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Absolute Maximum Ratings (*Note 2*)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range	−65°C to +175°C
Lead Temperature	
(Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation (*Note 1*) at 25°C	
'J' Package	1300 mW
'M' Package	735 mW
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS36F95	4.75	5.0	5.25	V
DS16F95	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		+12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	µA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)				
DS36F95	0	+25	+70	°C
DS16F95	−55	+25	+125	°C

Note 1: Derate 'J' package 8.7 mW/°C above 25°C. Derate 'M' package 5.88 mW/°C above 25°C.

Driver Electrical Characteristics (*Note 3*, *Note 4*)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA	0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA	0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.3	V
$\lvert V_{OD1}\rvert$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\lvert V_{OD2}\rvert$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1*		1.5	2.0		
$\Delta\lvert V_{OD}\rvert$	Change in Magnitude of Differential Output Voltage (*Note 5*)	R_L = 54Ω or 100Ω, *Figure 1*	−40°C to +125°C			±0.2	V
			−55°C to +125°C			±0.4	
V_{OC}	Common Mode Output Voltage (*Note 6*)					3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage (*Note 5*)					±0.2	V
I_O	Output Current (*Note 9*) (Includes Receiver I_I)	Output Disabled	V_O = +12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	µA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	µA
I_{OS}	Short Circuit Output Current (*Note 10*)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

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9629 Version 12 Revision 6 Print Date/Time: 2009/12/15 10:38:00

Driver Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	25	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per *Figure 5* Timing per *Figure 6*		300		ns
t_{SKEW}	Skew (Pulse Width Distortion)	R_L = 60Ω, *Figure 3*		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (*Note 7*)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+}-V_{T-}$	Hysteresis (*Note 8*)	V_{CM} = 0V		35	50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 µA, *Figure 2*	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	µA
I_I	Line Input Current (*Note 9*)	Other Input = 0V	V_I = +12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	µA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−50	µA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

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9629 Version 12 Revision 6 Print Date/Time: 2009/12/15 10:38:00

Receiver Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V, C_L = 15 pF, *Figure 7*	14	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	19	24	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	ns
t_{LZ}	Output Disable Time from Low Level			12	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	4.0	ns

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16F95 and across the 0°C to +70°C range for the DS36F95. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 5: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 6: In TIA/EIA-422A and TIA/EIA-485 Standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 7: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 8: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 9: Refer to TIA/EIA-485 Standard for exact conditions.

Note 10: Only one output at a time should be shorted.

Order Number

DS16F95J, NS Package Number J08A

DS36F95J, NS Package Number J08A

DS36F95M, NS Package Number M08A

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Parameter Measurement Information

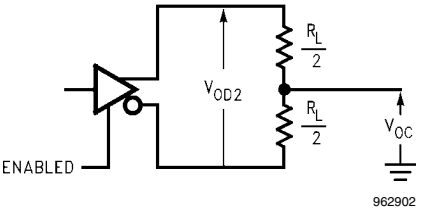


FIGURE 1. Driver V_{OD} and V_{OC} (*Note 14*)

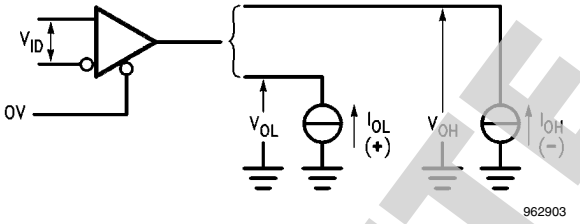
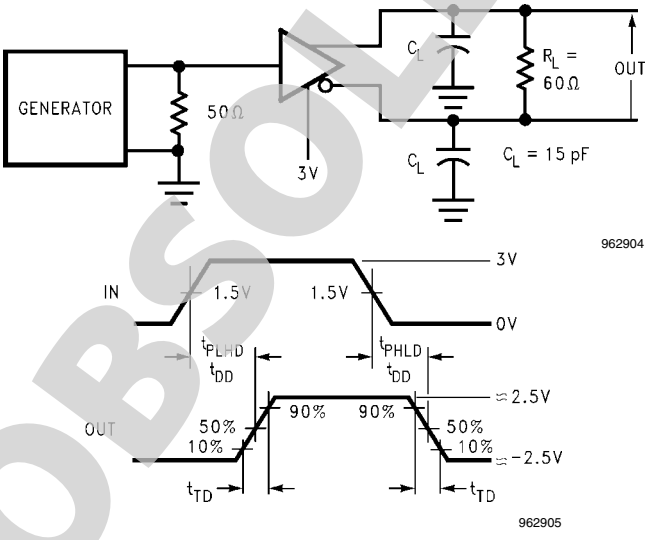
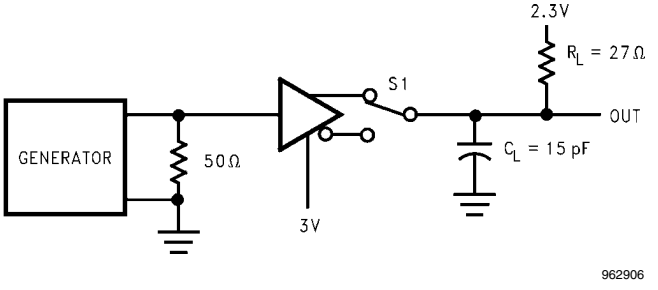


FIGURE 2. Receiver V_{OH} and V_{OL}



$t_{SKEW} = |t_{PLHD} - t_{PHLD}|$

FIGURE 3. Driver Differential Output Delay and Transition Times (*Note 11*, *Note 13*)



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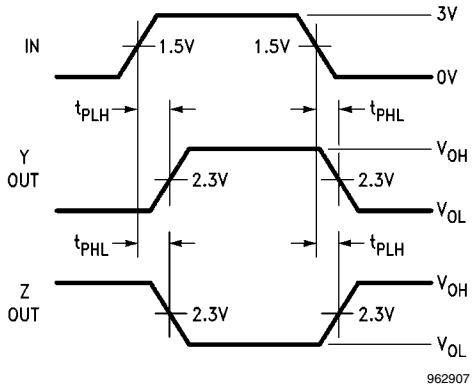

FIGURE 4. Driver Propagation Times (*Note 11*, *Note 12*)

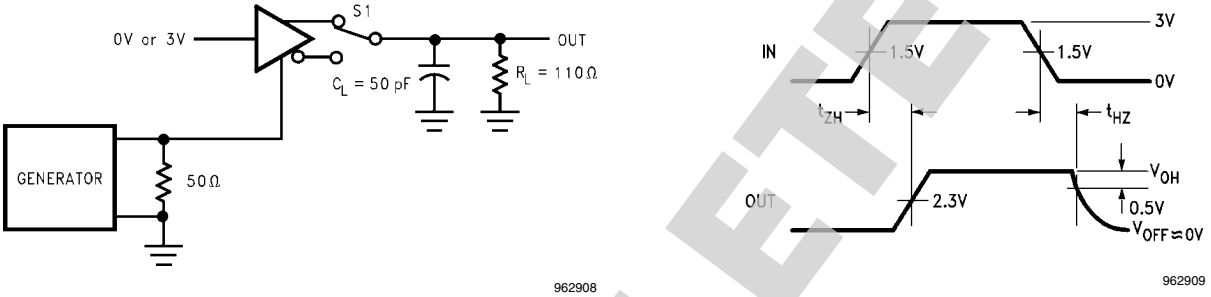

FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ}) (*Note 11*, *Note 12*, *Note 13*)

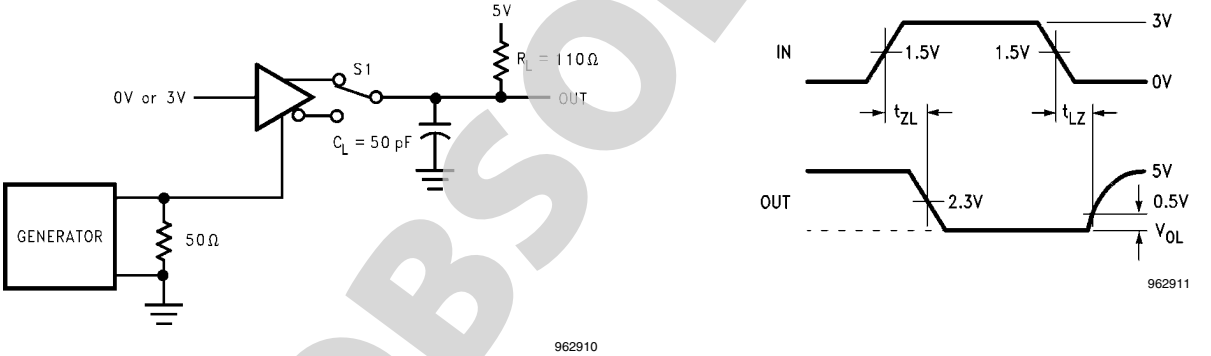

FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ}, t_{LZL}) (*Note 11*, *Note 12*, *Note 13*)

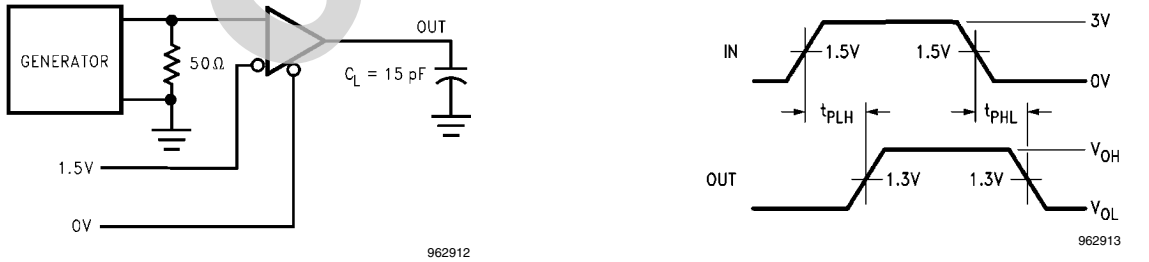

FIGURE 7. Receiver Propagation Delay Times (*Note 11*, *Note 12*)

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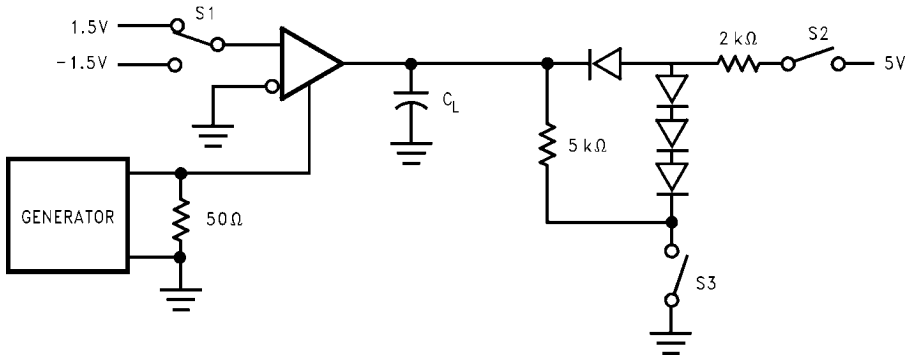

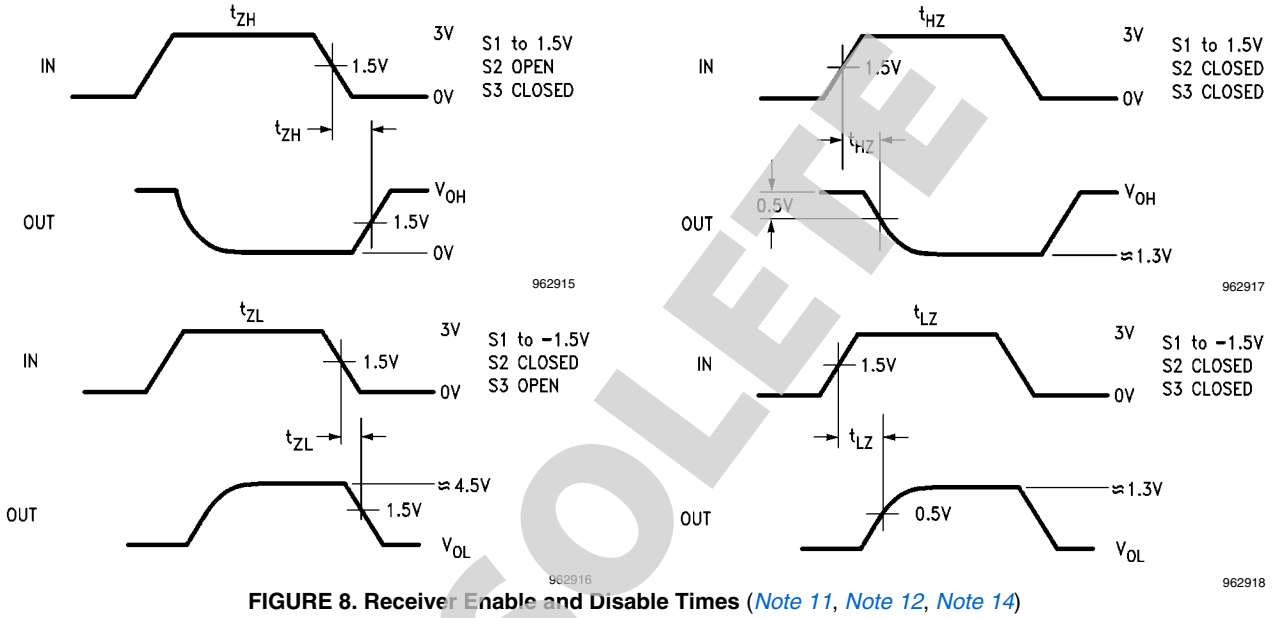

FIGURE 8. Receiver Enable and Disable Times (*Note 11*, *Note 12*, *Note 14*)

Note 11: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 12: C_L includes probe and stray capacitance.

Note 13: DS16F95/DS36F95 Driver enable is Active-High.

Note 14: All diodes are 1N916 or equivalent.

Note 15: Testing at 20 pF assures conformance to 5 pF specification.

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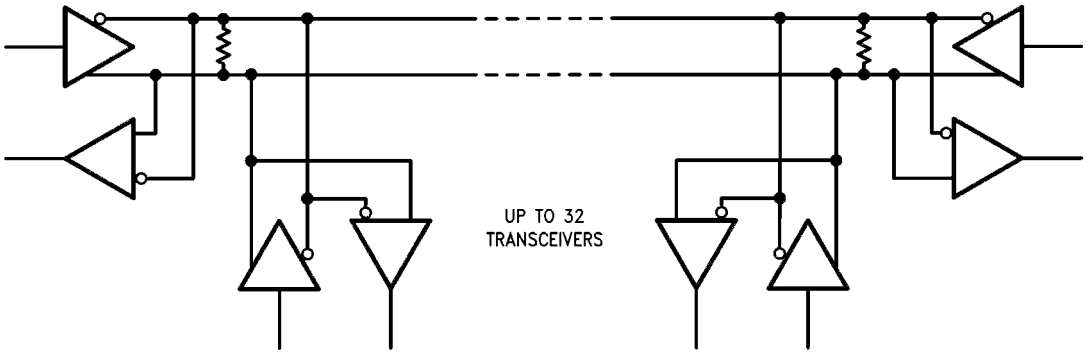
Typical Application



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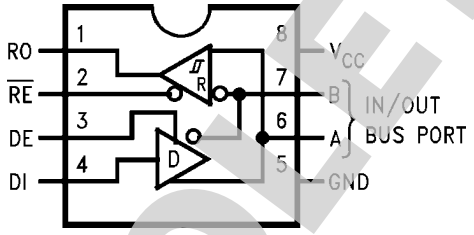
The line should be terminated at both ends in its characteristic impedance, typically 120Ω.
Stub lengths off the main line should be kept as short as possible.

Connection Diagram

8-Lead Dual-In-Line Package or Small Outline Molded Package



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Order Number DS16F95, DS16F95J/883, DS36F95J, DS36F95M
See NS Package Number J08A, or M08A

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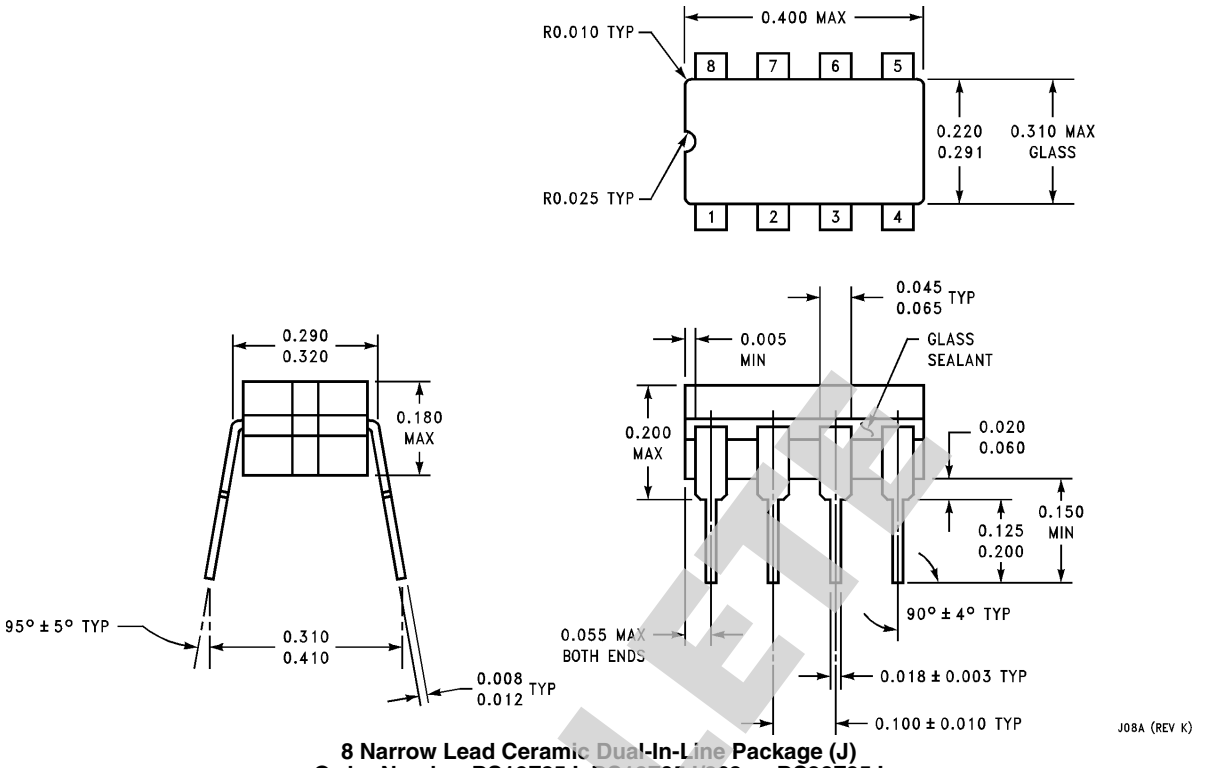
Physical Dimensions inches (millimeters) unless otherwise noted



8 Narrow Lead Ceramic Dual-In-Line Package (J)
Order Number DS16F95J, DS16F95J/883 or DS36F95J
NS Package Number J08A

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Notes

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