

Structure : Silicon Monolithic Integrated Circuit

Product Name : 8bit 12channels · D/A converter (with output buffer)

Model Name : BU2500FV

External Dimensions : Figure 1 (Plastics Mould)

Block Diagram : Figure 2

Applied Circuit Diagram : Figure 3

Features :
 The BU2500FV is an integrated semiconductor of CMOS structure with 12 channels of built-in high quality 8 bit D/A converters with output buffer operational amplifiers of Rail to Rail output type.
 Digital input corresponds to TTL level input.
 Data is inputted by 12 bit 3-wire serial data.
 [Address 4 bit + Data 8 bit]
 It is able to cascading serial use with "Do" terminal.
 Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.
 Adopting compact package of 0.65mm pitch 20 pin.

Application : Adjustment/control of industrial or home-use electric equipment, such as CD-R, CD-R/W, and DVC.

Abusolute Maximum Rating : (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	-0.3~+6.0	V
Upper reference voltage of D/A converter	VDD	-0.3~+6.0	V
Input voltage	VIN	-0.3~+6.0	V
Output voltage	VOOUT	-0.3~+6.0	V
Power dissipation	Pd	400 #	mW
Operating temperture	Toopr	-25~+85	°C
Storage temperture	Tstg	-55~+125	°C

Operating at higher than T a = 25°C, 4mW shall be reduced per 1°C.

Power supply operating voltage range :

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	4.5~5.5	V

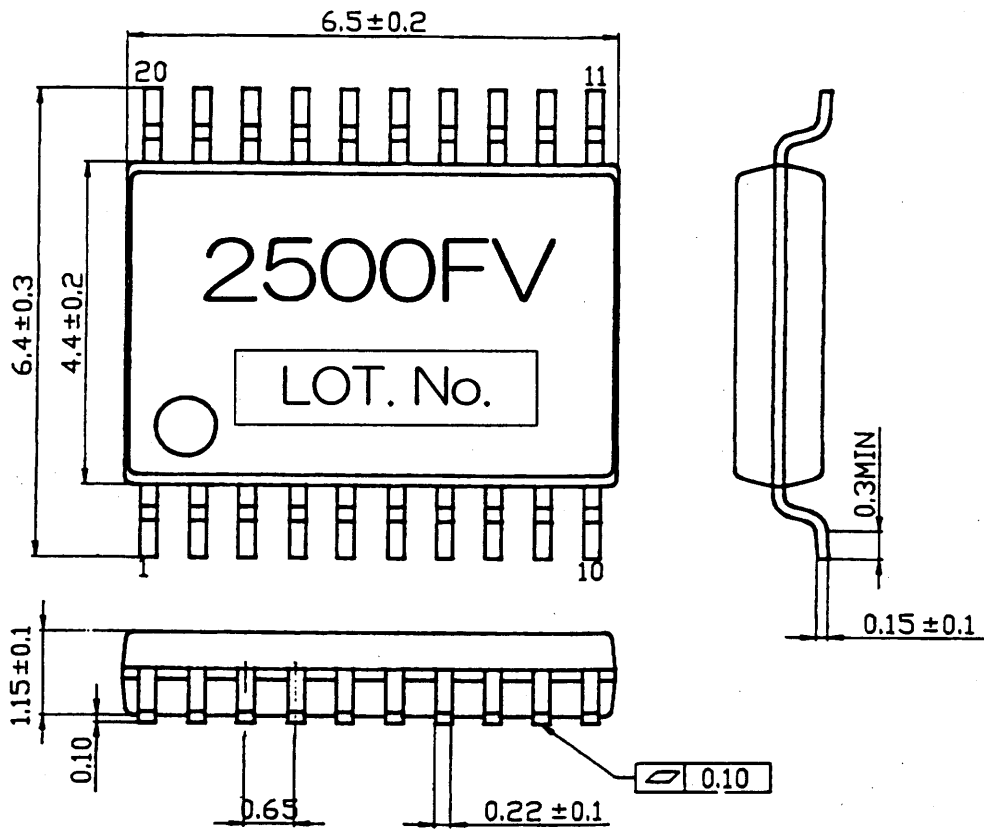
Application example

The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
 When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
 Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
 Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Design <i>M. Onoda</i>	Check <i>K. Nakagawa</i>	Approval <i>S. H. 6/6/00</i>	Date 25 /May./2000	Specification Rev. B
ROHM CO., LTD.			Specification No. TSZ02201-BU2500FV-1-2	



(UNIT : mm)

Figure 1 External Dimensions

Date 25 /May./2000.	Specification
ROHM CO., LTD.	Specification No. TSZ02201-BU2500FV-1-2

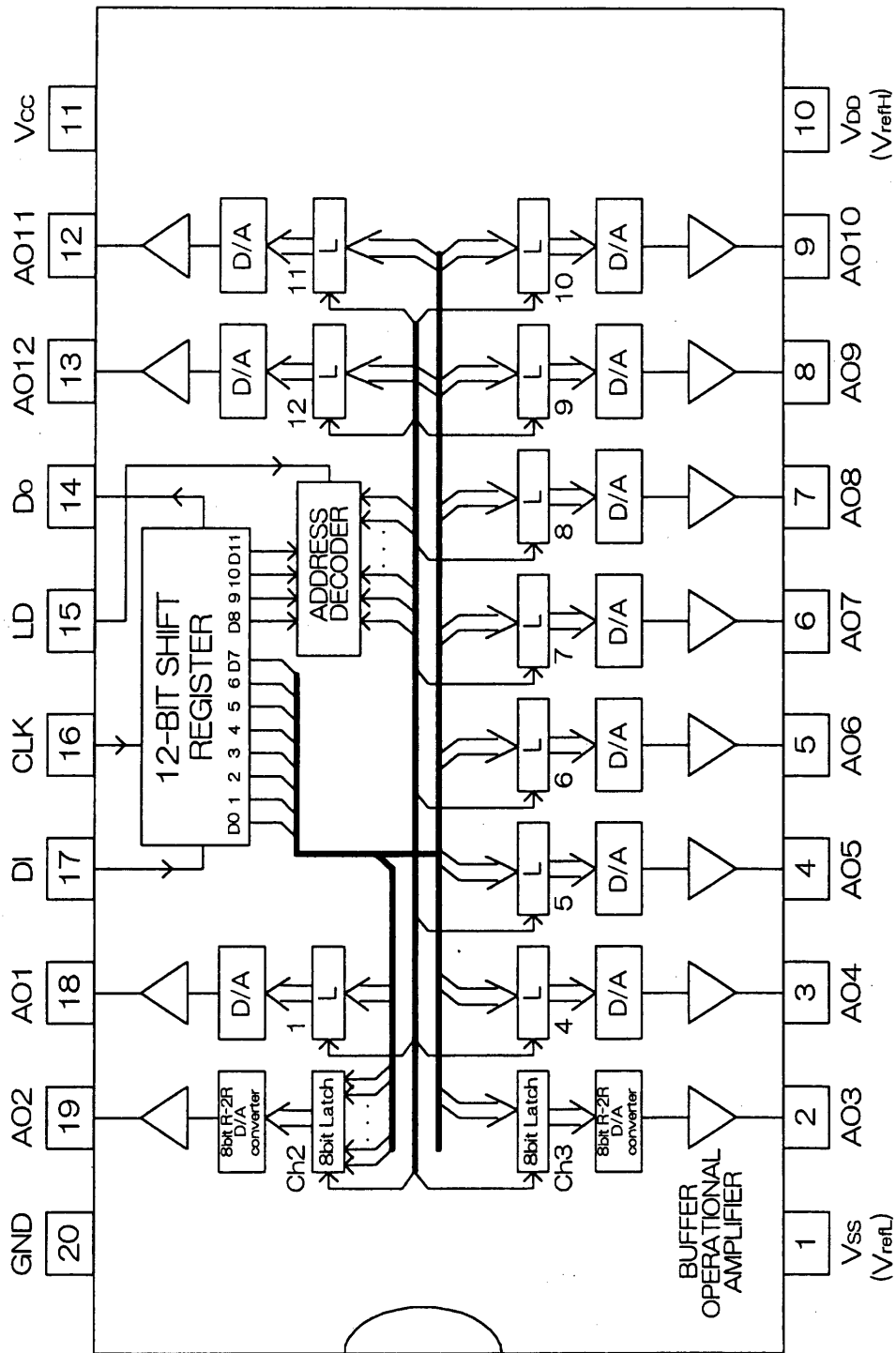


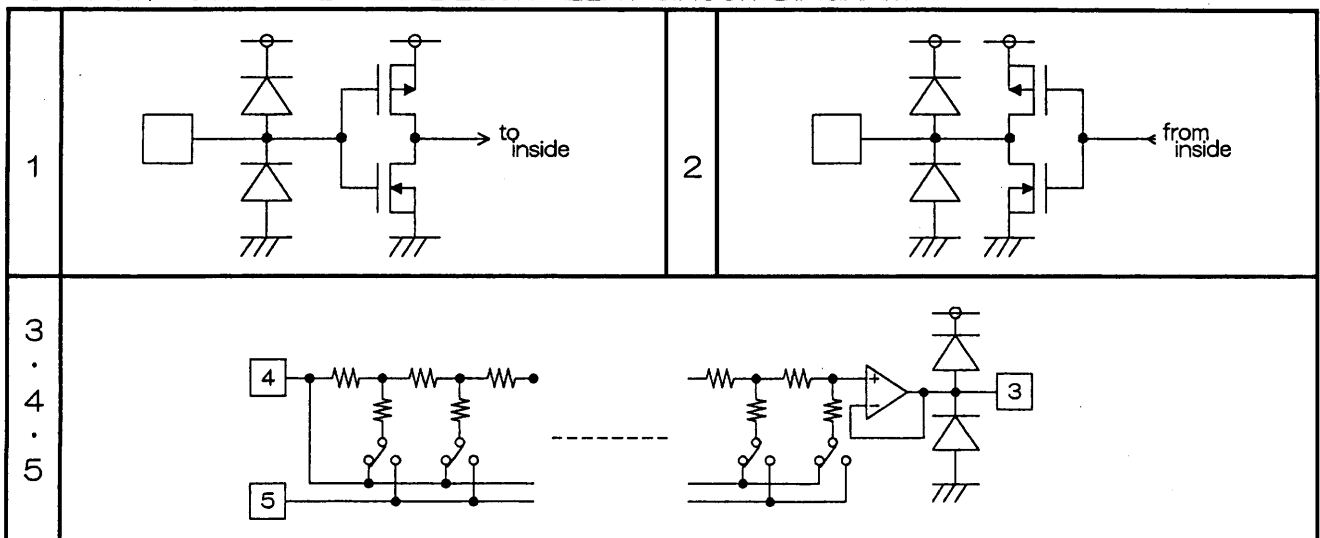
Figure 2 BLOCK DIAGRAM

Date 25 /May./2000	Specification
ROHM CO., LTD.	Specification No.
	TSZ02201-BU2500FV-1-2

O EXPLANATION OF TERMINALS

Pin No.	Symbol	Analog / Digital	I/O	Function	Equivalent Circuit
1	Vss	Analog	—	D/A converter lower reference voltage input terminal	5
2	Ao3	Analog	O	8bit D/A converter output terminal (CH3)	3
3	Ao4	Analog	O	8bit D/A converter output terminal (CH4)	3
4	Ao5	Analog	O	8bit D/A converter output terminal (CH5)	3
5	Ao6	Analog	O	8bit D/A converter output terminal (CH6)	3
6	Ao7	Analog	O	8bit D/A converter output terminal (CH7)	3
7	Ao8	Analog	O	8bit D/A converter output terminal (CH8)	3
8	Ao9	Analog	O	8bit D/A converter output terminal (CH9)	3
9	Ao10	Analog	O	8bit D/A converter output terminal (CH10)	3
10	VDD	Analog	—	D/A converter upper reference voltage input terminal	4
11	VCC	—	—	Power supply terminal	—
12	Ao11	Analog	O	8bit D/A converter output terminal (CH11)	3
13	Ao12	Analog	O	8bit D/A converter output terminal (CH12)	3
14	Do	Digital	O	Terminal to output MSB data of 12-bit shift register	2
15	LD	Digital	I	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D/A converter output register	1
16	CLK	Digital	I	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse	1
17	DI	Digital	I	Serial data input terminal to input 12-bit long serial data	1
18	Ao1	Analog	O	8bit D/A converter output terminal (CH1)	3
19	Ao2	Analog	O	8bit D/A converter output terminal (CH2)	3
20	GND	—	—	GND terminal	—

O INPUT/OUTPUT TERMINAL EQUIVALENT CIRCUIT DIAGRAM



Date 25 /May./2000

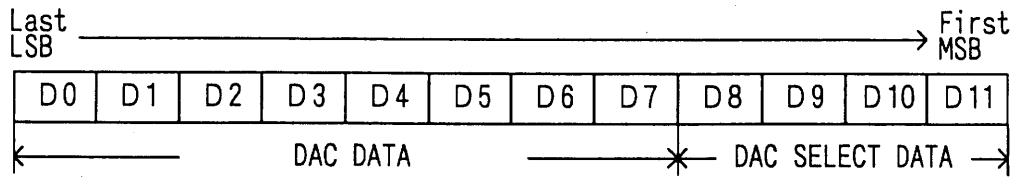
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ROHM CO., LTD.

Specification No.

TSZ02201-BU2500FV-1-2

○ DIGITAL DATA FORMAT

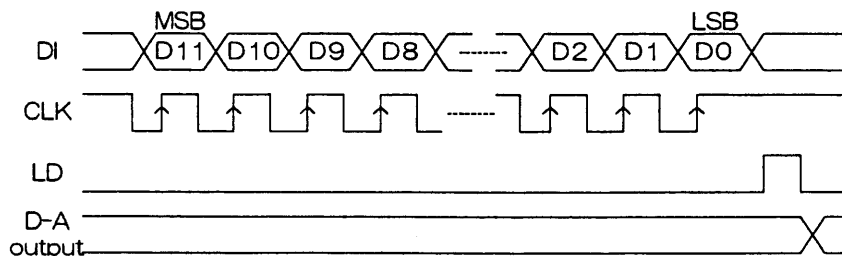


D0	D1	D2	D3	D4	D5	D6	D7	D/A output
0	0	0	0	0	0	0	0	$(V_{refH} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refH} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refH} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refH} - V_{refL}) / 256 \times 4 + V_{refL}$
0	1	1	1	1	1	1	1	$(V_{refH} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refH}

* $V_{refH} = V_{DD}$ $V_{refL} = V_{SS}$

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't Care
0	0	0	1	A01 selection
0	0	1	0	A02 selection
0	0	1	1	A03 selection
0	1	0	0	A04 selection
0	1	0	1	A05 selection
0	1	1	0	A06 selection
0	1	1	1	A07 selection
1	0	0	0	A08 selection
1	0	0	1	A09 selection
1	0	1	0	A010 selection
1	0	1	1	A011 selection
1	1	0	0	A012 selection
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

○ TIMING CHART (MODEL)



Date 25 /May./2000

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TSZ02201-BU2500FV-1-2

○ ELECTRICAL CHARACTERISTICS

«Digital part»

($V_{CC}=5V$, $V_{refH}=5V$, $V_{refL}=0V$, $T_a=25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		Min.	Typ.	Max.		
Circuit current	I_{CC}	—	0.5	1.5	mA	CLK=1MHz operation, $V_{CC}=5V$, $I_{AO}=0\mu A$
Input leak current	I_{ILK}	-5	—	5	μA	$V_{IN}=0\sim V_{CC}$
Input low voltage	V_{IL}	—	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Output low voltage	V_{OL}	0	—	0.4	V	$I_{OL}=2.5mA$
Output high voltage	V_{OH}	4.6	—	5	V	$I_{OH}=-2.5mA$

«Analog part»

($V_{CC}=5V$, $V_{refH}=5V$, $V_{refL}=0V$, $T_a=25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		Min.	Typ.	Max.		
Current dissipation	I_{refH}	—	0.9	1.8	mA	$V_{refU}=5V$, $V_{refL}=0V$ Data condition: Maximum Current
D/A converter upper reference voltage range	V_{refH}	3.5	—	5	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range
D/A converter lower reference voltage range	V_{refL}	0	—	1.5	V	
Buffer amplifier output driver voltage range	V_{AO}	0.1	—	4.9	V	$I_{AO}=\pm 100\mu A$
		0.2	—	4.8		$I_{AO}=\pm 500\mu A$
Buffer amplifier output voltage range	I_{AO}	-1	—	1	mA	Upper saturation voltage=0.3V Lower saturation voltage=0.2V
Accuracy	Differential nonlinearity error	SDL	-1.0	—	1.0	LSB $V_{refH}=4.79V$ $V_{refL}=0.95V$ $V_{CC}=5.5V$ (15mV/LSB) Without load ($I_{AO}=+0$)
	Nonlinearity error	SL	-1.5	—	1.5	
	Zero code error	SZERO	-2	—	2	
	Full scale error	SFULL	-2	—	2	
Output capacitive load	C_O	—	—	10	μF	
Buffer amplifier output impedance	R_O	—	5	15	Ω	

Date 25 /May./2000

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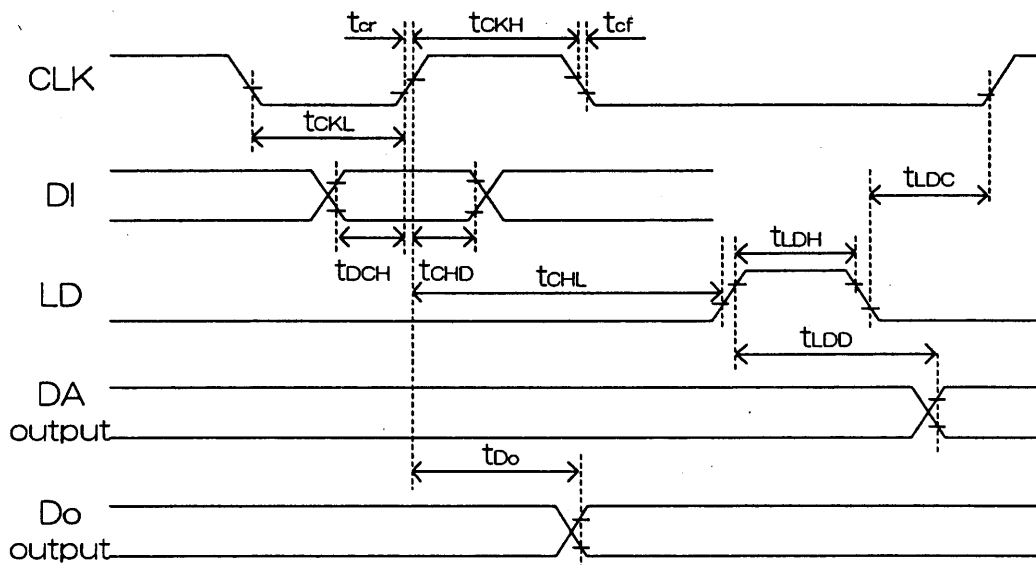
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 <<AC CHARACTERISTICS>>

(V_{CC}=5V, V_{refH}=5V, V_{refL}=0V, T_a=25°C, unless otherwise noted)

Parameter	Symbol	Limits			Unit	Test conditions
		Min	Typ	Max		
Clock "L" pulse width	t _{CKL}	150	—	—	n s	
Clock "H" pulse width	t _{CKH}	150	—	—		
Clock rise time	t _{cr}	—	—	150		
Clock fall time	t _{cf}	—	—	150		
Data set up time	t _{DCH}	20	—	—		
Data hold time	t _{CHD}	40	—	—		
LD set up time	t _{CHL}	150	—	—		
LD hold time	t _{LDC}	100	—	—		
LD "H" pulse duration	t _{LDH}	70	—	—		
Data output delay time	t _{DO}	70	—	350		
D/A output setting time	t _{LDD}	—	80	250	μ S	CL ≤ 1000pF V _{AO} : 0.5V ⇔ 4.5V The time until the becomes the final value of 1/2 LSB.



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Applied Circuit Diagram

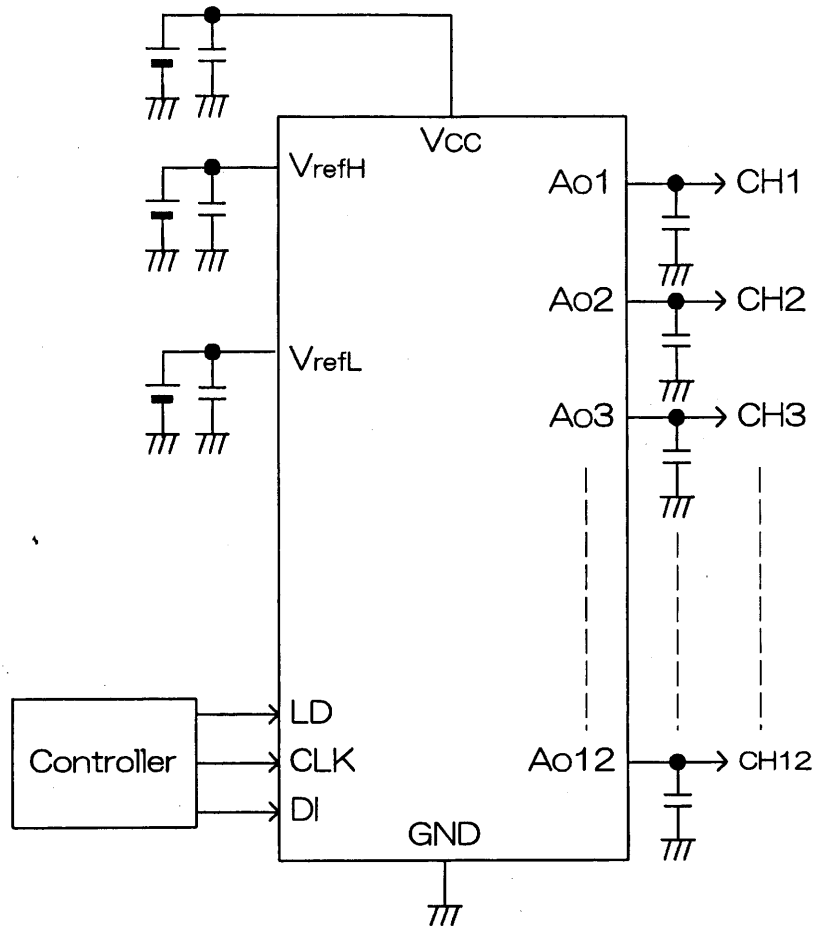


Figure 3 Applied Circuit Diagram

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