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NTE6810
Integrated Circuit
128 x 8–Bit Static Random Access Memory (SRAM)

Description:

The NTE6810 is a byte–orgainzed memory in a 24–Lead DIP type package designed for use in bus–organized systems. It is fabricated with N–channel silicon–gate technology. For ease of use, this device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the 6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

Features:

- Organized as 128 Bytes of 8–Bits
- Static Operation
- Bidirectional Three–State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5V Power Supply
- TTL Compatible
- Maximum Access Time: 450ns

Absolute Maximum Ratings:

Supply Voltage, V_{CC} . . . . . –0.3 to +7V
Input Voltage, V_{in} . . . . . –0.3 to +7V
Operating Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Thermal Resistance, Junction to Ambient, $R_{\Theta JA}$ . . . . . +120°C/W

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either V_{SS} or V_{CC}).

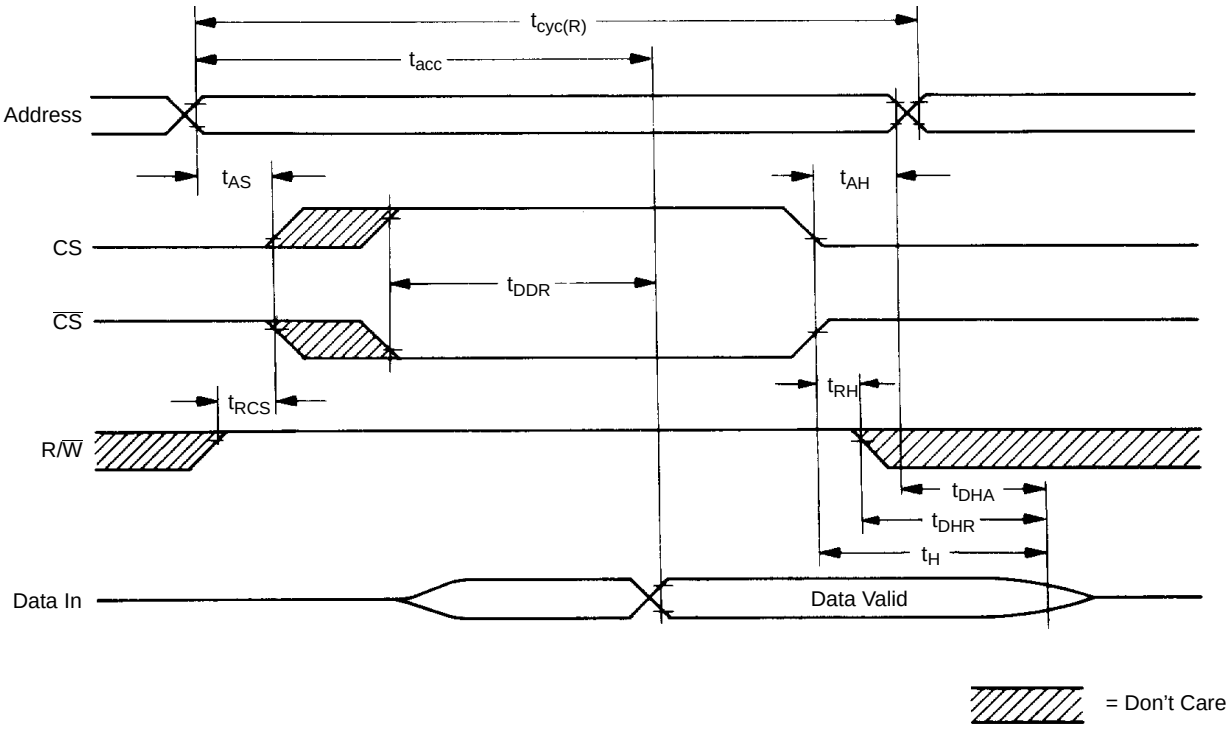
DC Electrical Characteristics: (V_{CC} = 5V ±5%, V_{SS} = 0, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input High Voltage	V_{IH}		V_{SS} +2.0	V_{CC}	V
Input Low Voltage	V_{IL}		V_{SS} –0.3	V_{SS} +0.8	V
Input Current (A_n, R/$\overline{W}$, $\overline{CS}_n$)	I_{in}	V_{in} = 0 to 5.25V	–	2.5	µA
Output High Voltage	V_{OH}	I_{OH} = –205µA	2.4	–	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	–	0.4	V
Output Leakage Current (Three–State)	I_{TSI}	CS = 0.8V or $\overline{CS}$ = 2V, V_{out} = 0.4V to 2.4V	–	10	µA
Supply Current	I_{CC}	V_{CC} = 5.25V, All other pins grounded	–	80	mA
Input Capacitance (A_n, R/$\overline{W}$, CS_n, $\overline{CS}_n$)	C_{in}	V_{in} = 0, T_A = +25°C, f = 1MHz	–	7.5	pF
Output Capacitance (D_n)	C_{out}	V_{out} = 0, T_A = +25°C, f = 1MHz, CSO = 0	–	12.5	pF

AC Operating Conditions and Characteristics:

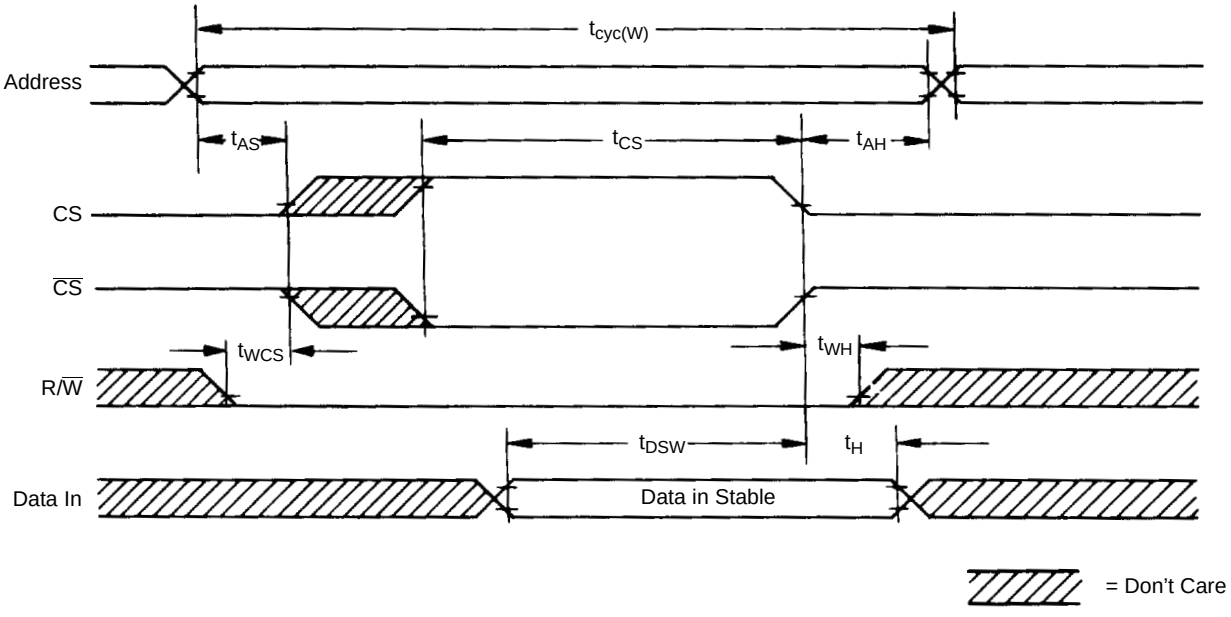
Parameter	Symbol	Min	Max	Unit
Read Cycle (V_{CC} = 5V ±5%, V_{SS} = 0, T_A = 0° to +70° unless otherwise specified)				
Read Cycle Time	$t_{cyc(R)}$	450	–	ns
Access Time	t_{acc}	–	450	ns
Address Setup Time	t_{AS}	20	–	ns
Address Hold Time	t_{AH}	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	ns
Read to Select Delay Time	t_{RCS}	0	–	ns
Data Hold from Address	t_{DHA}	10	–	ns
Output Hold Time	t_H	10	–	ns
Data Hold from Read	t_{DHR}	10	80	ns
Read Hold from Chip Select	t_{RH}	0	–	ns
Write Cycle (V_{CC} = 5V ±5%, V_{SS} = 0, T_A = 0° to +70° unless otherwise specified)				
Write Cycle Time	$t_{cyc(W)}$	450	–	ns
Address Setup Time	t_{AS}	20	–	ns
Address Hold Time	t_{AH}	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	ns
Input Hold Time	t_H	10	–	ns
Write Hold Time from Chip Select	t_{WH}	0	–	ns

Read Cycle Timing



Note 1. Voltage levels shown are $V_L \leq 0.4V$, $V_H \geq 2.4V$, unless otherwise specified.
Note 2. Measurement pointas shown are 0.8V and 2.0V, unless otherwise specified.
Note 3. CS and $\overline{CS}$ have same timing.

Write Cycle Timing



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Pin Connection Diagram