

FEATURES

- Quad integrated I/Q demodulator**
- 16 phase select on each output (22.5° per step)**
- Quadrature demodulation accuracy**
 - Phase accuracy: $\pm 1^\circ$
 - Amplitude balance: ± 0.25 dB
- Bandwidth**
 - 4LO: LF to 200 MHz
 - RF: LF to 50 MHz
- Baseband: determined by external filtering**
- Output dynamic range: 160 dB/Hz**
- LO drive: >0 dBm (50 Ω), single-ended sine wave**
- Supply: ± 5 V**
- Power consumption: 73 mW/channel (290 mW total)**
- Power-down via SPI (each channel and complete chip)**

APPLICATIONS

- Medical imaging (CW ultrasound beamforming)**
- Phased array systems**
 - Radar
 - Adaptive antennas
- Communication receivers**

GENERAL DESCRIPTION

The AD8339¹ is a quad I/Q demodulator configured to be driven by a low noise preamplifier with differential outputs. It is optimized for the LNA in the AD8332/AD8334/AD8335 family of VGAs. The part consists of four identical I/Q demodulators with a 4 \times local oscillator (LO) input that divides this signal and generates the necessary 0° and 90° phases of the internal LO that drive the mixers. The four I/Q demodulators can be used independently of each other (assuming that a common LO is acceptable) because each has a separate RF input.

Continuous wave (CW) analog beamforming (ABF) and I/Q demodulation are combined in a single 40-lead ultracompact chip scale device, making the AD8339 particularly applicable in high density ultrasound scanners. In an ABF system, time domain coherency is achieved following the appropriate phase alignment and summation of multiple receiver channels. A reset pin synchronizes multiple ICs to start each LO divider in the same quadrant. Sixteen programmable 22.5° phase increments are available for each channel. For example, if Channel 1 is used as a reference and Channel 2 has an I/Q phase lead of 45°, then the user can phase align Channel 2 with Channel 1 by choosing the correct code.

¹ Patent pending.

Rev. 0

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FUNCTIONAL BLOCK DIAGRAM

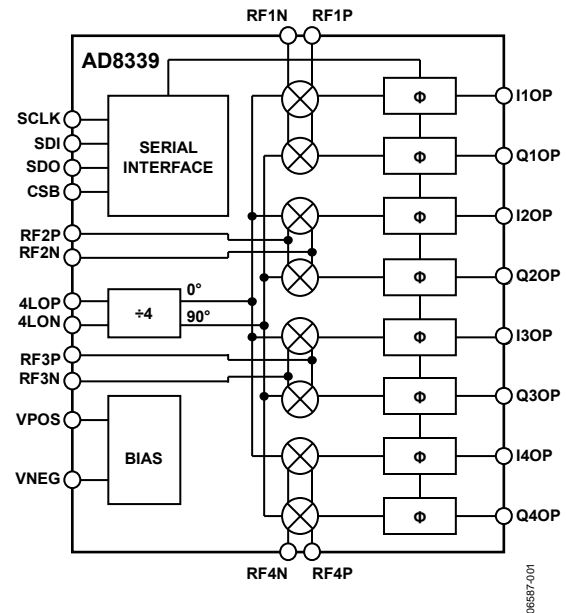


Figure 1.

The mixer outputs are in current form for convenient summation. The independent I and Q mixer output currents are summed and converted to a voltage by a low noise, high dynamic range, current-to-voltage (I-V) transimpedance amplifier, such as the AD8021 or the AD829. Following the current summation, the combined signal is applied to a high resolution analog-to-digital converter (ADC), such as the AD7665 (16-bit, 570 kSPS).

An SPI-compatible serial interface port is provided to easily program the phase of each channel; the interface allows daisy chaining by shifting the data through each chip from SDI to SDO. The SPI also allows for power-down of each individual channel and the complete chip. During power-down, the serial interface remains active so that the device can be programmed again.

The dynamic range is typically 160 dB/Hz at the I and Q outputs. The AD8339 is available in a 6 mm \times 6 mm, 40-lead LFCSP and is specified over the industrial temperature range of -40°C to $+85^\circ\text{C}$.

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REVISION HISTORY

8/07—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$, $4f_{LO} = 20\text{ MHz}$, $f_{RF} = 5.01\text{ MHz}$, $f_{BB} = 10\text{ kHz}$, $P_{LO} \geq 0\text{ dBm}$, per channel performance, dBm (50 Ω), unless otherwise noted. Single-channel AD8021 LPF values: $R_{FILT} = 787\ \Omega$ and $C_{FILT} = 2.2\text{ nF}$ (see Figure 52).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Local Oscillator Frequency Range	4× internal LO at Pin 4LOP and Pin 4LON, square wave drive via LVDS (see Figure 62)	0.01		200	MHz
RF Frequency Range	Mixing	DC		50	MHz
Baseband Bandwidth	Limited by external filtering	DC		50	MHz
LO Input Level			0	13	dBm
V_{SUPPLY} (V_S)		± 4.5	± 5	± 5.5	V
Temperature Range		-40		+85	$^\circ\text{C}$
DEMODULATOR PERFORMANCE					
Input Impedance	RF, differential LO, differential		25 10 100 4		k Ω pF k Ω pF
Transconductance	Demodulated I_{OUT}/V_{IN} ; each Ix or Qx output after low-pass filtering measured from RF inputs, all phases		1.15		mS
Dynamic Range	IP1 dB – input referred noise (dBm)		160		dB (1 Hz BW)
Maximum Input Swing	Differential; inputs biased at 2.5 V; Pin RFxP, Pin RFxN		2.8		V p-p
Peak Output Current (No Filtering)	0° phase shift 45° phase shift		± 2.4 ± 3.1		mA mA
Input P1dB	Ref = 50 Ω Ref = 1 V rms		14.8 1.85		dBm dBV
Third-Order Intermodulation (IM3)	$f_{RF1} = 5.010\text{ MHz}$, $f_{RF2} = 5.015\text{ MHz}$, $f_{LO} = 5.023\text{ MHz}$				
Equal Input Levels	Baseband tones: 0 dBm @ 8 kHz and 13 kHz		-60		dBc
Unequal Input Levels	Baseband tones: -1 dBm @ 8 kHz and -31 dBm @ 13 kHz		-66		dBc
Third-Order Input Intercept (IIP3)	$f_{RF1} = 5.010\text{ MHz}$, $f_{RF2} = 5.015\text{ MHz}$, $f_{LO} = 5.023\text{ MHz}$		31		dBm
LO Leakage	Measured at RF inputs, worst phase, measured into 50 Ω Measured at baseband outputs, worst phase, AD8021 disabled, measured into 50 Ω		-118 -68		dBm dBm
Conversion Gain	All codes, see Figure 41		-1.3		dB
Input Referred Noise	Output noise/conversion gain (see Figure 46)		11.8		nV/ $\sqrt{\text{Hz}}$
Output Current Noise	Output noise/ R_{FILT}		12.9		pA/ $\sqrt{\text{Hz}}$
Noise Figure	With AD8334 LNA $R_S = 50\ \Omega$, $R_{FB} = \infty$ $R_S = 50\ \Omega$, $R_{FB} = 1.1\text{ k}\Omega$ $R_S = 50\ \Omega$, $R_{FB} = 274\ \Omega$		8.4 9.1 11.5		dB dB dB
Bias Current	Pin 4LOP and Pin 4LON Pin RFxP and Pin RFxN		-3 -45		μA μA
LO Common-Mode Range	Pin 4LOP and Pin 4LON (each pin)	0.2		3.8	V
RF Common-Mode Voltage	For maximum differential swing; Pin RFxP and Pin RFxN (dc-coupled to AD8334 LNA output)		2.5		V
Output Compliance Range	Pin IxOP and Pin QxOP	-1.5		+0.7	V
PHASE ROTATION PERFORMANCE					
Phase Increment	One channel is reference, others are stepped 16 phase steps per channel		22.5		Degrees
Quadrature Phase Error	Ix to Qx; all phases, 1 σ	-2	± 1	+2	Degrees
I/Q Amplitude Imbalance	Ix to Qx; all phases, 1 σ		± 0.05		dB
Channel-to-Channel Matching	Phase match I-to-I and Q-to-Q; $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ Amplitude match I-to-I and Q-to-Q; $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		± 1 ± 0.1		Degrees dB

AD8339

Parameter	Conditions	Min	Typ	Max	Unit
LOGIC INTERFACES					
Logic Level High	Pin SDI, Pin CSB, Pin SCLK, Pin RSET	1.5			V
Logic Level Low				0.9	V
Logic Level High	Pin RSTS	1.8			V
Logic Level Low				1.2	V
Bias Current	Logic high (pulled to +5 V)		0.5		μA
	Logic low (pulled to GND)		0		μA
Input Resistance			4		MΩ
LO Divider RSET Setup Time	RSET rising or falling edge to 4LOP to 4LON (differential) rising edge	5			ns
LO Divider RSET High Pulse Width		20			ns
LO Divider RSET Response Time			200		ns
Phase Response Time	Measured from CSB going high		5		μs
Enable Response Time	Measured from CSB going high (with 0.1 μF capacitor on Pin LODC); no channel enabled		12	15	μs
	At least one channel enabled		500		ns
Output	Pin SDO loaded with 5 pF and next SDI input				
Logic Level High		1.7	1.9		V
Logic Level Low			0.2	0.5	V
SPI TIMING CHARACTERISTICS					
SCLK Frequency	Pin SDI, Pin SDO, Pin CSB, Pin SCLK, Pin RSTS f_{CLK}			10	MHz
CSB Fall to SCLK Setup Time	t_1	0			ns
SCLK High Pulse Width	t_2	10			ns
SCLK Low Pulse Width	t_3	10			ns
Data Access Time (SDO) After SCLK Rising Edge	t_4			100	ns
Data Setup Time Before SCLK Rising Edge	t_5	2			ns
Data Hold Time After SCLK Rising Edge	t_6	2			ns
SCLK Rise to CSB Rise Hold Time	t_7	15			ns
CSB Rise to SCLK Rise Hold Time	t_8	0			ns
POWER SUPPLY					
Supply Voltage	Pin VPOS, Pin VNEG	±4.5	±5	±5.5	V
Current	VPOS, all phase bits = 0		35		mA
	VNEG, all phase bits = 0		-18		mA
Over Temperature -40°C < T _A < +85°C	VPOS, all phase bits = 0	33		36	mA
	VNEG, all phase bits = 0		-19	-17	mA
Quiescent Power	Per channel, all phase bits = 0		66		mW
	Per channel maximum (depends on phase bits)		88		mW
Disable Current	All channels disabled; SPI stays on		2.75		mA
PSRR	VPOS to Ix/Qx outputs, @ 10 kHz		-85		dB
	VNEG to Ix/Qx outputs, @ 10 kHz		-85		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltages	
Supply Voltage (V_S)	± 6 V
RF Inputs	+6 V to GND
4LO Inputs	+6 V to GND
Outputs (IxOP, QxOP)	+0.7 V to -6 V
Digital Inputs	+6 V to GND
SDO Output	+6 V to GND
LODC Pin	VPOS – 1.5 V to +6 V
Thermal Data (4-Layer JEDEC Board, No Air Flow, Exposed Pad Soldered to PC Board)	
θ_{JA}	32.2°C/W
θ_{JB}	17.8°C/W
θ_{JC}	2.7°C/W
ψ_{JT}	0.3°C/W
ψ_{JB}	16.7°C/W
Maximum Junction Temperature	150°C
Maximum Power Dissipation (Exposed Pad Soldered to PC Board)	2 W
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

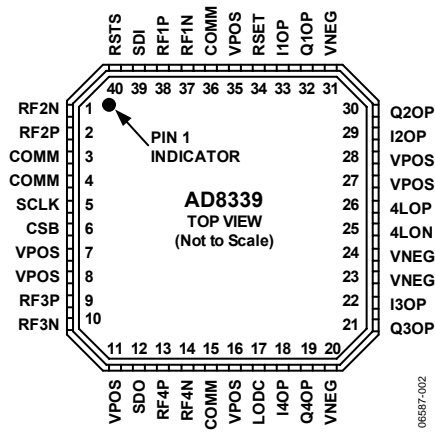


Figure 2. 40-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10, 13, 14, 37, 38	RF1P to RF4P, RF1N to RF4N	RF Inputs. Require external 2.5 V bias for optimum symmetrical input differential swing if ± 5 V supplies are used.
3, 4, 15, 36	COMM	Ground.
5	SCLK	Serial Interface—Clock.
6	CSB	Serial Interface—Chip Select Bar. Active low.
7, 8, 11, 16, 27, 28, 35	VPOS	Positive Supply. These pins should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μ F and 1 nF capacitor between the VPOS pins and ground. Because the VPOS pins are internally connected, one set of supply decoupling components on each side of the chip should be sufficient.
12	SDO	Serial Interface—Data Output. Normally connected to SDI of next chip or left open.
17	LODC	Decoupling Pin for LO. A 0.1 μ F capacitor should be connected between this pin and ground. Value of capacitor influences chip enable/disable times.
18, 19, 21, 22, 29, 30, 32, 33	I1OP to I4OP, Q1OP to Q4OP	I/Q Outputs. These outputs provide a bidirectional current that can be converted back to a voltage via a transimpedance amplifier. Multiple outputs can be summed together by simply connecting them (wire-OR). The bias voltage should be set to 0 V or less by the transimpedance amplifier (see Figure 52).
20, 23, 24, 31	VNEG	Negative Supply. These pins should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μ F and 1 nF capacitor between the pin and ground. Because the VNEG pins are internally connected, one set of supply decoupling components should be sufficient.
25, 26	4LOP, 4LON	LO Inputs. No internal bias; optimally biased by an LVDS driver. For best performance, these inputs should be driven differentially. If driven by single-ended sine wave at 4LOP or 4LON, the signal level should be > 0 dBm (50 Ω) with external bias resistors.
34	RSET	LO Interface—Reset. Logic threshold is at ~ 1.3 V and therefore can be driven by > 1.8 V CMOS logic.
39	SDI	Serial Interface—Data Input. Logic threshold is at ~ 1.3 V and therefore can be driven by > 1.8 V CMOS logic.
40	RSTS	Reset for SPI Interface. Logic threshold is at ~ 1.5 V with ± 0.3 V hysteresis and should be driven by > 3.3 V CMOS logic. For quick testing without the need to program the SPI, the voltage on the RSTS pin should be pulled to -1.4 V; this enables all four channels in the phase (I = 1, Q = 0) state.

EQUIVALENT INPUT CIRCUITS

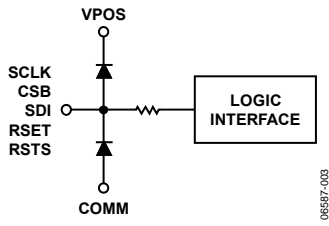


Figure 3. Logic Inputs

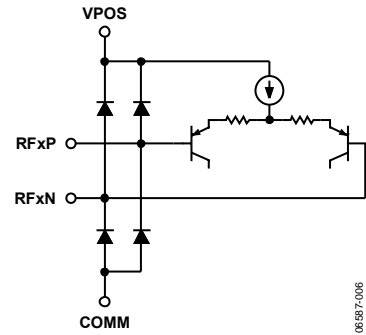


Figure 6. RF Inputs

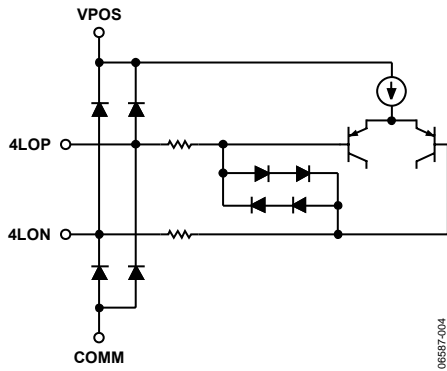


Figure 4. Local Oscillator Inputs

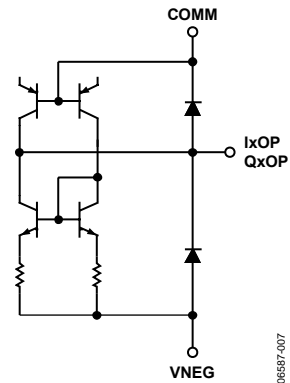


Figure 7. Output Drivers

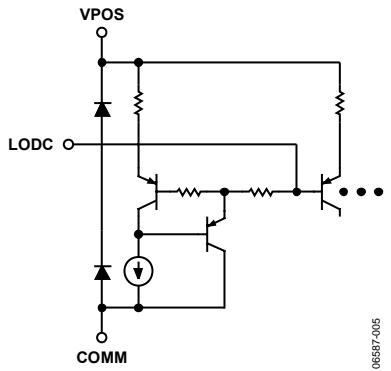


Figure 5. LO Decoupling Pin

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$, $4f_{LO} = 20\text{ MHz}$, $f_{LO} = 5\text{ MHz}$, $f_{RF} = 5.01\text{ MHz}$, $f_{BB} = 10\text{ kHz}$, $4f_{LO}$ – LVDS drive; per channel performance shown is typical of all channels, differential voltages, dBm (50 Ω), phase select code = 0000, unless otherwise noted (see default test circuit).

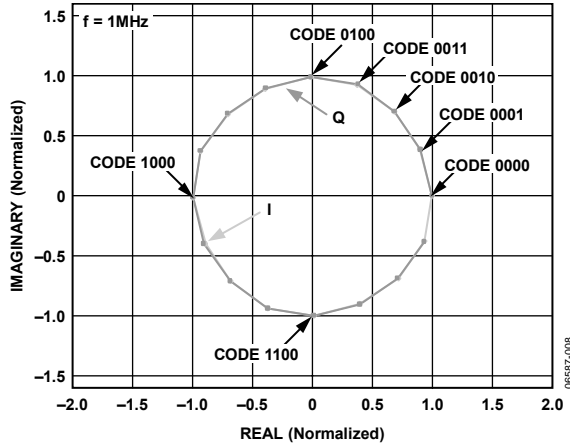


Figure 8. Normalized Vector Plot of Phase, CH2, CH3, and CH4 vs. CH1, CH1 Is Fixed at 0°, CH2, CH3, and CH4 Stepped 22.5°/Step, All Codes Displayed

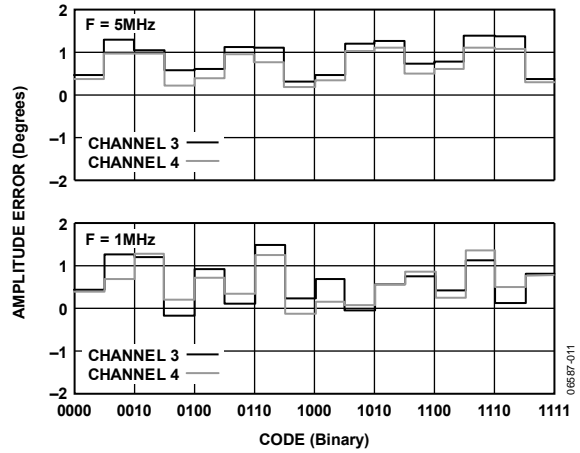


Figure 11. Representative Phase Error vs. Binary Phase-Select Code at 1 MHz and 5 MHz, CH3 and CH4 Are Displayed With Respect to CH1

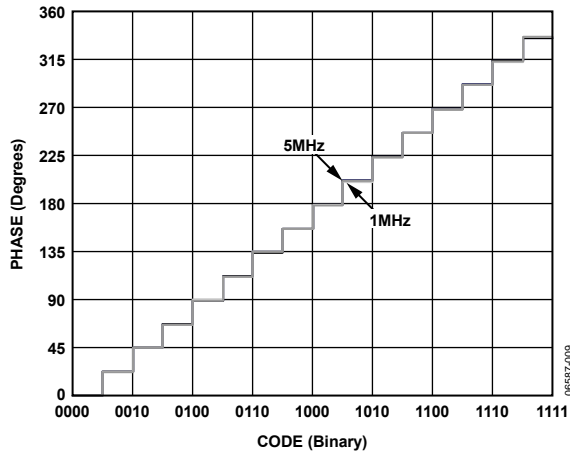


Figure 9. Representative Phase Delay vs. Binary Phase-Select Code at 1 MHz and 5 MHz, CH3 and CH4 Are Displayed With Respect to CH1

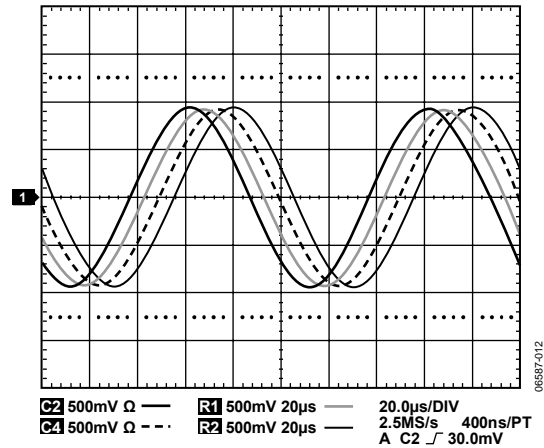


Figure 12. Representative Phase Delays of the I or Q Outputs, CH2 Is Displayed With Respect to CH1, for Delays of 22.5°, 45°, 67.5°, and 90°

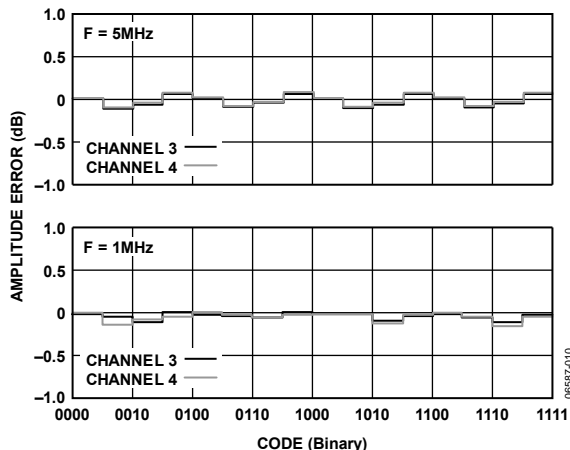


Figure 10. Representative Amplitude Error vs. Binary Phase-Select Code at 1 MHz and 5 MHz, CH3 and CH4 Are Displayed With Respect to CH1

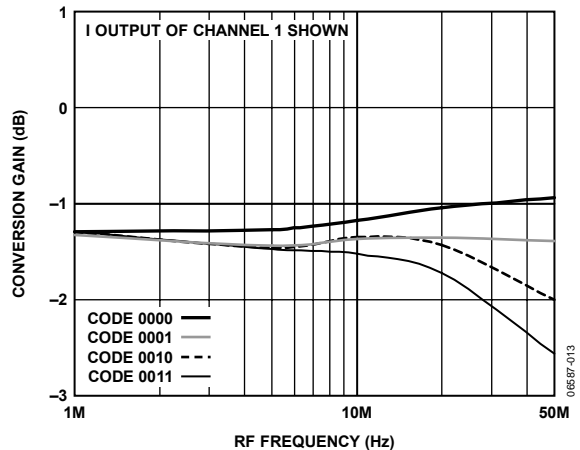


Figure 13. Conversion Gain vs. RF Frequency, First Quadrant, Baseband Frequency = 10 kHz

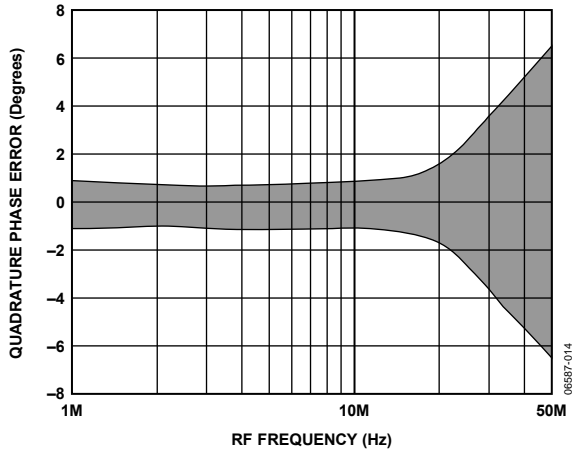


Figure 14. Representative Range of Quadrature Phase Error vs. RF Frequency for All Channels and Codes

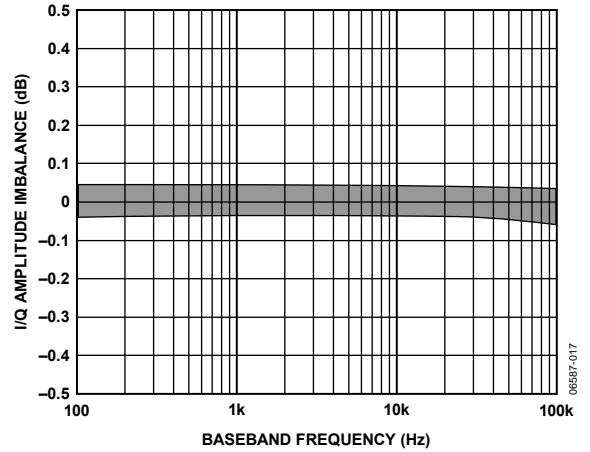


Figure 17. Representative Range of I/Q Amplitude Imbalance vs. Baseband Frequency for All Channels and Codes (See Figure 43)

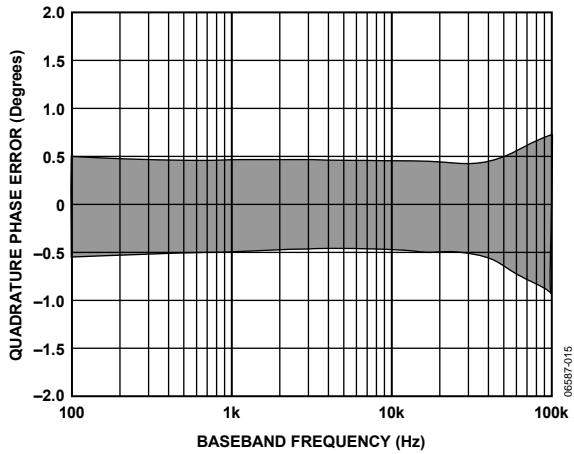


Figure 15. Representative Range of Quadrature Phase Error vs. Baseband Frequency for All Channels and Codes (See Figure 43)

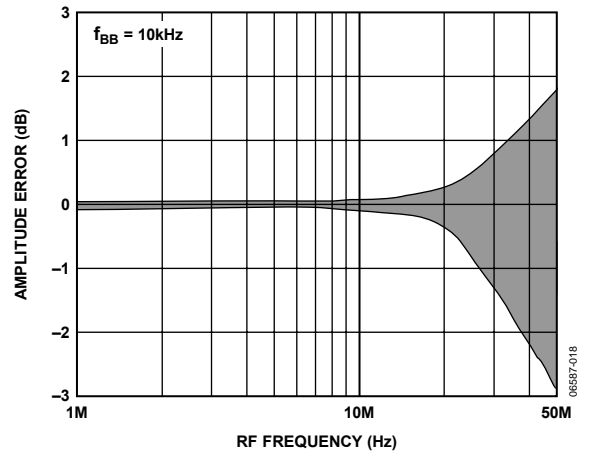


Figure 18. Typical Channel-to-Channel Amplitude Match vs. RF Frequency, First Quadrant, Over the Range of Operating Temperatures

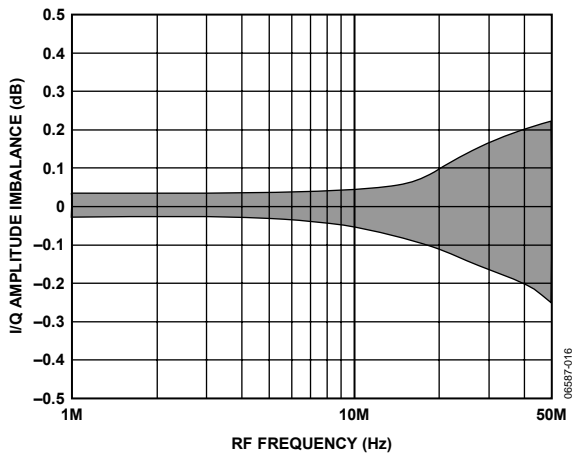


Figure 16. Representative Range of I/Q Amplitude Imbalance vs. RF Frequency for All Channels and Codes

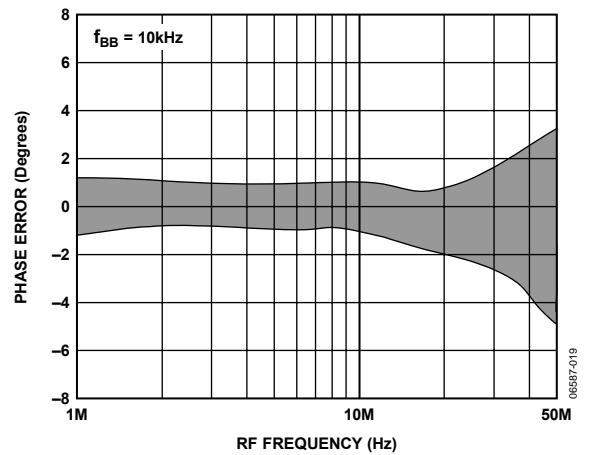


Figure 19. Typical Channel-to-Channel Phase Error vs. RF Frequency, First Quadrant, Over the Range of Operating Temperatures

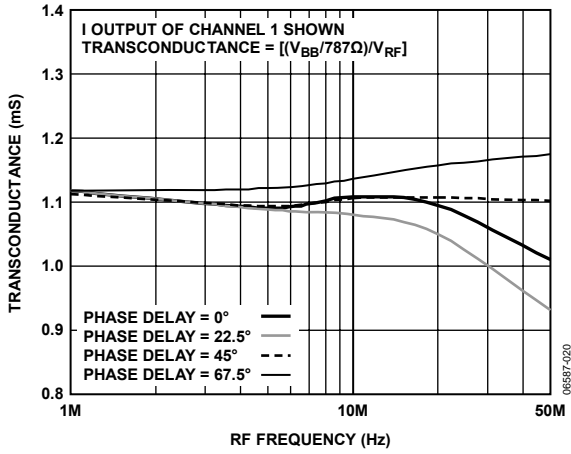


Figure 20. Transconductance vs. RF Frequency for First Quadrant Phase Delays

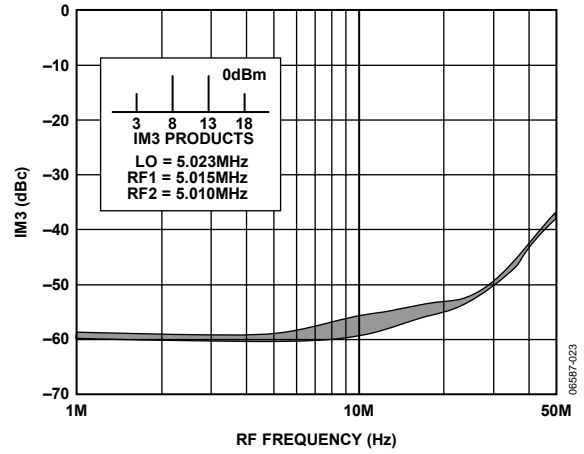


Figure 23. Representative Range of IM3 vs. RF Frequency, First Quadrant (See Figure 48)

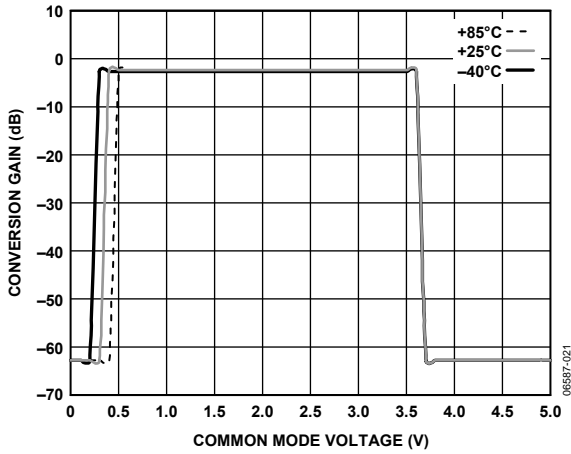


Figure 21. LO Common-Mode Range at Three Temperatures

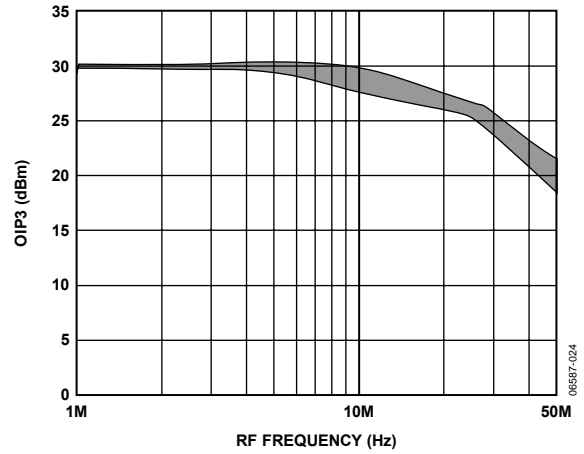


Figure 24. Representative Range of OIP3 vs. RF Frequency, First Quadrant (See Figure 48)

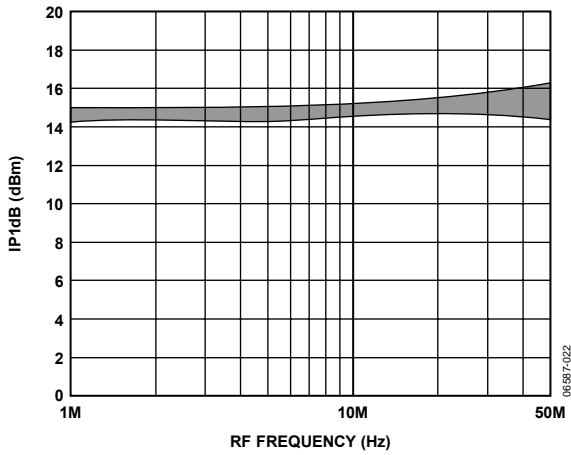


Figure 22. Representative Range of IP1dB vs. RF Frequency, Baseband Frequency = 10 kHz, First Quadrant (See Figure 42)

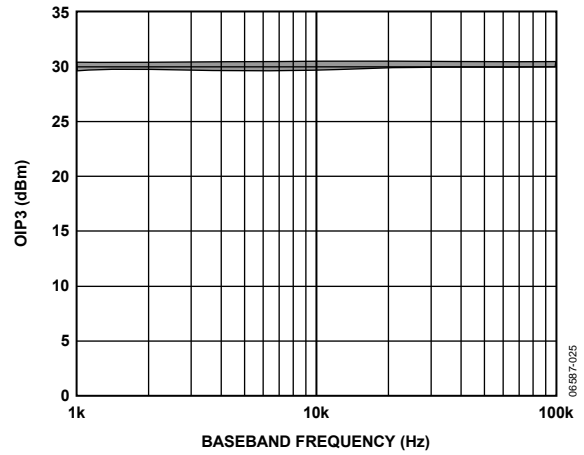


Figure 25. Representative Range of OIP3 vs. Baseband Frequency (See Figure 47)

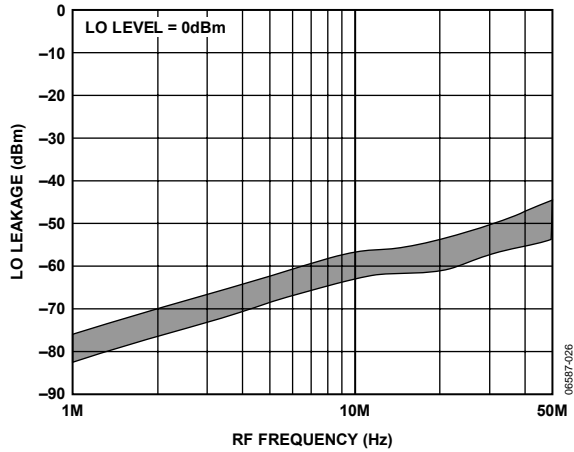


Figure 26. Representative Range of LO Leakage vs. RF Frequency at I and Q Outputs

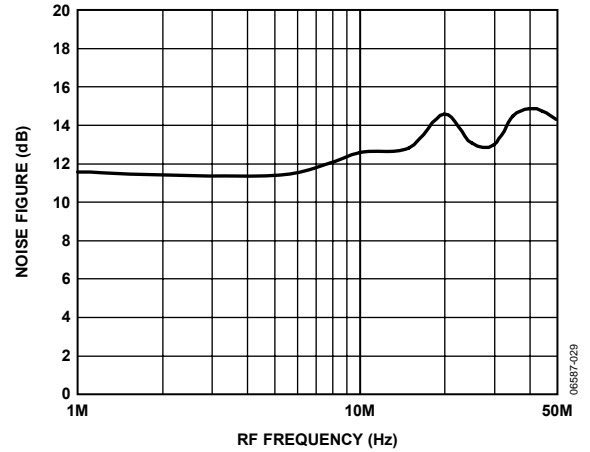


Figure 29. Noise Figure vs. RF Frequency (When Driven by AD8334 LNA)

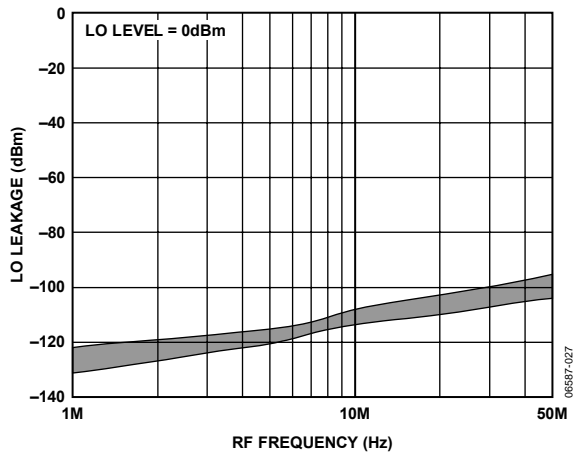


Figure 27. Representative Range of LO Leakage vs. RF Frequency at RF Inputs

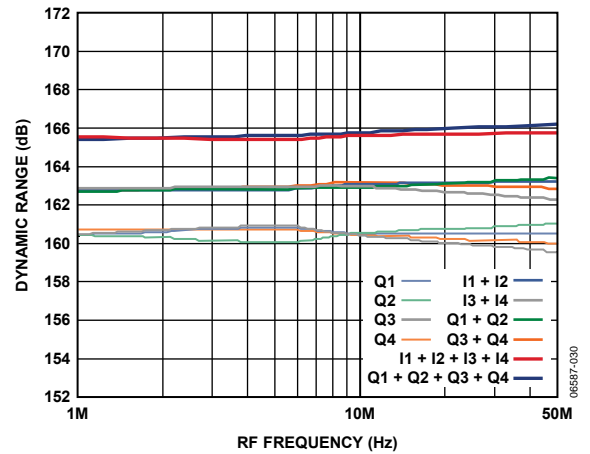


Figure 30. Dynamic Range vs. RF Frequency, IP1dB Minus Noise Level

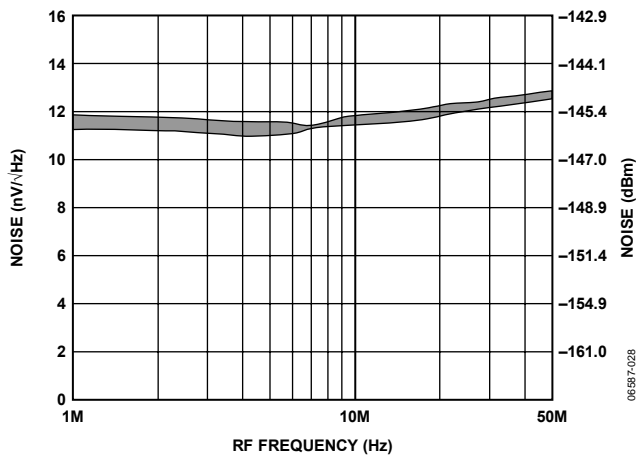


Figure 28. Representative Range of Input Referred Noise vs. RF Frequency

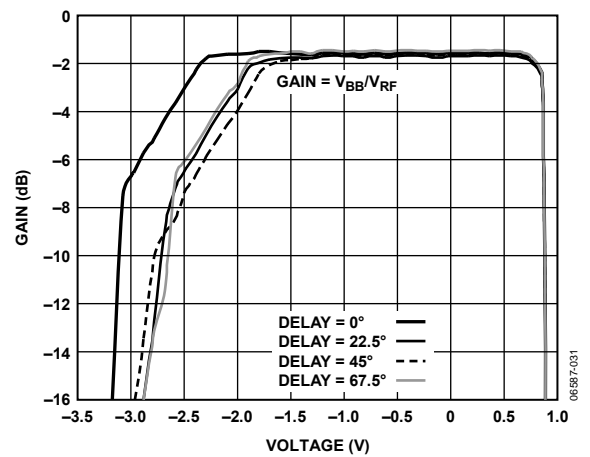


Figure 31. Output Compliance Range for Four Values of Phase Delay (See Figure 49)

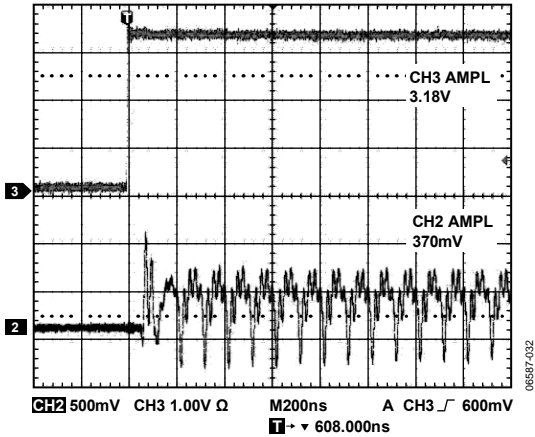


Figure 32. Enable Response vs. CSB (Filter Disabled to Show Response) with a Previously Enabled Channel (See Figure 43)

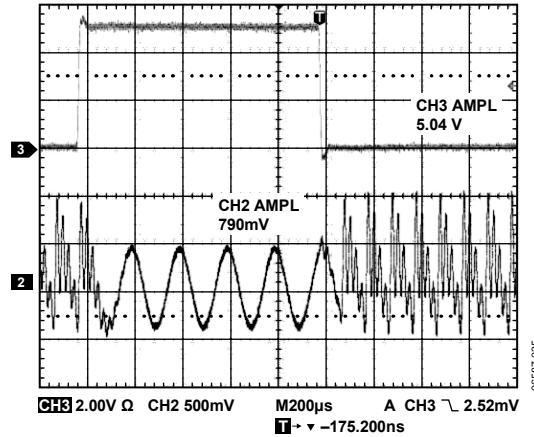


Figure 35. LO Reset Response (see Figure 44)

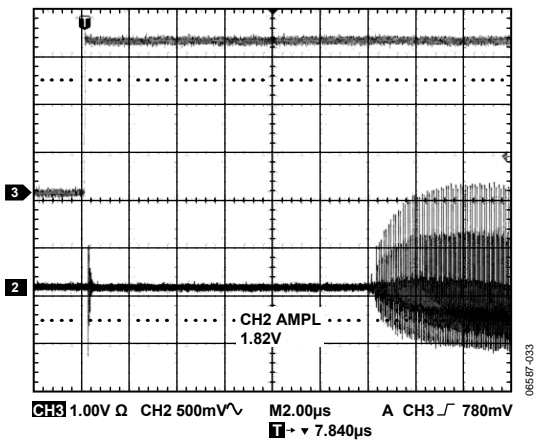


Figure 33. Enable Response vs. CSB (Filter Disabled to Show Response) with No Channels Previously Enabled (See Figure 43)

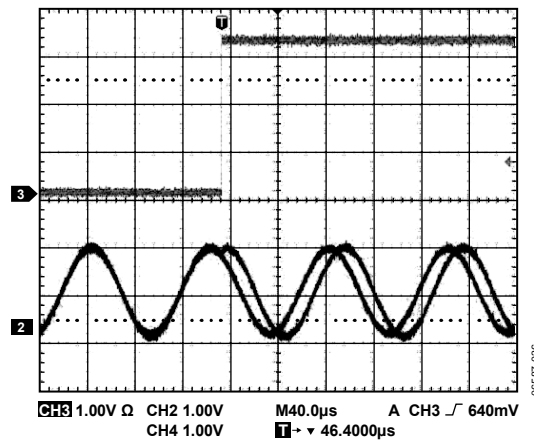


Figure 36. Phase Switching Response at 45° (Top: CSB)

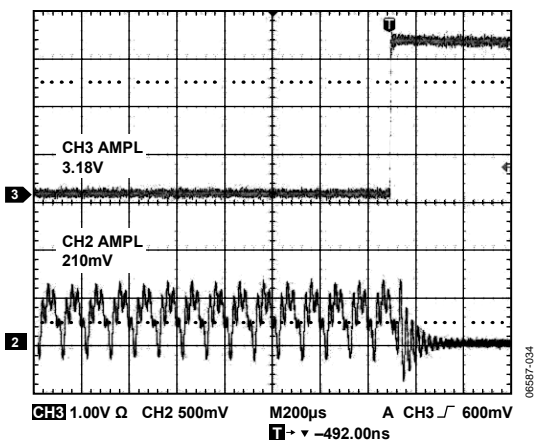


Figure 34. Disable Response vs. CSB (Top: CSB) (See Figure 43)

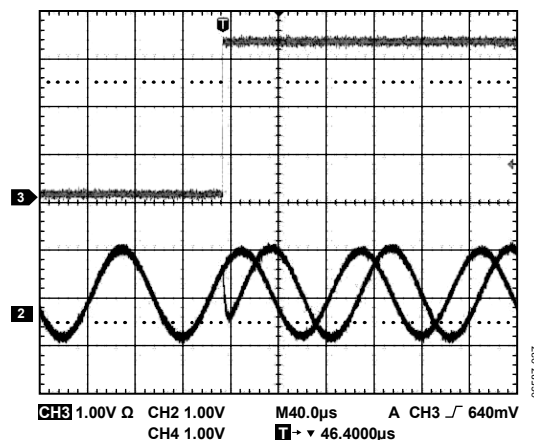


Figure 37. Phase Switching Response at 90° (Top: CSB)

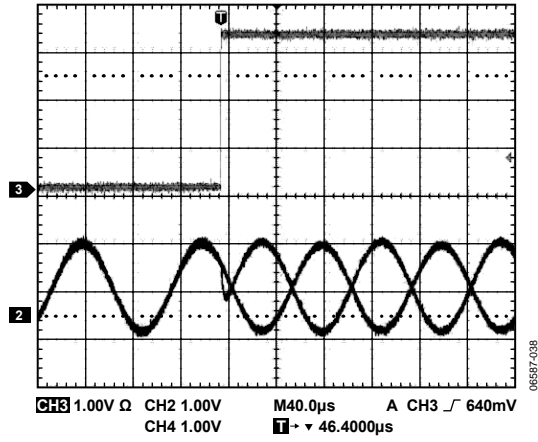


Figure 38. Phase Switching Response at 180° (Top: CSB)

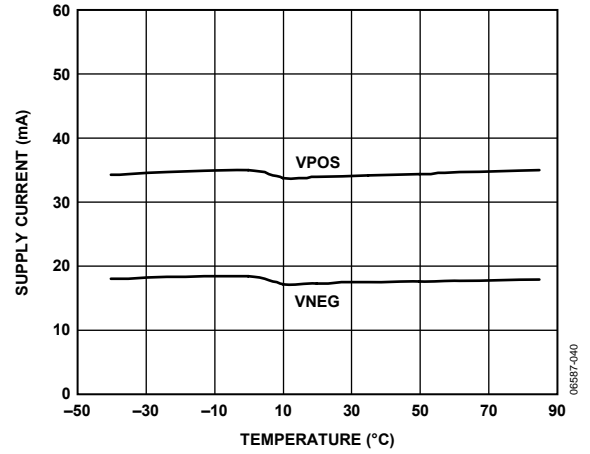


Figure 40. Supply Current vs. Temperature

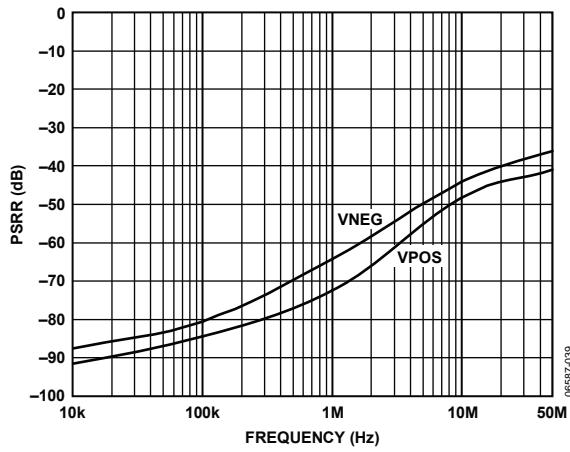


Figure 39. PSRR vs. Frequency (see Figure 50)

TEST CIRCUITS

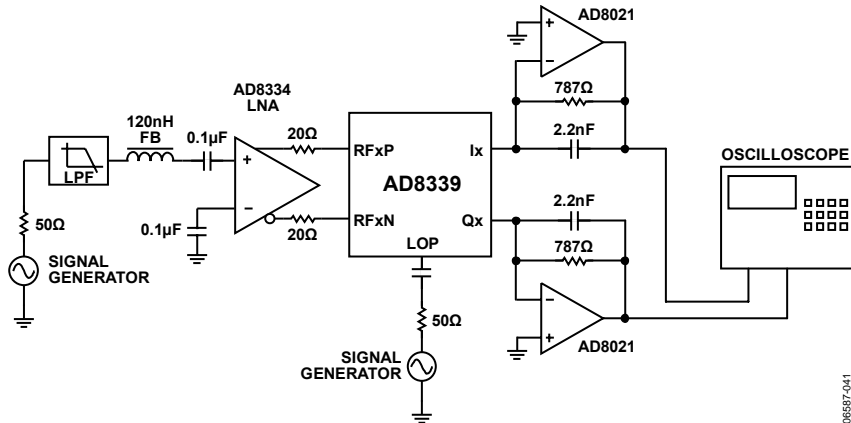


Figure 41. Default Test Circuit

06587-041

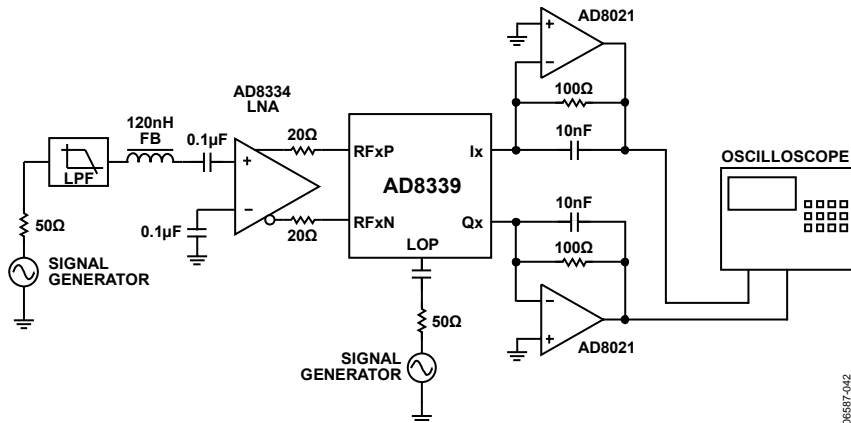


Figure 42. P1dB Test Circuit

06587-042

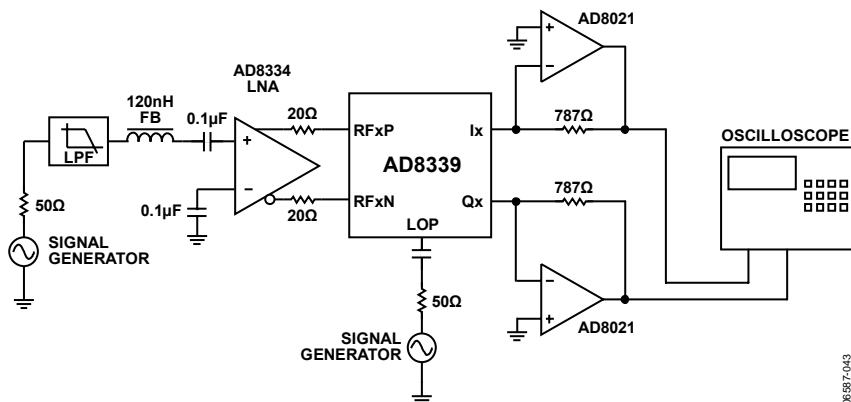


Figure 43. Phase and Amplitude vs. Baseband Frequency

06587-043

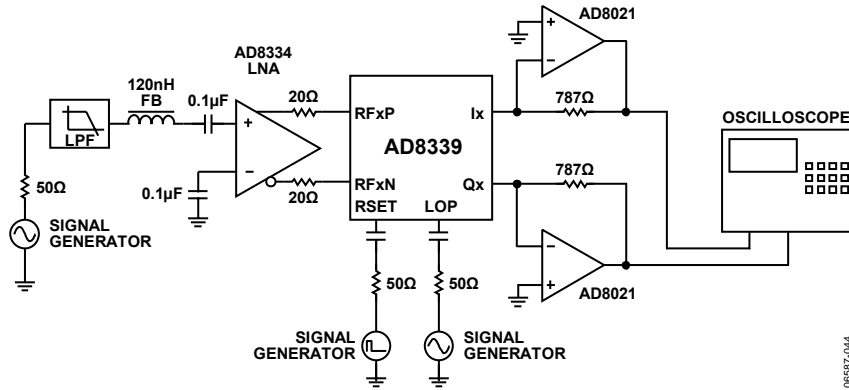


Figure 44. LO Reset Response

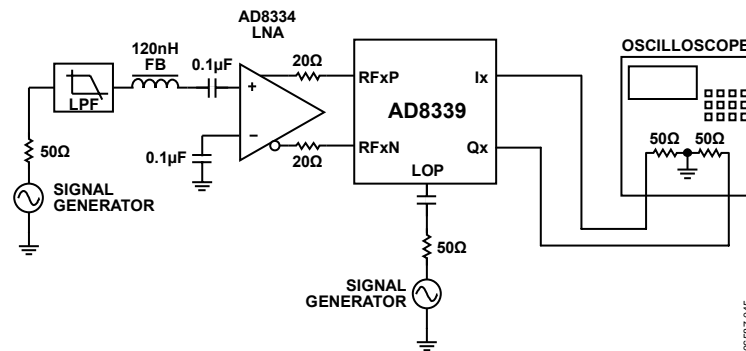


Figure 45. RF Input Range

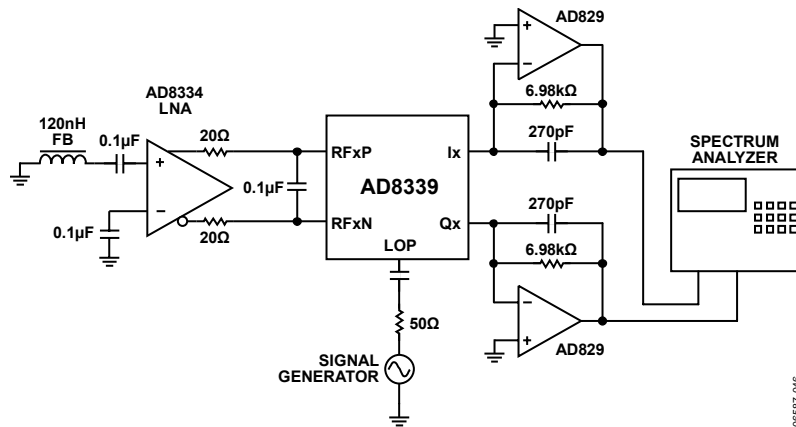


Figure 46. Noise

AD8339

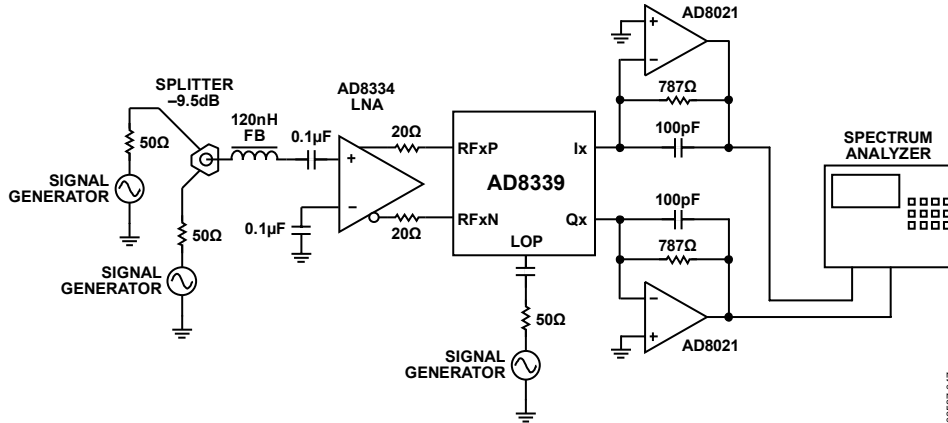


Figure 47. OIP3 vs. Baseband Frequency

06587-047

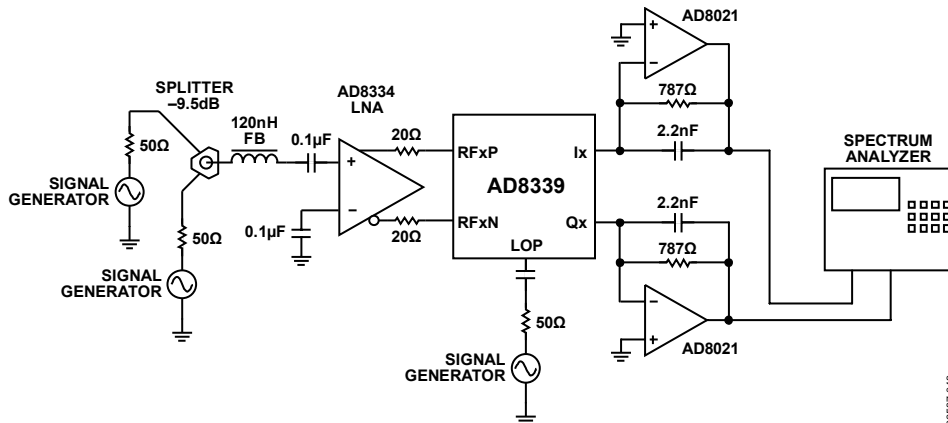


Figure 48. OIP3 and IM3 vs. RF Frequency

06587-048

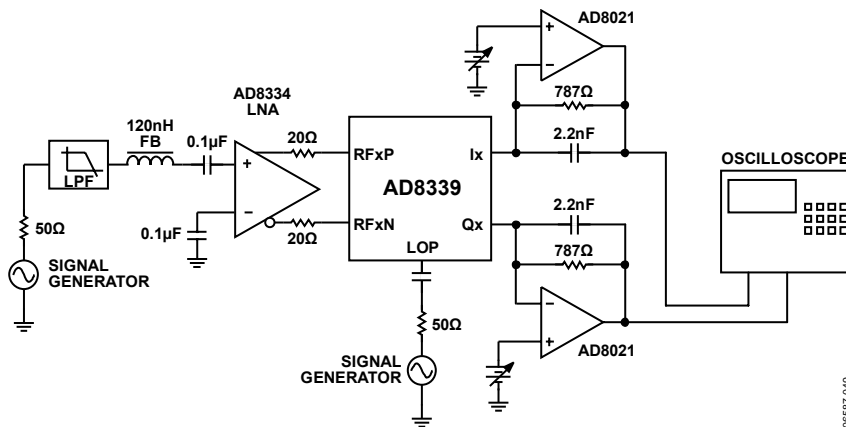


Figure 49. Output Compliance Range

06587-049

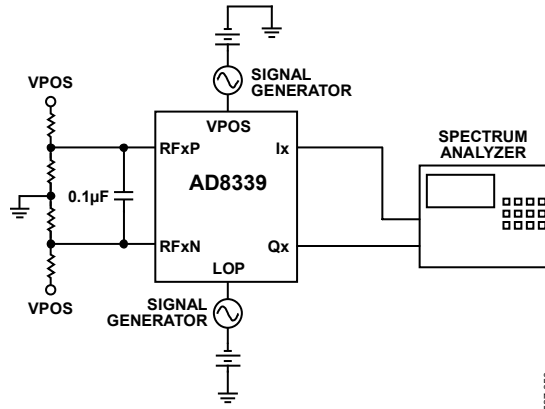


Figure 50. PSRR

06587-060

THEORY OF OPERATION

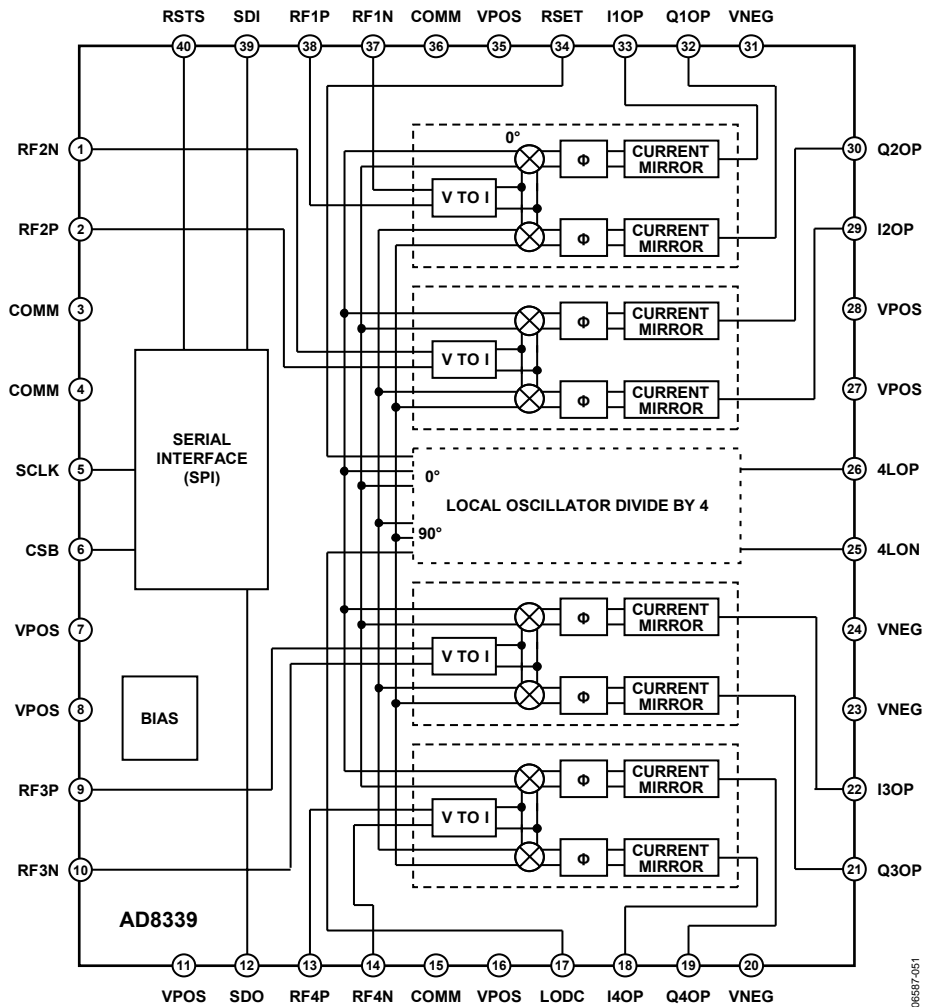


Figure 51. AD8339 Block Diagram

The AD8339 is a quad I/Q demodulator with a programmable phase shifter for each channel. The primary application is phased array beamforming in medical ultrasound. Other potential applications include phased array radar and smart antennas for mobile communications. The AD8339 can also be used in applications that require multiple well matched I/Q demodulators. The AD8339 is architecturally very similar to its predecessor, the [AD8333](#). The major differences are

- The addition of a serial (SPI) interface that allows daisy chaining of multiple devices
- Reduced power per channel

Figure 51 shows the block diagram and pinout of the AD8339. Four RF inputs that accept signals from the RF sources and a local oscillator (applied to differential input pins marked 4LOP and 4LON) common to all channels comprise the analog inputs. Each channel has the option to program 16 delay states/360° (or 22.5°/step) selectable via the SPI port. The part has two reset inputs: RSET is used to synchronize the LO dividers in multiple AD8339s used in arrays; RSTS is used to set the SPI port bits to all zeros. This can be useful in testing or to quickly turn off the device without first programming the SPI port.

Each of the current formatted I and Q outputs sum together for beamforming applications. Multiple channels are summed and converted to a voltage using a transimpedance amplifier. If desired, channels can also be used individually.

QUADRATURE GENERATION

The internal 0° and 90° LO phases are digitally generated by a divide-by-four logic circuit. The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals is intrinsically 50% and is unaffected by the asymmetry of the externally connected 4LO input. Furthermore, the divider is implemented such that the 4LO signal reclocks the final flip-flops that generate the internal LO signals and thereby minimizes noise introduced by the divide circuitry.

For optimum performance, the 4LO input is driven differentially, but can also be driven single-ended. A good choice for a drive is an LVDS device as is done on the evaluation board. The common-mode range on each pin is approximately 0.2 V to 3.8 V with the nominal ± 5 V supplies.

The minimum 4LO level is frequency dependent when driven by a sine wave. For optimum noise performance, it is important to ensure that the LO source has very low phase noise (jitter) and adequate input level to ensure stable mixer-core switching. The gain through the divider determines the LO signal level vs. RF frequency. The AD8339 can be operated to very low frequencies at the LO inputs if a square wave is used to drive the LO, as is done with the LVDS driver on the evaluation board.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. A reset pin is provided to synchronize the LO divider circuits in different AD8339s when they are used in arrays. The RSET pin resets the dividers to a known state after power is applied to multiple AD8339s. A logic input must be provided to the RSET pin when using more than one AD8339. Note that at least one channel must be enabled for the LO interface to also be enabled and the LO reset to work. See the Reset Input section in the applications section for more detail.

I/Q DEMODULATOR AND PHASE SHIFTER

The I/Q demodulators consist of double-balanced Gilbert cell mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability of 2.8 V p-p. These currents are then presented to the mixers, which convert them to baseband (RF – LO) and twice RF (RF + LO). The signals are phase shifted according to the codes programmed into the SPI latch (see Table 4); the phase bits are labeled PHx0 through PHx3 where 0 indicates LSB and 3 indicates MSB. The phase shift function is an integral part of the overall circuit (patent pending). The phase shift listed in Column 1 of Table 4 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to a pair of RF inputs to an AD8339, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and that of Channel 2 is 0001, then Channel 2 leads Channel 1 by 22.5°.

Following the phase shift circuitry, the differential current signal is converted from differential to single-ended via a current mirror. An external transimpedance amplifier is needed to convert the I and Q outputs to voltages.

Table 4. Phase Select Code for Channel-to-Channel Phase Shift

Φ Shift	PHx3 (MSB)	PHx2	PHx1	PHx0 (LSB)
0°	0	0	0	0
22.5°	0	0	0	1
45°	0	0	1	0
67.5°	0	0	1	1
90°	0	1	0	0
112.5°	0	1	0	1
135°	0	1	1	0
157.5°	0	1	1	1
180°	1	0	0	0
202.5°	1	0	0	1
225°	1	0	1	0
247.5°	1	0	1	1
270°	1	1	0	0
292.5°	1	1	0	1
315°	1	1	1	0
337.5°	1	1	1	1

DYNAMIC RANGE AND NOISE

Figure 52 is an interconnection block diagram of all four channels of the AD8339. More channels are easily added to the summation (up to 16 when using an AD8021 as the summation amplifier) by wire-OR connecting the outputs as shown for four channels. For optimum system noise performance, the RF input signal is provided by a very low noise amplifier, such as the LNA of the AD8332/AD8334 or the AD8335. In beamforming applications, the I and Q outputs of a number of receiver channels are summed (for example, the four channels illustrated in Figure 52). The dynamic range of the system increases by the factor $10\log_{10}(N)$, where N is the number of channels (assuming random uncorrelated noise). The noise in the 4-channel example of Figure 52 is increased by 6 dB while the signal quadruples (+12 dB), yielding an aggregate SNR improvement of $(+12 - 6) = +6$ dB.

Judicious selection of the RF amplifier ensures the least degradation in dynamic range. The input referred spectral voltage noise density (e_n) of the AD8339 is nominally ~ 11 nV/ $\sqrt{\text{Hz}}$. For the noise of the AD8339 to degrade the system noise figure (NF) by 1 dB, the combined noise of the source and the LNA should be approximately twice that of the AD8339, or 22 nV/ $\sqrt{\text{Hz}}$. If the noise of the circuitry before the AD8339 is less than 22 nV/ $\sqrt{\text{Hz}}$, the system NF degrades more than 1 dB. For example, if the noise contribution of the LNA and source is equal to the AD8339, or 11 nV/ $\sqrt{\text{Hz}}$, the degradation is 3 dB. If the circuit noise preceding the AD8339 is 1.3 \times as large as that of the AD8339 (or ~ 14 nV/ $\sqrt{\text{Hz}}$), the degradation is 2 dB. For a circuit noise 1.45 \times that of the AD8339 (16 nV/ $\sqrt{\text{Hz}}$), the degradation is 1.5 dB.

AD8339

To determine the input referred noise, it is important to know the active low-pass filter (LPF) values R_{FILT} and C_{FILT} , shown in Figure 52. Typical filter values for a single channel are 1.58 k Ω and 1 nF, and implement a 100 kHz single-pole LPF. In the case that two channels are summed, as is done on the evaluation board, the values are the same as for a single channel of the AD8333, namely 787 Ω and 2.2 nF.

If the RF and LO are offset by 10 kHz, the demodulated signal is 10 kHz and is passed by the LPF. The single-channel mixing gain, from the RF input to the AD8021 output (for example, I1', Q1') is approximately 1.7 (4.7 dB) for 1.58 k Ω and 1 nF, or 6 dB less when a single channel is operated on the evaluation board ($\times 0.85$; -1.3 dB). This, together with the 11 nV/ $\sqrt{\text{Hz}}$ of AD8339 noise, results in ~ 18.7 nV/ $\sqrt{\text{Hz}}$ at the AD8021 output. Because the AD8021, including the 1.58 k Ω feedback resistor, contributes another 6.3 nV/ $\sqrt{\text{Hz}}$, the total output referred noise is approximately 19.7 nV/ $\sqrt{\text{Hz}}$. This value can be adjusted by increasing the filter resistor while maintaining the corner

frequency, thereby increasing the gain. The factor limiting the magnitude of the gain is the output swing and drive capability of the op amp selected for the I-to-V converter, in this instance, the AD8021.

Because any amplifier has limited drive capability, there is a finite number of channels that can be summed. This is explained in detail in the Channel Summing section.

SUMMATION OF MULTIPLE CHANNELS (ANALOG BEAMFORMING)

Beamforming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals generated from a common source, but received at different times by a multi-element ultrasound transducer. Beamforming has two functions: it imparts directivity to the transducer, enhancing its gain and it defines a focal point within the body from which the location of the returning echo is derived. The primary application for the AD8339 is in analog beamforming circuits for ultrasound.

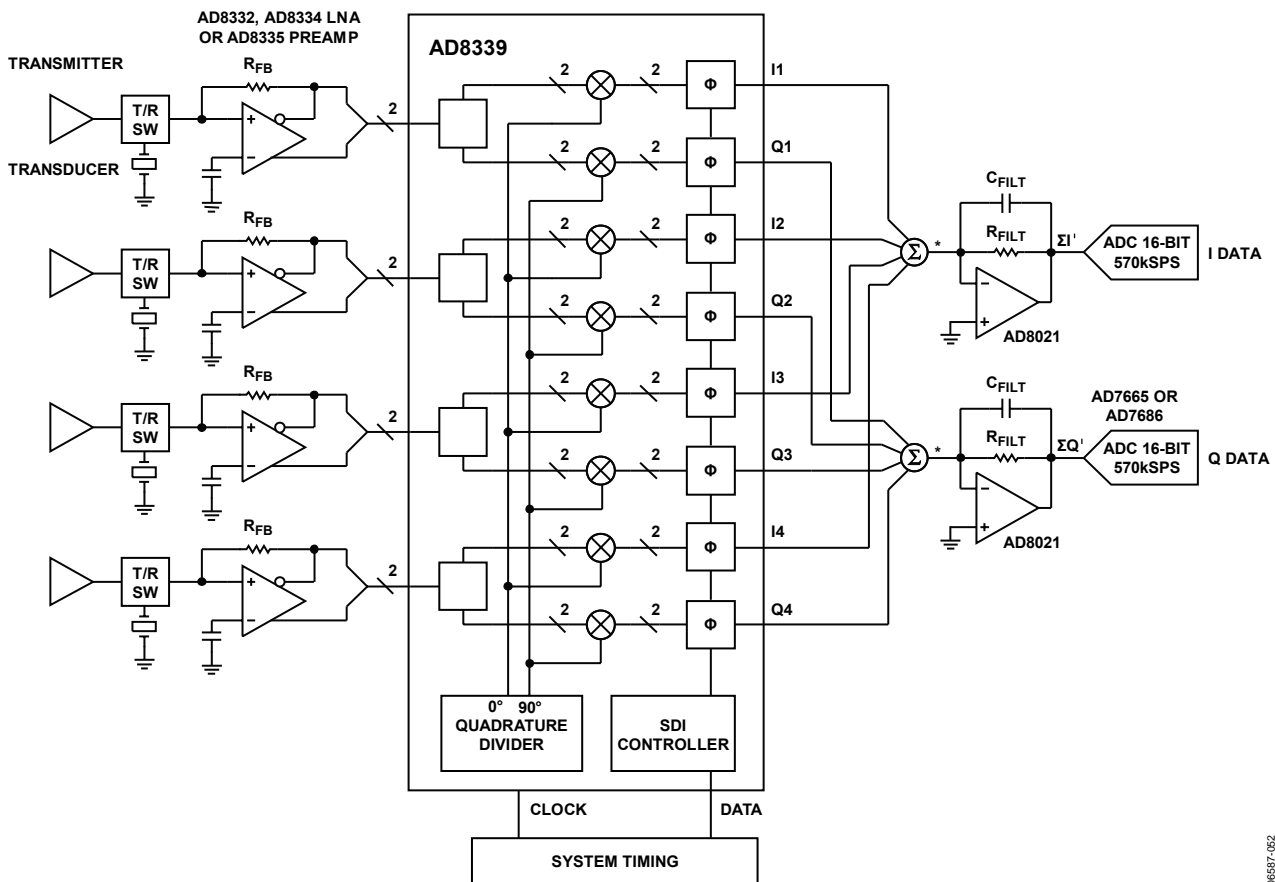


Figure 52. Interconnection Block Diagram for AD8339

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PHASE COMPENSATION AND ANALOG BEAMFORMING

Modern ultrasound machines used for medical applications employ an array of receivers for beamforming, with typical CW Doppler array sizes of up to 64 receiver channels that are phase shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N , where N is the number of channels), while the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beamformer design are the means to align the incoming signals in the time domain, and the means to sum the individual signals into a composite whole.

In traditional analog beamformers incorporating Doppler, a V-to-I converter per channel and a crosspoint switch precede passive delay lines used as a combined phase shifter and summing circuit. The system operates at the carrier frequency (RF) through the delay line, which also sums the signals from the various channels, and then the combined signal is down-converted by a very large dynamic range I/Q demodulator.

The resultant I and Q signals are filtered and then sampled by two high resolution analog-to-digital converters. The sampled signals are processed to extract the relevant Doppler information.

Alternatively, the RF signal can be processed by downconversion on each channel individually, phase shifting the downconverted signal, and then combining all channels. The AD8333 and the AD8339 implement this architecture. The downconversion is done by an I/Q demodulator on each channel, and the summed current output is the same as in the delay line approach. The subsequent filters after the I-to-V conversion and the ADCs are similar.

The AD8339 integrates the phase shifter, frequency conversion, and I/Q demodulation into a single package, and directly yields the baseband signal. Figure 53 is a simplified diagram showing the idea for all four channels. The ultrasound wave (USW) is received by four transducer elements, TE1 through TE4, in an ultrasound probe and generates signals E1 through E4. In this example, the phase at TE1 leads the phase at TE2 by 45° .

CHANNEL SUMMING

The circuit shown in Figure 55 of the AD8333 data sheet can be used to sum 32 channels of the AD8339. The reason for this is that the peak output currents of the AD8339 are approximately half of those of the AD8333. As is explained in the Channel Summing section of the AD8333 data sheet, the channel-summing limit relates directly to the current drive capability of the amplifier used to implement the active low-pass filter and current-to-voltage converter shown in Figure 52. The maximum sum, when the AD8021 is used, is 16 channels of the AD8339 vs. eight channels of the AD8333; that is, four AD8339s ($4 \times 4 = 16$ channels) can be summed in one AD8021.

In a real application, the phase difference depends on the element spacing, λ (wavelength), speed of sound, angle of incidence, and other factors. The signals E1 through E4 are amplified 19 dB by the low noise amplifiers in the AD8334; for lower performance portable ultrasound applications, the combination of the AD8335 and the AD8339 result in the lowest power per channel. For optimum signal-to-noise performance, the output of the LNA is applied directly to the input of the AD8339. In order to sum the signals E1 through E4, E2 is shifted 45° relative to E1 by setting the phase code in Channel 2 to 0010, E3 is shifted 90° (0100), and E4 is shifted 135° (0110). The phase aligned current signals at the output of the AD8339 are summed in an I-to-V converter to provide the combined output signal with a theoretical improvement in dynamic range of 6 dB for the four channels.

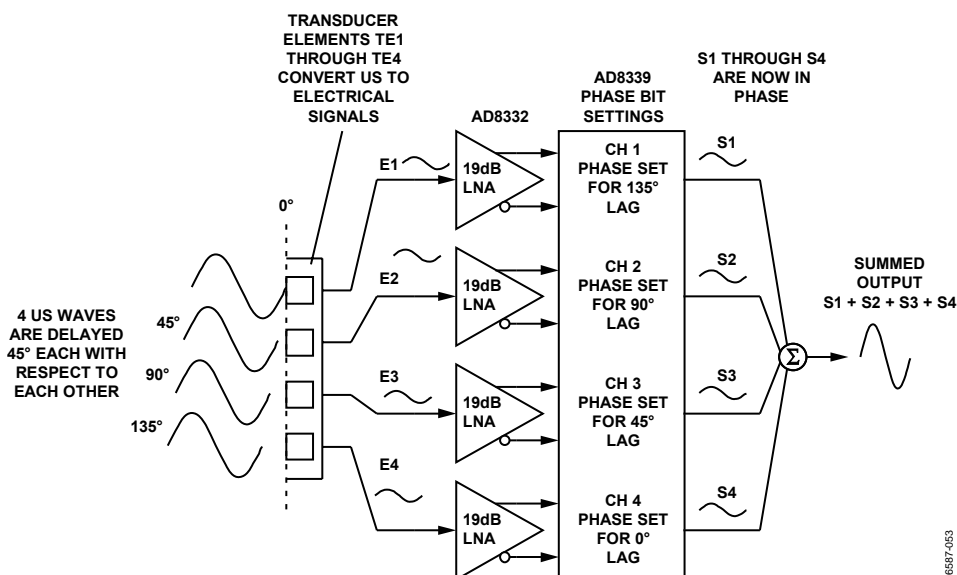


Figure 53. Simplified Example of the AD8339 Phase Shifter

SERIAL INTERFACE

The AD8339 contains a 4-wire SPI-compatible digital interface (SDI, SCLK, CSB, and SDO). The interface comprises a 20-bit shift register plus a latch. The shift register is loaded MSB first. Phase selection and channel enabling information are contained in the 20-bit word. Figure 54 is a bit map of the data-word, and Figure 55 is the timing diagram.

The shift direction is to the right with MSB first. Because the latch is implemented with D-flip-flops (DFF) and CSB acts as the clock to the latch, anytime that CSB is low, the latch flip-flops monitor the shift register outputs. As soon as CSB goes high, the data present in the register is latched. New data can be loaded into the shift register at any time.

Twenty bits are required to program each AD8339 and the data transfers from the register to the latch when CSB goes high. Depending on the data, the corresponding channels are enabled, and the phases are selected. Figure 55 illustrates the timing for two sequentially programmed devices.

Note that the data is latched into the register flip-flops on the rising edge of SCLK, which means that the data output transitions when SDO goes high.

ENBL BITS

When all four ENBL bits are low, only the SPI port is powered up. This feature allows for low power consumption (~13 mW per AD8339 or 3.25 mW per channel) when the CW Doppler function is not needed. Because the SPI port stays alive even with the rest of the chip powered down, the part can be awakened again by simply programming the port. As soon as the CSB signal goes high, the part turns on again. Note that this takes a fair amount of time because of the external capacitor on the LODC pin. It takes ~10 μ s to 20 μ s with the recommended 0.1 μ F decoupling capacitor. The decoupling capacitor on this pin is intended to reduce bias noise contribution in the LO divider chain. The user can experiment with the value of this decoupling capacitor to determine the smallest value without degrading the dynamic range within the frequency band of interest.

The SPI also has an additional pin that can be used in a test mode, or as a quick way to reset the SPI and depower the chip. All bits in both the shift register and the latch are reset low when Pin RSTS is pulled above ~1.5 V. For quick testing without the need to program the SPI, the voltage on the RSTS pin should be first pulled high and then pulled to -1.4 V; this enables all four channels in the (I = 1, Q = 0) state (all phase bits are 0000); the channel enable bits are all set to 1.

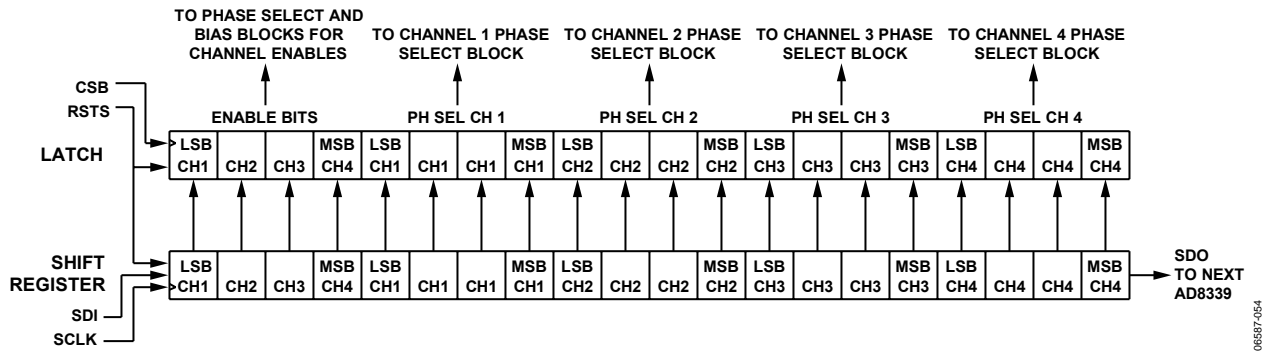


Figure 54. Serial Interface Showing the 20-Bit Shift Register and Latch

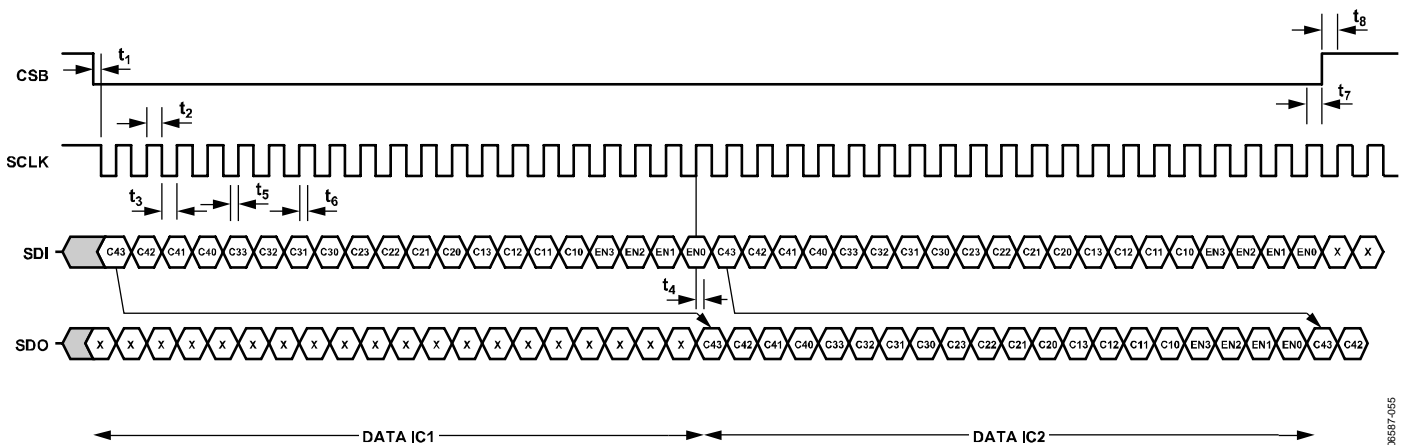


Figure 55. Timing Diagram

APPLICATIONS

The AD8339 is the key component of a phase shifter system that aligns time-skewed information contained in RF signals. Combined with a variable gain amplifier (VGA) and a low noise amplifier (LNA) as in the AD8332/AD8334/AD8335 VGA family, the AD8339 forms a complete analog receiver for a high performance ultrasound CW Doppler system.

LOGIC INPUTS AND INTERFACES

The SDI, SCLK, SDO, CSB, and RSET pins are CMOS compatible to 1.8 V. The threshold of the RSTS pin is 1.5 V, with a hysteresis of ± 0.3 V. Each logic input pin is Schmitt trigger activated, with a threshold centered at ~ 1.3 V, and a hysteresis of ± 0.1 V around this value.

The only logic output, SDO, generates a signal that has a logic low level of ~ 0.2 V and a logic high level of ~ 1.9 V to allow for easy interfacing to the next AD8339 SDI input. Note that the capacitive loading for the SDO pin should be kept as small as possible (< 5 pF), ideally only a short trace to the SDI pin of the next chip. The output slew is limited to approximately ± 500 μ A, which limits the speed when a large capacitor is connected. Excessive values of parasitic capacitance on the SDO pin can affect the timing and loading of data into the next chip's SDI input.

RSET INPUT

The RSET pin is used to synchronize the LO dividers in AD8339 arrays. Because they are driven by the same internal LO, the four channels in any AD8339 are inherently synchronous. However, when multiple AD8339s are used, it is possible that their dividers wake up in different phase states. The function of the RSET pin is to phase align all the LO signals in multiple AD8339s.

The 4LO divider of each AD8339 can initiate in one of four possible states— 0° , 90° , 180° , and 270° , relative to other AD8339s. The internally generated I/Q signals of each AD8339 LO are always at a 90° angle relative to each other, but a phase shift can occur during power-up between the dividers of multiple AD8339s used in a common array.

The LO divider reset function has been improved in the AD8339 over the AD8333. The RSET pin still provides an asynchronous reset of the LO dividers by forcing the internal LO to hang; however, in the AD8339, the LO reset function is fast and does not require a shutdown of the 4LO input signal.

The RSET mechanism also allows the measurement of non-mixing gain from the RF input to the output. The rising edge of the active high RSET pulse can occur at any time; however, the duration should be ≥ 20 ns minimum. When the RSET pulse transitions from high to low, the LO dividers are reactivated on the next rising edge of the 4LO clock. To guarantee synchronous operation of an array of AD8339s, the RSET pulse must go low on all devices before the next rising edge of the 4LO clock. Therefore, it is best to have the RSET pulse go low on the falling edge of the 4LO clock; at the very least, the t_{SETUP} should be ≥ 5 ns. An optimal timing setup would be for the RSET pulse to go high on a 4LO falling edge and to go low on a 4LO falling edge; this gives 10 ns of setup time even at a 4LO frequency of 50 MHz (12.5 MHz internal LO).

Check the synchronization of multiple AD8339s using the following procedure:

1. Activate at least one channel per AD8339 by setting the appropriate channel enable bit in the serial interface.
2. Set the phase code of all AD8339 channels to the same logic state, for example, 0000.
3. Apply the same test signal to all devices that generates a sine wave in the baseband output and measure the output of one channel per device.
4. Apply a RSET pulse to all AD8339s.
5. Because all the phase codes of the AD8339s should be the same, the combined signal of multiple devices should be N times greater than a single channel. If the combined signal is less than N times one channel, then one or more of the LO phases of the individual AD8339s is in error.

LO INPUT

The LO input is a high speed, fully differential, analog input that responds to differences in the input levels (and not logic levels). The LO inputs can be driven with a low common-mode voltage amplifier, such as the National Semiconductor DS90C401 LVDS driver. The graph in Figure 21 shows the range of common-mode voltage. Logic families, such as TTL or CMOS, are unsuitable for direct coupling to the LO input.

AD8339

EVALUATION BOARD

Figure 56 is a photograph of the AD8339 evaluation board, and the schematic diagram is shown in Figure 61, Figure 62, and Figure 63. Four single-ended RF inputs can be phase aligned using the LNA inputs of an AD8334 and the 16 phase adjustment options of the AD8339. The RF input signals can be derived from three sources, user selectable by jumpers. Test points enable signal tracing at various circuit nodes.

The AD8339 requires dual power supplies, the AD8334 and digital section only a single supply. A 3.3 V on-board regulator provides power for the USB and EEPROM devices. The AD8339 can be configured using the software provided on the CD-ROM included with the board, or using an external digital pattern generator via the 20-pin flat-cable connector.

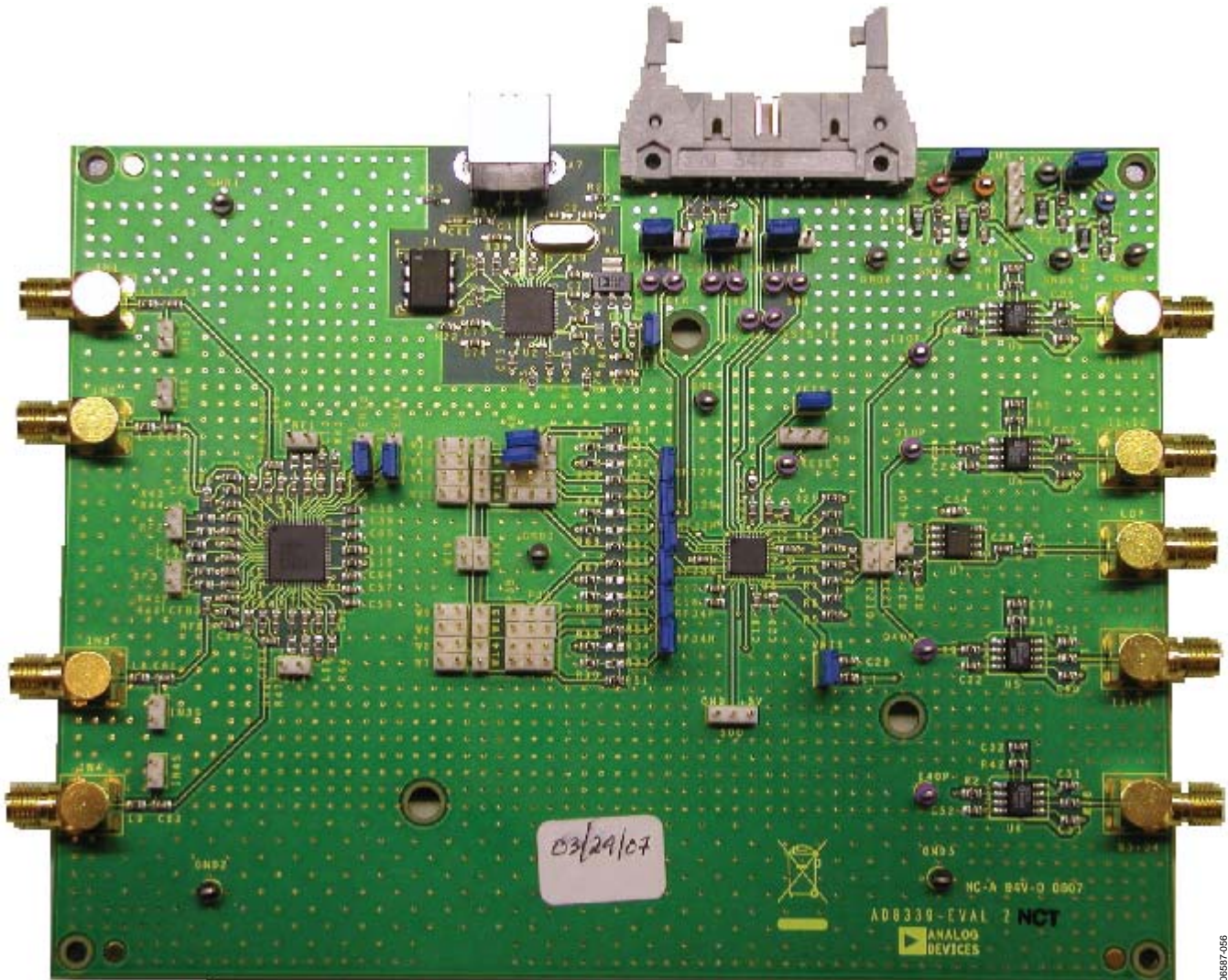


Figure 56. AD8339 Evaluation Board

CONNECTIONS TO THE BOARD

Table 5 is a list of equipment required to activate the board with suggested test equipment, and Figure 59 shows a typical setup. In order to phase align any two RF input signals, the RF and clock inputs must be coherent, that is, from the same timing source. Many laboratory signal generators have this capability, including the Rohde & Schwartz model shown in Table 5. Other signal generators can also be used; the only requirement is that they have external clock inputs and outputs. Selecting the frequency of the generators is quite simple. As an example, select an RF frequency of interest, for example 5 MHz. Then select the 4LO frequency, which is four times the RF frequency, in this example 20 MHz. The output frequency is 0 Hz—note that the AD8021 outputs are at either a positive or negative dc voltage under this condition under perfect RF and 4LO frequency lock; more likely the signal is slowly varying if the lock is not perfect.

To detect an output, advance or retard the RF frequency by the desired baseband frequency. A baseband frequency of 10 kHz at the output results from an RF frequency of 5.01 MHz or 4.99 MHz.

Table 5. Recommended Equipment List

Description	Suggested Equipment
Signal Generators (2), with Synchronizing Connectors 4-Channel Oscilloscope	Rohde & Schwartz SMT3 or equivalent Tektronix DPO7104 or equivalent
Power Supplies Scope Probes (4)	Agilent E3631A or equivalent Tektronix P6104 or equivalent

TEST CONFIGURATIONS

The three test configuration options for the AD8339-EVALZ are common input, independent input, and AD9271 drive.

Common Input Signal Drive

Figure 57 is a block diagram showing the simplest way to use the evaluation board, with a common signal applied to all four AD8339 inputs in parallel. Boards are configured this way as shipped. The inputs of each of the channels are connected in common by means of jumpers, as shown in Table 6, although they can be just as easily connected to any of the AD8334 LNA outputs. As seen in Figure 62, two pairs of summing amplifiers provide the I and Q outputs so that Channel 1 and Channel 2 can be observed independently of Channel 3 and Channel 4.

Using a common input signal source as shown in Figure 59, the same input is applied to all four channels of the AD8339. To observe an output at the I or Q connectors, simply enable the appropriate channel or channels using the menu shown in Figure 60. For example, if only Channel 1 is enabled and the phases set to 0°, a waveform is seen at the I1 + I2 and Q1 + Q2 outputs. If Channel 2 is enabled with the phase also set to 0°, the amplitude of the waveforms double. If Channel 1 is 0° and Channel 2 phase set to 180°, the output becomes zero because the phases of the two channels cancel.

When using the common input drive mode, it is important that only the top two positions of P4A and P4B be used to avoid shorting the LNA outputs together.

Independent Channel Drive

Independent input mode means that each channel is driven by an LNA. Of course, the LNA inputs of the AD8334 can be driven by up to four independent signal generators or from a single generator. If the user chooses this mode, it is important not to connect the LNA inputs in parallel because of the active matching feature. Any standard splitter can be used.

AD9271 Input Drive

Connectors P3A, P3B and P4A, P4B are configured to route input signals from the AD8334 LNA outputs or from an AD9271 evaluation board. The AD9271 is an octal ultrasound front end with a 12-bit ADC for each channel. When using an AD9271 as an input drive, consult the AD9271 data sheet for setup details.

The AD9271 board is attached to the AD8339 by inserting the three plastic standoffs into the three guide holes in the AD8339-EVALZ board; all the jumpers in P3 and P4 are removed. The bottom connectors of the AD9271 board engage P3 and P4 and route the LNA outputs of the AD9271 to the AD8339. Figure 58 is a photograph of the two boards attached.

Table 6. P3, P4 Input Jumper Configuration

Common Input	Independent Input
P4A-1 to P4B-1, top two positions (2)	P3A-1 to P3B-1, P4A-1 to P4B-1
RF12N, RF12P, RF23N, RF23P, RF34N, RF34P	P3A-1 to P3B-1, P4A-1 to P4B-1, all positions (8)

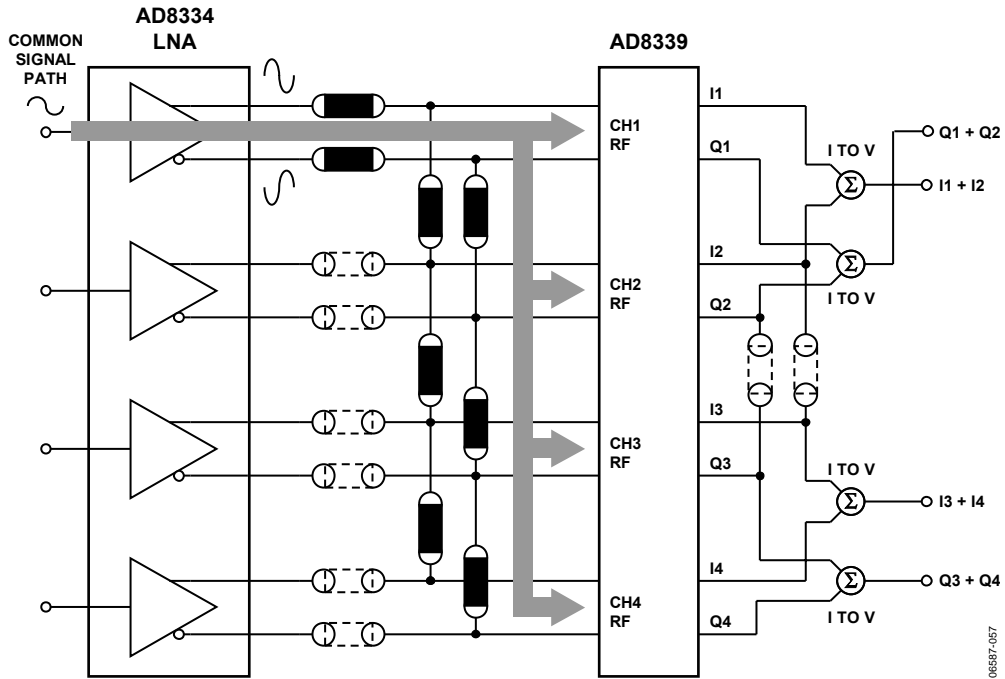


Figure 57. AD8339 Test Configuration—Common Signal Input Drive

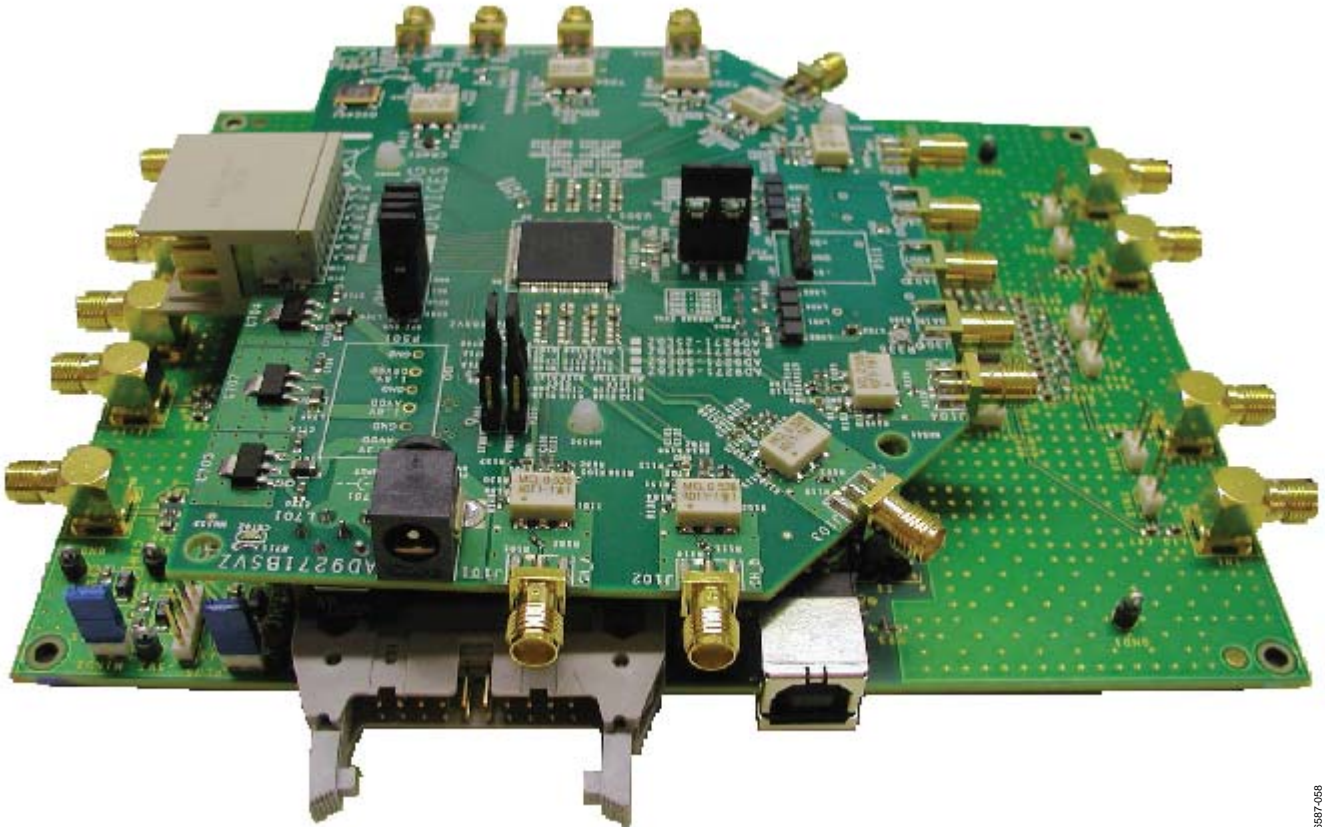


Figure 58. AD8339-EVALZ with AD9271 Attached as Input Source

TOP:
SIGNAL GENERATOR FOR 4LO INPUT (e.g., 20MHz, 1Vp-p)
BOTTOM:
SIGNAL GENERATOR FOR RF INPUT (e.g., 5.01MHz)

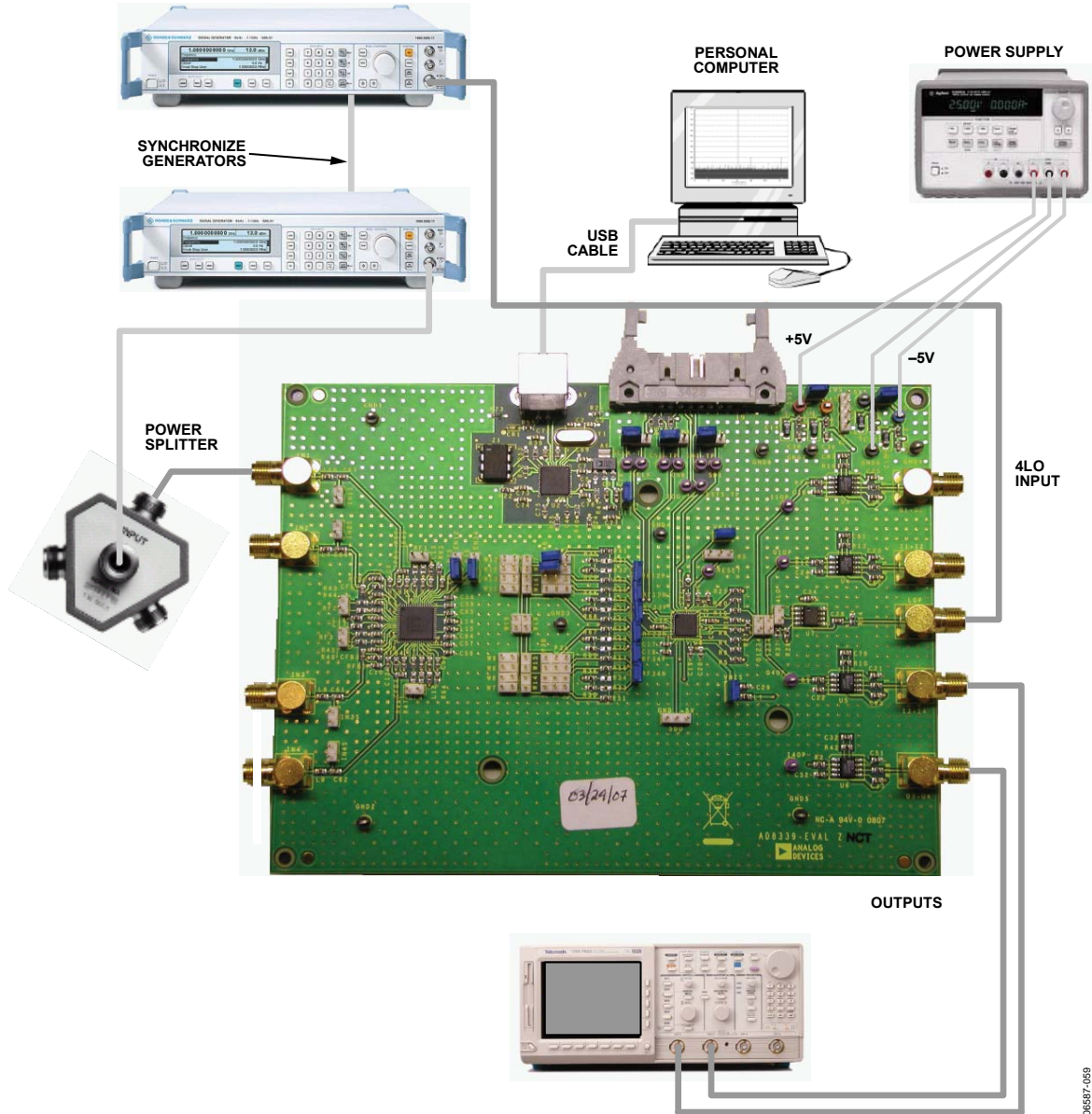


Figure 59. AD8339-EVALZ Typical Test Setup

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AD8339

Using the SPI Port

Channel and phase selection are accessed via the SPI port on the AD8339 and the evaluation board provides two means of access. If it is desired to exercise the SPI input with custom waveforms, the SDI, SCLK, and CSB are available at the auxiliary connector P1. A digital pattern generator can be programmed in conformance with the timing diagram shown in Figure 55.

The most convenient way to select channels and phase delays is through the USB port of a PC using the executable program provided on the CD-ROM or the Analog Devices, Inc. website. Copy the .EXE and .MSI files into the same folder on the PC. Double-click on the .EXE file and the program will self-install and place a shortcut on the desktop. Double-clicking on the desktop icon brings up the control menu, as shown in Figure 60. The menu consists of an array of radio buttons that are self-

explanatory. Channels are enabled or disabled by clicking on the boxes in the list, and the 16 phase options are selected from a drop-down menu for each of the channels.

Hardwired Jumpers

Hardwired jumpers provide for interconnection of channels and as a means for measuring output voltages at various strategic modes.

When shipped, the board is configured to connect all the AD8339 RF inputs to a single LNA output. In this configuration, the phases of the four channels can be shifted throughout the full range and the outputs viewed on a multichannel scope using one of the channels as a reference. To operate all the LNA channels independently, it is only necessary to move the input shorting jumpers to the channel RF outputs.

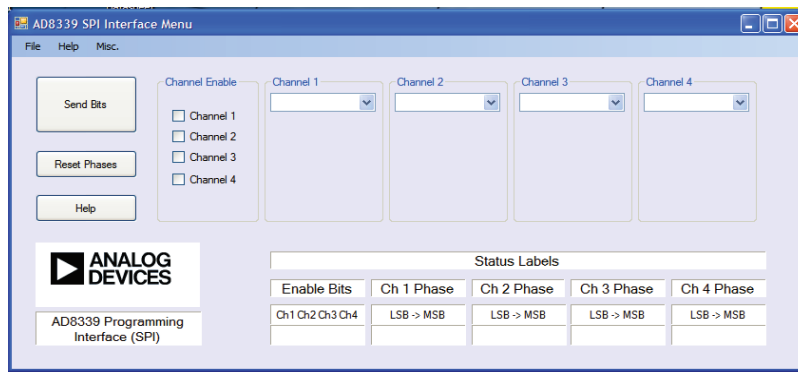


Figure 60. SPI Software Control Menu

Table 7. Jumper and Header List

Jumper, Header	Description
AxSHT	Shorts the current summing outputs—shipped omitted
CSB	Connects the chip select input to the connector or the USB inputs—normally connected to USB (test)
CSBG	Grounds the CSB input—shipped omitted
EN12, EN34	Enables or disables Channel 1 through Channel 4—boards shipped enabled
G12, G34	Connects gain pin for Channel 1 through Channel 4 to ground—boards are shipped with these jumpers inserted
I1234	Sums all four I-channel current outputs together—shipped omitted
Q1234	Sums all four Q-channel current outputs together—shipped omitted
RF1 to RF4	Test points for the LNA outputs—a differential probe fits these
RSTS	Resets the SPI input—shipped omitted
RSET	Resets the local oscillator input—shipped omitted
SDIG	Grounds the SDI input
SCLK	Connects the S-clock input to the connector or the USB inputs—normally connected to USB (test)
SDI	Connects the serial data input to the connector or the USB input—normally connected to USB (test)
SLKG	Grounds the S-clock input—shipped omitted
VO1 to VO4	Test points for the VGA outputs—a differential probe fits these
4LO	Test pins for the 4LO level shifter output—a differential probe fits these

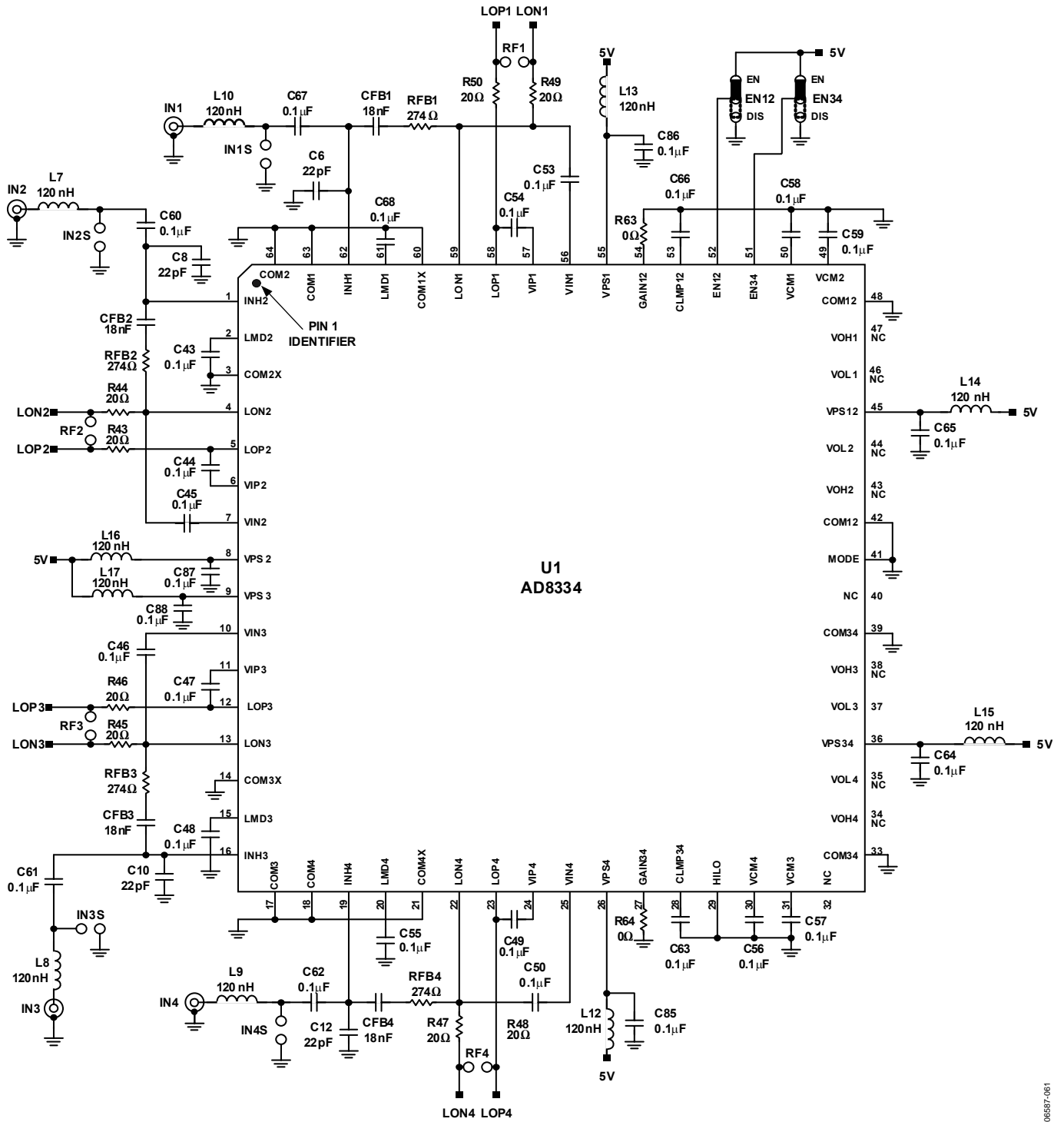


Figure 61. Schematic—LNA Section

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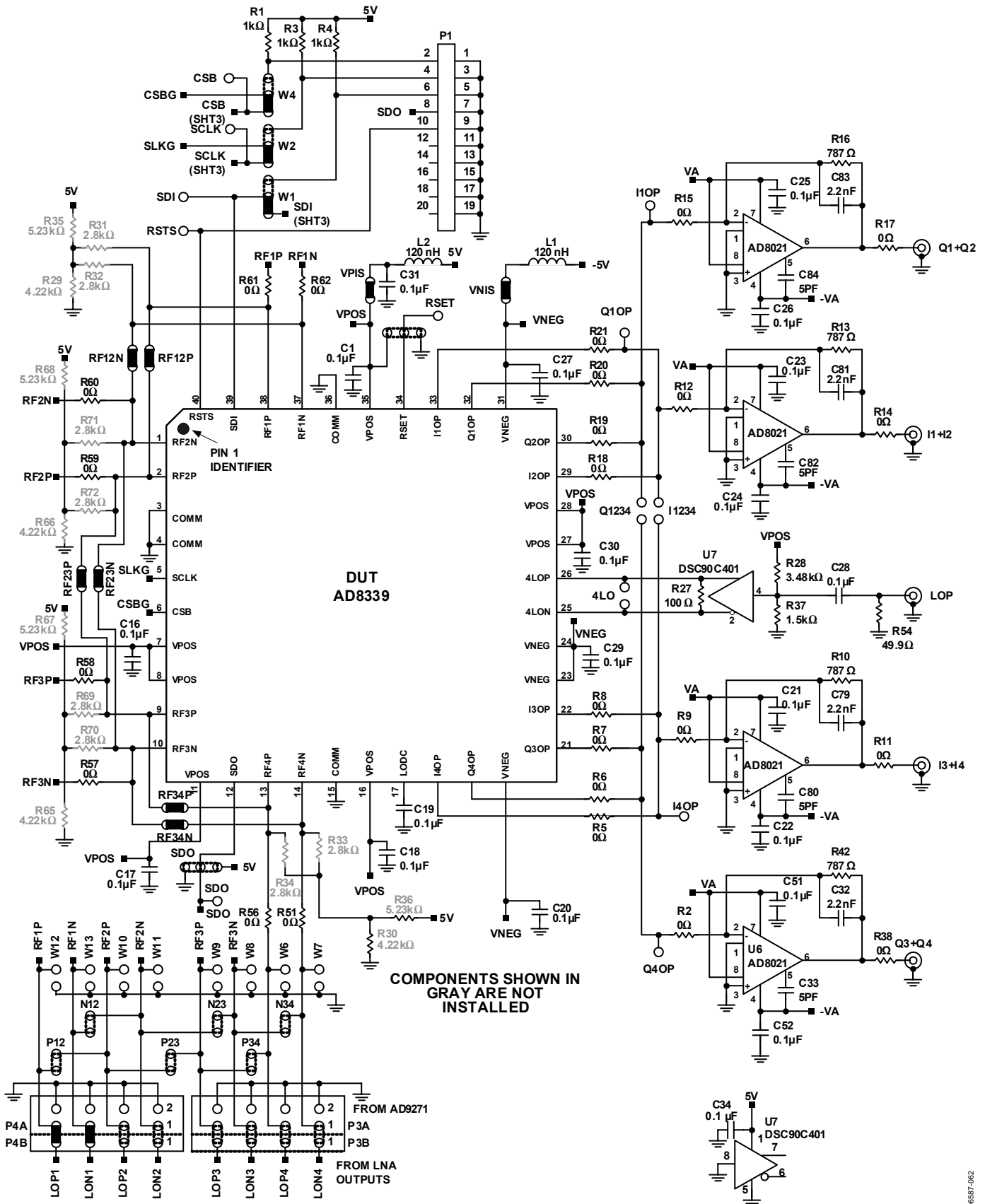


Figure 62. Schematic—IQ Demodulator and Phase Shifter

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AD8339-EVALZ ARTWORK

Figure 64 through Figure 67 show the artwork for the AD8339-EVALZ.

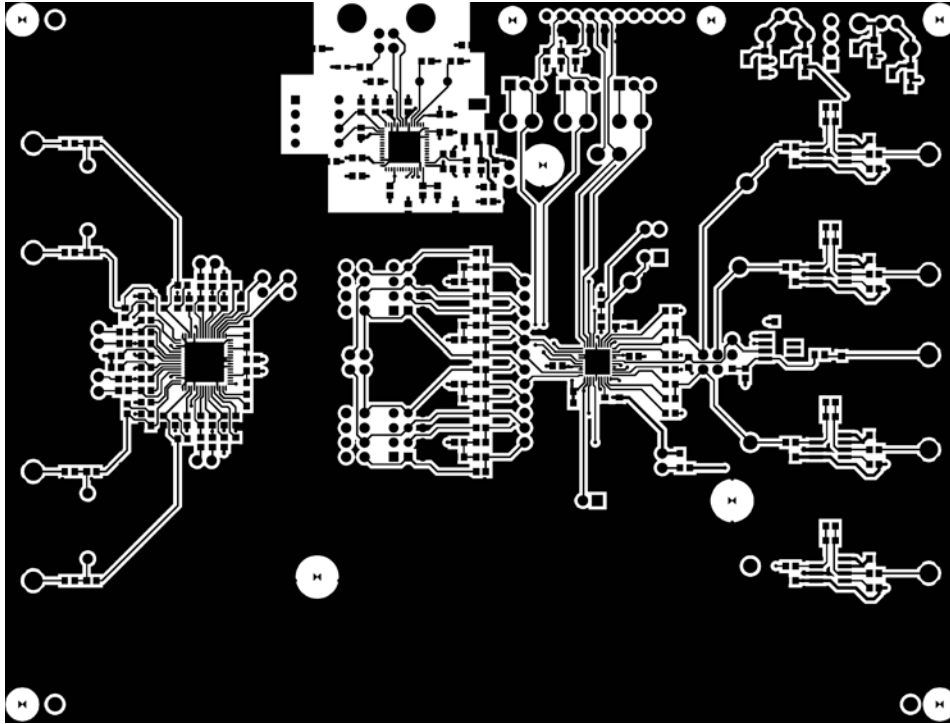


Figure 64. AD8339-EVALZ Component Side Copper

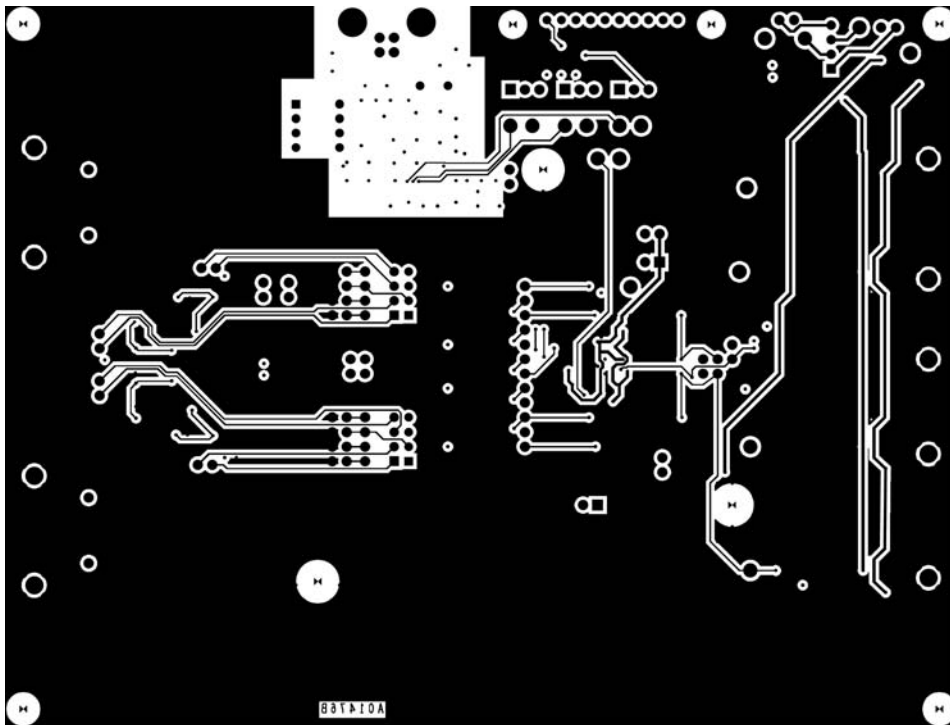


Figure 65. AD8339-EVALZ Wiring Side Copper

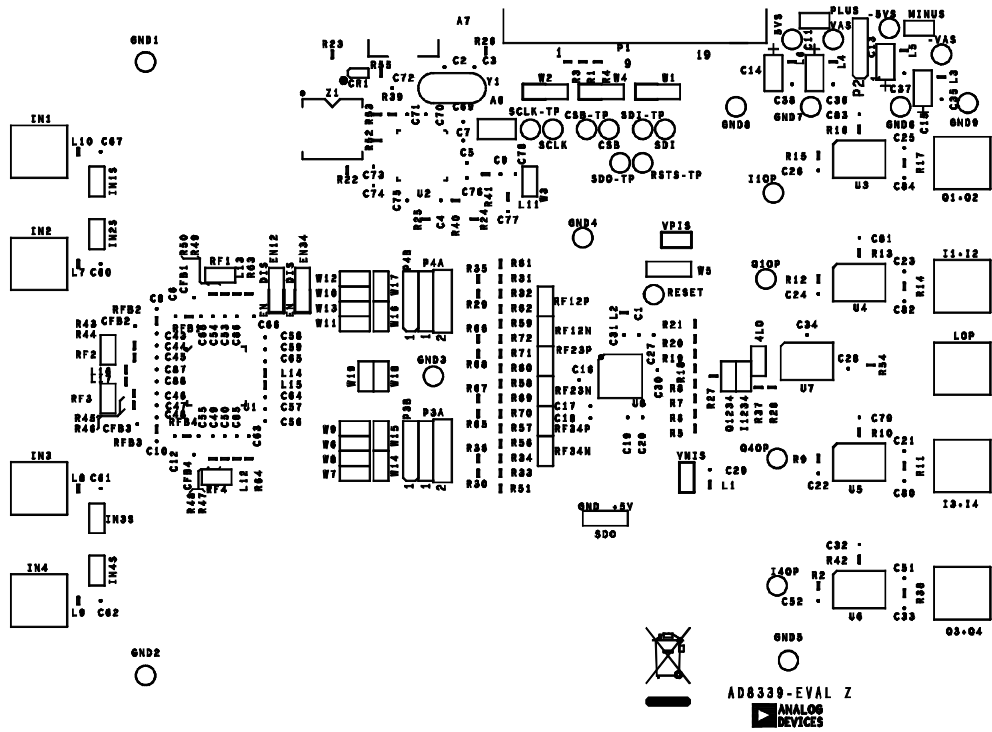


Figure 66. AD8339-EVALZ Component Side Silkscreen

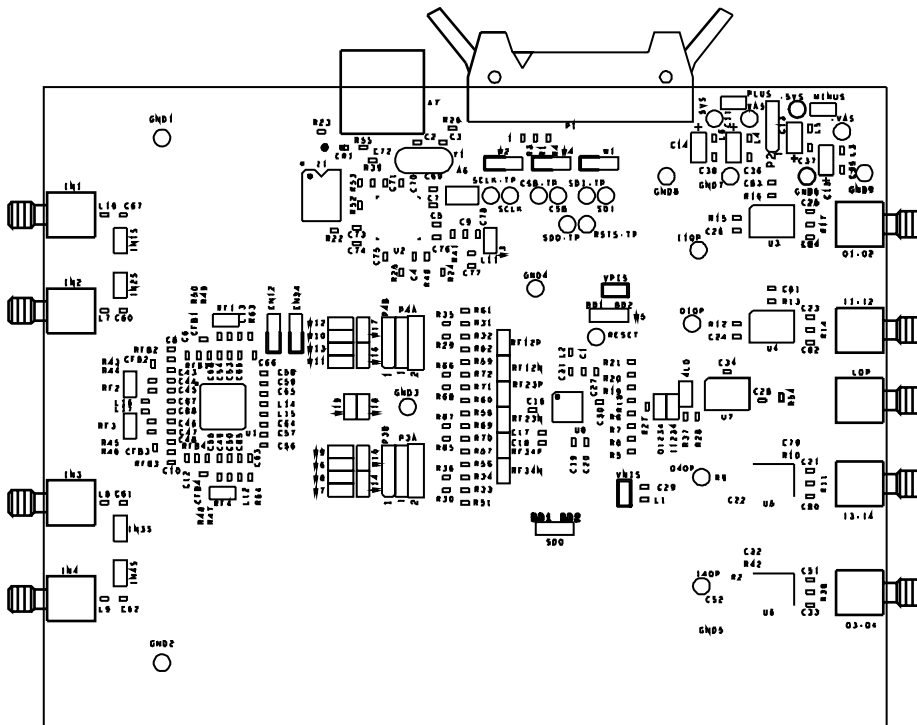


Figure 67. AD8339-EVALZ Assembly

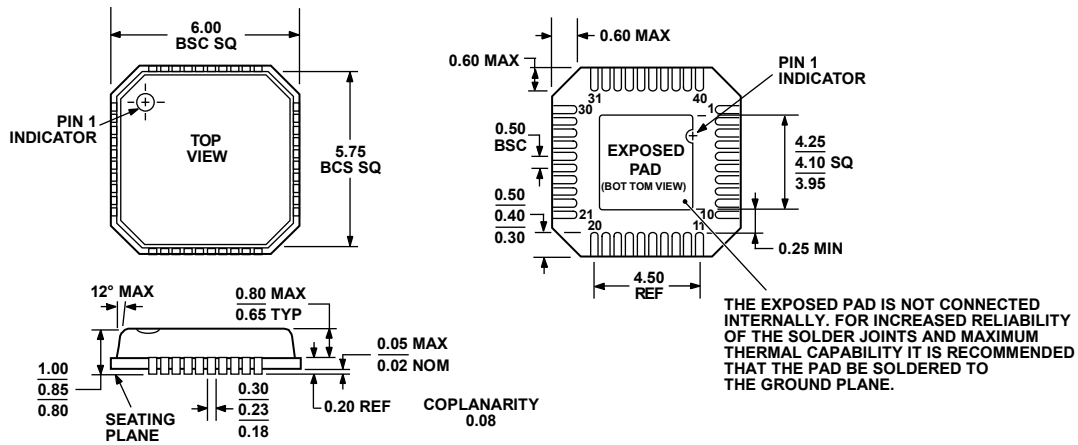
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Table 8. Bill of Materials

Qty	Name	Description	Reference Designator	Manufacturer	Part Number
1	Test Loop	Green	-5VS	Components Corp.	TP-104-01-05
1	Test Loop	Blue	-VAS	Components Corp.	TP-104-01-06
24	Header	Berg 2	4LO, I1234, IN1S, IN2S, IN3S, IN4S, MINUS, PLUS, Q1234, RF1, RF2, RF3, RF4, RF12N, RF12P, RF23N, RF23P, RF34N, RF34P, VNIS, VPIS, WQ3, W18, W19	Molex	22-10-2021
1	Test Loop	Red	+VS	Components Corp.	TP-104-01-02
1	Integrated Circuit	3.3 V regulator	A6	Analog Devices	AD3339AKCZ-3.3-RL
1	Connector	Right angle USB, Type B, 4-position	A7	Tyco	292304-1
63	Capacitor	0.1 μ F, 16 V, 0603 X7R	C1, C7, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C34, C35, C36, C37, C38, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C85, C86, C87, C88	Kemet	C0603C104K4RACTU
2	Capacitor	12 pF, 50 V, 5%, 0603	C2, C3	AVX	06035A120JAT2A
6	Capacitor	22 pF, 50 V, 5%, 0603	C4, C5, C6, C8, C10, C12	Panasonic	ECJ-1VC1H220J
1	Capacitor	1 μ F, 6.3 V, 10%, 0603	C9	Panasonic	ECJ-1VB0J105K
4	Capacitor	Tantalum 10 μ F, 10 V, 20%, 3216, SMD	C11, C13, C14, C15	Nichicon	F931A106MAA
4	Capacitor	2.2 nF, 50 V, 10%, 0603	C32, C79, C81, C83	Panasonic	ECJ-1VB1H222K
4	Capacitor	5 pF, 50 V, 0603	C33, C80, C82, C84	Panasonic	ECJ-1VC1H050C
4	Capacitor	0.018 μ F, 10%, 50 V, X7R, 0603	CFB1, CFB2, CFB3, CFB4	AVX	06035C183KAT2A
1	LED	Green, USS type, 0603	CR1	Panasonic	LNJ314G8TRA
12	Test Loop	Purple	CSB, CSB-TP, I10P, I40P, Q10P, Q40P, RESET, RSTS-TP, SCLK-TP, SDI, SDI-TP, SDO-TP	Components Corp.	TP-104-01-07
1	Integrated Circuit	Quad I/Q demodulator	U8	Analog Devices	AD8339ACPZ
7	Header	Berg 3	EN12, EN34, SDO, W1, W2, W4, W5	Molex	22-10-2031
9	Test Loop	Black	GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9	Components Corp.	TP-104-01-00
9	Connector	SMA right angle	I1 + I2, I3 + I4, IN1, IN2, IN3, IN4, LOP, Q1 + Q2, Q3 + Q4	Amphenol	901-143-6RFX
17	Bead	Ferrite, 120 μ H	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17	Murata	BLM18BA750SN1D
1	Connector	20-pin RT/A latch eject	P1	3M	3428-5603
3	Connector	Header, vertical, 1" 1X4 30AU	P2, Positions W14 to W15, Positions W16 to W17	Molex	22-10-2041
2	Connector	Header, vertical, 1" 3X4P 30AU	Positions 3A to 3B, Positions 4A to 4B	Samtec	TSW-104-14-G-T
2	Connector	Header, 100 dual str, 2 x 4	Positions W10 to W13, Positions W6 to W9	Sullins	S2011E-04-ND
3	Resistor	1.0 k Ω , 1/16 W, 1%, 0603	R1, R3, R4	Panasonic	ERJ-3EKF1001V
31	Resistor	0 Ω , 5%, 1/10 W, 0603	R2, R5, R6, R7, R8, R9, R11, R12, R14, R15, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R38, R51, R56, R57, R58, R59, R60, R61, R62, R63, R64	Panasonic	ERJ-2GE0R00X
4	Resistor	787 Ω , 1%, 1/16 W, 0603	R10, R13, R16, R42	Panasonic	ERJ-3EKF7870V
1	Resistor	100 Ω , 1%, 1/16 W, 0603	R27	Panasonic	ERJ-3EKF1000V
1	Resistor	3.48 k Ω , 1%, 1/16 W, 0603	R28	Panasonic	ERJ-3EKF3.48K
1	Resistor	1.5 k Ω , 1%, 1/16 W, 0603	R37	Panasonic	ERJ-3EKF1501V

Qty	Name	Description	Reference Designator	Manufacturer	Part Number
1	Resistor	10 k Ω , 1%, 1/16 W, 0603	R39	Panasonic	ERJ-3EKF1002V
2	Resistor	100 k Ω , 1%, 1/16 W, 0603	R40, R41	Panasonic	ERJ-3EKF1003V
8	Resistor	20.0 Ω , 1%, 1/16 W, 0603	R43, R44, R45, R46, R47, R48, R49, R50	Panasonic	ERJ-3EKF20R0V
2	Resistor	22.1 k Ω , 1%, 1/16 W, 0603	R52, R53	Panasonic	ERJ-3EKF2212V
1	Resistor	49.9 Ω , 1%, 1/16 W	R54	Panasonic	ERJ-3EKF49R9V
1	Resistor	499 Ω , 1%, 1/16 W, 0603	R55	Panasonic	ERJ-3EKF4990V
4	Resistor	274 Ω , 1%, 1/16 W, 0603	RFB1, RFB2, RFB3, RFB4	Panasonic	ERJ-3EKF2740V
1	Integrated Circuit	Quad VGA	U1	Analog Devices	AD8334ACPZ-REEL7
1	Integrated Circuit	MCU USB peripheral, high speed, 56 QFN	U2	Cypress	CY7C68013A-56LFXC
4	Integrated Circuit	Amplifier	U3, U4, U5, U6	Analog Devices	AD8021ARZ
1	Integrated Circuit	LVDS driver	U7	National Semiconductor	DS90C401M
1	Test Loop	Orange	VAS	Components Corp.	TP-104-01-03
1	Crystal	24.00 MHz, 12 pF, HC-49/US	Y1	ECS Inc.	ECS-240-12-4X
1	Integrated Circuit	EEPROM	Z1	Microchip Technology	24LC00/P

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

Figure 68. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 6 mm × 6 mm Body, Very Thin Quad
 (CP-40-1)
 Dimensions shown in millimeters

101306-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8339ACPZ ¹	-40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
AD8339ACPZ-R7 ¹	-40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
AD8339ACPZ-RL ¹	-40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
AD8339-EVALZ ¹		Evaluation Board	

¹ Z = RoHS Compliant Part.