- **Excellent-Price/Performance Floating-Point Digital Signal Processor (DSP): TMS320C6711D**
  - **Eight 32-Bit Instructions/Cycle**
  - **167-, 200-, 250-MHz Clock Rates**
  - **6-, 5-, 4-ns Instruction Cycle Time**
  - **1000, 1200, 1500 MFLOPS**
- **Advanced Very Long Instruction Word (VLIW) C67x™ DSP Core**
  - **Eight Highly Independent Functional Units:**
    - **Four ALUs (Floating- and Fixed-Point)**
    - **Two ALUs (Fixed-Point)**
    - **Two Multipliers (Floating- and Fixed-Point)**
  - **Load-Store Architecture With 32 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Hardware Support for IEEE Single-Precision and Double-Precision Instructions**
  - **Byte-Addressable (8-, 16-, 32-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Saturation**
  - **Bit-Field Extract, Set, Clear**
  - **Bit-Counting**
  - **Normalization**
- **L1/L2 Memory Architecture**
  - **32K-Bit (4K-Byte) L1P Program Cache (Direct Mapped)**
  - **32K-Bit (4K-Byte) L1D Data Cache (2-Way Set-Associative)**
  - **512K-Bit (64K-Byte) L2 Unified Mapped RAM/Cache (Flexible Data/Program Allocation)**
- **Device Configuration**
  - **Boot Mode: HPI, 8-, 16-, 32-Bit ROM Boot**
  - **Endianness: Little Endian, Big Endian**
- **Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)**
- **32-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to Asynchronous Memories: SRAM and EPROM**
  - **Glueless Interface to Synchronous Memories: SDRAM and SBSRAM**
  - **256M-Byte Total Addressable External Memory Space**
- **16-Bit Host-Port Interface (HPI)**
- **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Direct Interface to T1/E1, MVIP, SCSA Framers**
  - **ST-Bus-Switching Compatible**
  - **Up to 256 Channels Each**
  - **AC97-Compatible**
  - **Serial-Peripheral-Interface (SPI) Compatible (Motorola™)**
- **Two 32-Bit General-Purpose Timers**
- **Flexible Software Configurable PLL-Based Clock Generator Module**
- **A Dedicated General-Purpose Input/Output (GPIO) Module With 5 Pins**
- **IEEE-1149.1 (JTAG†) Boundary-Scan-Compatible**
- **272-Pin Ball Grid Array (BGA) Package (GDP and ZDP Suffixes)**
- **CMOS Technology**
  - **0.13-μm/6-Level Copper Metal Process**
- **3.3-V I/O, 1.4-V Internal (−250)**
- **3.3-V I/O, 1.20-V Internal ‡**

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.
‡ These values are compatible with existing 1.26V designs.

Table of Contents

REVISION HISTORY

The TMS320C67**11D** device-specific documentation has been split from *TMS320C6711, TMS320C6711B*, *TMS320C6711C, TMS320C6711D Floating−Point Digital Signal Processors*, literature number SPRS088N, into a separate Data Sheet, literature number SPRS292. It also highlights technical changes made to SPRS292 to generate SPRS292A. These changes are marked by "**[Revision A]**." **Additionally**, made changes to SPRS292A to generate SPRS292B. These changes are marked by **"[Revision B]."** Both Revision A and B changes are noted in the Revision History table below.

Scope: Updated information on McBSP and JTAG for clarification. Changed Pin Description for A12 and B11 (Revisions SPRS292 and SPRS292A). Updated Nomenclature figure by adding device−specific information for the ZDP package. Updated Characteristics of the Processor table with device−specific information (footnote) for the ZDP package

TI Recommends for *new designs* that the following pins be configured as such:

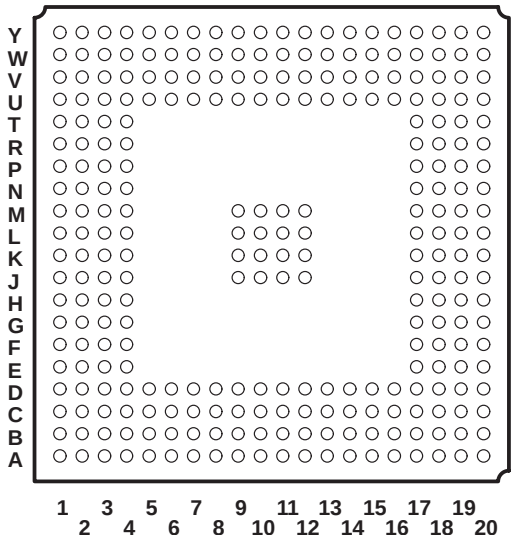
- Pin A12 connected directly to CV_{DD} (core power)
- Pin B11 connected directly to V_{SS} (ground)

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
21	Device Configurations, device configurations at device reset: Updated "For proper device operation..." paragraph **[Revision B]**
22	Device Configurations, Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12, and CLKMODE0) section: Removed "CE1 width 32−bit" from Functional Description for "**00**" in HD[4:3](BOOTMODE) Configuration Pin
22	Device Configurations, Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12, and CLKMODE0) section: Updated "All other HD pins..." footnote **[Revision B]**
26	Terminal Functions, Resets and Interrupts section: Updated IPU/IPD for RESET Signal Name ***from*** "IPU" ***to*** "−−"
27	Terminal Functions, Host Port Interface, Description section: Updated "Other HD pins..." paragraph **[Revision B]**
27	Terminal Functions, Host Port Interface section: Removed "CE1 width 32−bit" from Description for "**00**" in Bootmode HD[4:3]
32	Terminal Functions, Reserved for Test section: Updated Description for RSV Signal Name, A12 GDP/ZDP Updated Description for RSV Signal Name, B11 GDP/ZDP
32	Terminal Functions, Reserved for Test section: Updated/changed Description for RSV Signal Name, A12 GDP (to ***"recommended"***) − **[Revision A]** Updated/changed Description for RSV Signal Name, B11 GDP (to ***"recommended"***) **− [Revision A]**
39	Device Support, device and development-support tool nomenclature: Updated figure for clarity
40	Device Support, documentation support section: Updated paragraphs for clarity
55	Power−Down Mode Logic − Triggering, Wake−up and Effects section: Updated paragraphs **[Revision B]**
57	Power−Down Mode Logic − Triggering, Wake−up and Effects section, Characteristics of the Power-Down Modes table: Added "It is recommended to use the PLLPWDN bit (PLLCSR.1) as an alternative to PD3" to PRWD Field (BITS 15−10) − 011100 − Effect on Chip's Operation **[Revision B]**

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
57	Power−Down Mode Logic − Triggering, Wake−up and Effects section, Characteristics of the Power-Down Modes table: Deleted three paragraphs following table **[Revision B]**
59	IEEE 1149.1 JTAG Compatibility Statement section: Updated/added paragraphs for clarity
60	EMIF Device Speed section, Example Boards and Maximum EMIF Speed table: Type − 3−Loads Short Traces, EMIF Interface Components section: Updated ***from*** “32−Bit SDRAMs” ***to*** “16−Bit SDRAMs” **[Revision B]**
63	Recommended Operating Conditions: Added $V_{OS,}$ Maximum voltage during overshoot row and associated footnote Added $V_{US,}$ Maximum voltage during undershoot row and associated footnote
66	Parameter Measurement Information: AC transient rise/fall time specifications section: Added AC Transient Specification Rise Time figure Added AC Transient Specification Fall Time figure
94	MULTICHANNEL BUFFERED SERIAL PORT TIMING: switching characteristics over recommended operating conditions for McBSP section: Updated McBSP Timings figure for clarification

GDP and ZDP BGA packages (bottom view)

GDP and ZDP 272-PIN BALL GRID ARRAY (BGA) PACKAGES†
(BOTTOM VIEW)



† The ZDP mechanical package designator represents the version of the GDP package with lead−free balls. For more detailed information, see the *Mechanical Data* section of this document.

description

The TMS320C67x™ DSPs (including the TMS320C6711, TMS320C6711B, TMS320C6711C, TMS320C6711D devices†) compose the floating-point DSP family in the TMS320C6000™ DSP platform. The C6711, C6711B, C6711C, and C6711D devices are based on the high-performance, advanced very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for multichannel and multifunction applications.

With performance of up to 1200 million floating-point operations per second (MFLOPS) at a clock rate of 200 MHz or up to 1500 MFLOPS at a clock rate of 250 MHz, the C6711D device also offers cost-effective solutions to high-performance DSP programming challenges. The C6711D DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide four floating-/fixed-point ALUs, two fixed-point ALUs, and two floating-/fixed-point multipliers. The C6711D can produce two MACs per cycle for a total of 400 MMACS.

The C6711D DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6711D device uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 32-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 32-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 512-Kbit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM and asynchronous peripherals.

The C6711D has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

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† Throughout the remainder of this document, the TMS320C6711D shall be referred to as its individual full device part number or abbreviated as C6711D or 11D.

device characteristics

Table 1 provides an overview of the C6711D DSP. The table shows significant features of the device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count. For more details on the C6000™ DSP device part numbers and part numbering, see Figure 5.

Table 1. Characteristics of the C6711D Processor

HARDWARE FEATURES		INTERNAL CLOCK SOURCE	C6711D FLOATING-POINT DSP
Peripherals	EMIF	ECLKIN	
		SYSCLK3 or ECLKIN	1
	EDMA	CPU clock frequency	1
	HPI	CPU/2 clock frequency	
		SYSCLK2	1
	McBSPs	CPU/2 clock frequency	
		SYSCLK2	2
	32-Bit Timers	CPU/4 clock frequency	—
		1/2 of SYSCLK2	2
	GPIO Module	SYSCLK2	1
On-Chip Memory	Size (Bytes)		72K
	Organization		4K-Byte (4KB) L1 Program (L1P) Cache 4KB L1 Data (L1D) Cache 64KB Unified Mapped RAM/Cache (L2)
CPU ID+ CPU Rev ID	Control Status Register (CSR.[31:16])		0x0203
Frequency	MHz		167, 200, 250
Cycle Time	ns		4 ns (C6711DGDP-250) 5 ns (C6711DGDP−200 and C6711DZDP−200) 6 ns (C6711DGDP**A**−167 and C6711DZDP**A**−167)
Voltage	Core (V)		1.20† 1.4 (−250)
	I/O (V)		3.3
PLL Options	CLKIN frequency multiplier		−
Clock Generator Options	Prescaler Multiplier Postscaler		/1, /2, /3, ..., /32 x4, x5, x6, ..., x25 /1, /2, /3, ..., /32
BGA Package	27 x 27 mm		272-Pin BGA (GDP and ZDP)§
Process Technology	µm		0.13 µm
Product Status Product Preview (PP) Advance Information (AI) Production Data (PD)			PD‡

† These values are compatible with existing 1.26−V designs.

‡ PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

§ The ZDP package devices are supported in the same speed grades as the GDP package devices (***available upon request***).

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device compatibility

The TMS320C6211/C6211B and C6711/C6711B devices are pin-compatible and have the same peripheral set; thus, making new system designs easier and providing faster time to market. The following list summarizes the device characteristic differences among the C6211, C6211B, C6711, C6711B, C6711C, and C6711D devices:

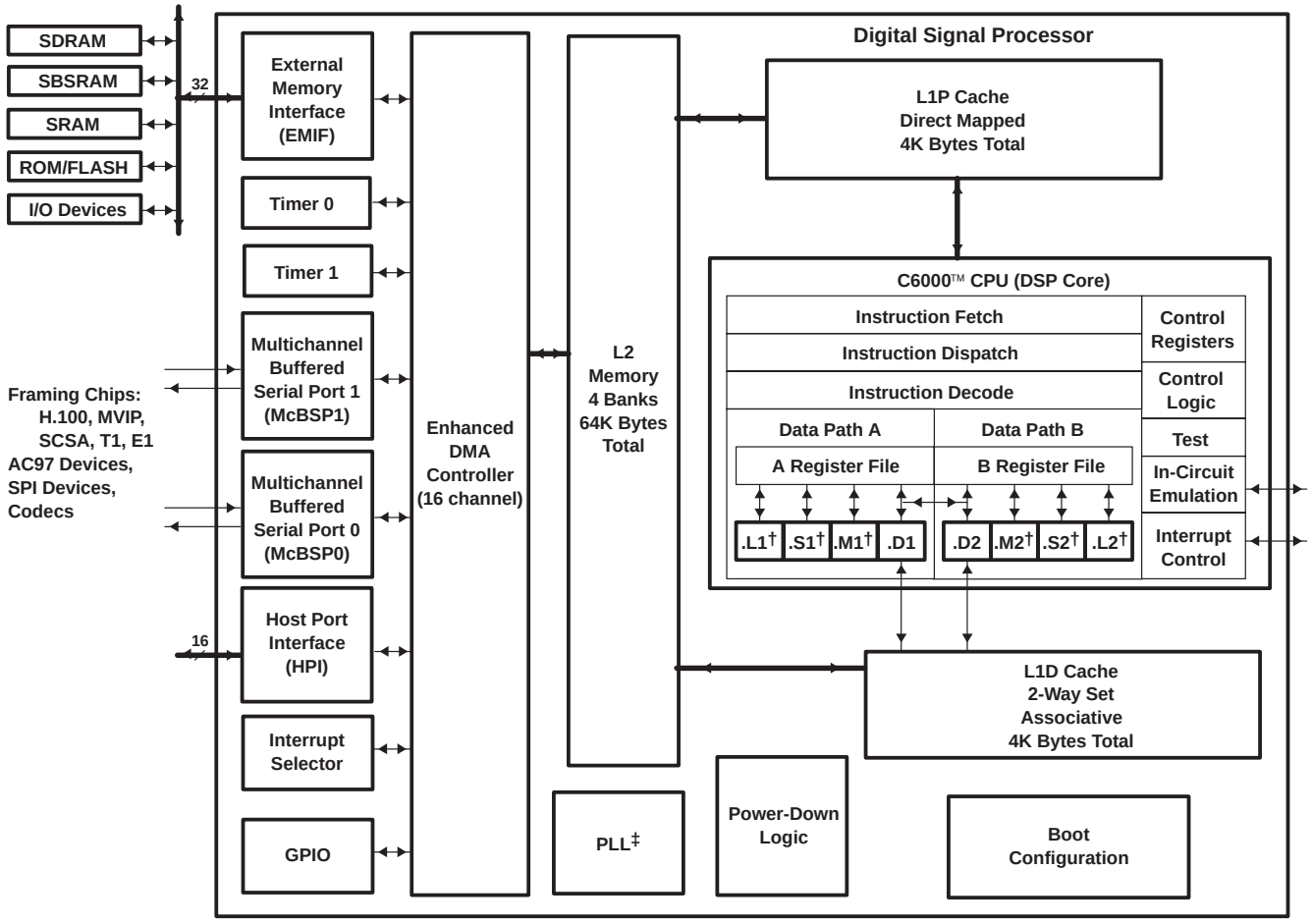
- The C6211 and C6211B devices have a fixed-point C62x CPU, while the C6711, C6711B, C6711C, and C6711D devices have a floating-point C67x CPU.
- The C6211/C6211B device runs at -167 and -150 MHz clock speeds (with a C6211BGFNA extended temperature device that also runs at -150 MHz), while the C6711/C6711B device runs at -150 and -100 MHz (with a C6711BGFNA extended temperature device that also runs at -100 MHz) and the C6711C and C6711D devices run at -200 clock speed (with a C6711CGDPA and C6711DGDPA extended temperature devices that also run at -167 MHz).
- The C6211/C6211B, C6711-100, and C6711B devices have a core voltage of 1.8 V, the C6711-150 device core voltage is 1.9 V, and the C6711C and C6711D devices operate with a core voltage of 1.20† V.
- There are several enhancements and features that are only available on the C6711C and C6711D devices, such as: the CLKOUT3 signal, a software programmable PLL and PLL Controller, and a GPIO peripheral module. The C6711D device also has additional enhancements such as: EMIF Big Endian mode correctness $\overline{\text{EMIFBE}}$ and the L1D requestor priority to L2 bit [“P” bit] in the cache configuration (CCFG) register.

For more detailed discussion on the migration of a C6211, C6211B, C6711, C6711B device to a TMS320C6711C device, see the *Migrating from TMS320C6211B/6711B to TMS320C6711C* application report (literature number SPRA837).

For a more detailed discussion on the similarities/differences between the C6211 and C6711 devices, see the *How to Begin Development Today with the TMS320C6211 DSP* and *How to Begin Development with the TMS320C6711 DSP* application reports (literature number SPRA474 and SPRA522, respectively).

† This value is compatible with existing 1.26V designs.

functional block and CPU (DSP core) diagram



† In addition to fixed-point instructions, these functional units execute floating-point instructions.
‡ The device has a software-configurable PLL (with x4 through x25 multiplier and /1 through /32 divider).

CPU (DSP core) description

The CPU fetches advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

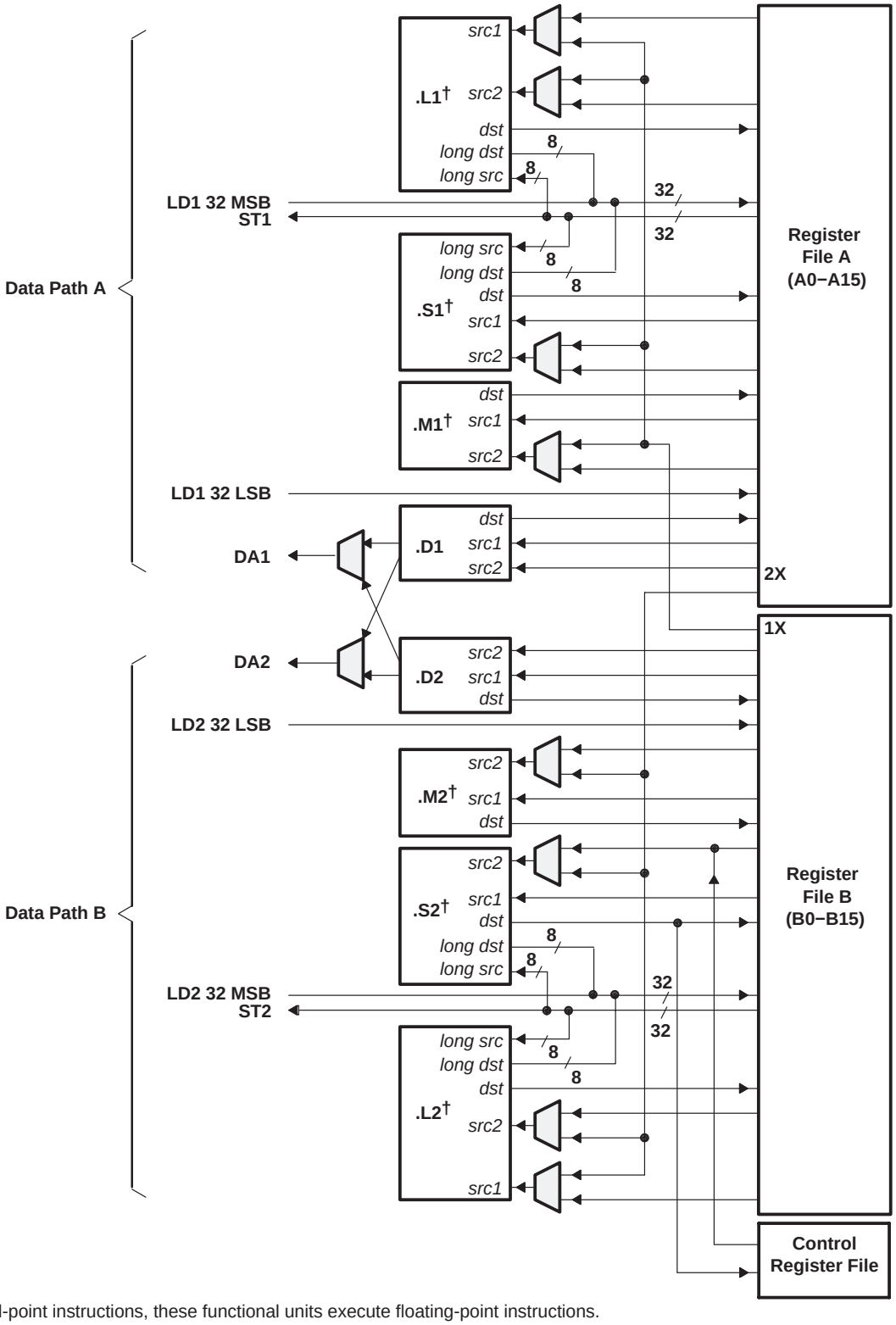
The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU (see the functional block and CPU diagram and Figure 1). The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all C62x instructions. In addition to C62x fixed-point instructions, the six out of eight functional units (.L1, .S1, .M1, .M2, .S2, and .L2) also execute floating-point instructions. The remaining two functional units (.D1 and .D2) also execute the new LDDW instruction which loads 64 bits per CPU side for a total of 128 bits per cycle.

Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically “true”). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

CPU (DSP core) description (continued)



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 1. TMS320C67x™ CPU (DSP Core) Data Paths

memory map summary

Table 2 shows the memory map address ranges of the device. Internal memory is always located at address 0 and can be used as both program and data memory. The configuration registers for the common peripherals are located at the same hex address ranges. The external memory address ranges in the device begin at the address location 0x8000 0000.

Table 2. TMS320C6711D Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Internal RAM (L2)	64K	0000 0000 – 0000 FFFF
Reserved	24M – 64K	0001 0000 – 017F FFFF
External Memory Interface (EMIF) Registers	256K	0180 0000 – 0183 FFFF
L2 Registers	256K	0184 0000 – 0187 FFFF
HPI Registers	256K	0188 0000 – 018B FFFF
McBSP 0 Registers	256K	018C 0000 – 018F FFFF
McBSP 1 Registers	256K	0190 0000 – 0193 FFFF
Timer 0 Registers	256K	0194 0000 – 0197 FFFF
Timer 1 Registers	256K	0198 0000 – 019B FFFF
Interrupt Selector Registers	512	019C 0000 – 019C 01FF
Device Configuration Registers	4	019C 0200 – 019C 0203
Reserved	256K − 516	019C 0204 – 019F FFFF
EDMA RAM and EDMA Registers	256K	01A0 0000 – 01A3 FFFF
Reserved	768K	01A4 0000 – 01AF FFFF
GPIO Registers	16K	01B0 0000 – 01B0 3FFF
Reserved	480K	01B0 4000 – 01B7 BFFF
PLL Controller Registers	8K	01B7 C000 – 01B7 DFFF
Reserved	4M + 520K	01B7 E000 – 01FF FFFF
QDMA Registers	52	0200 0000 – 0200 0033
Reserved	736M – 52	0200 0034 – 2FFF FFFF
McBSP 0 Data/Peripheral Data Bus	64M	3000 0000 – 33FF FFFF
McBSP 1 Data/Peripheral Data Bus	64M	3400 0000 – 37FF FFFF
Reserved	64M	3800 0000 – 3BFF FFFF
Reserved	1G + 64M	3C00 0000 – 7FFF FFFF
EMIF CE0†	256M	8000 0000 – 8FFF FFFF
EMIF CE1†	256M	9000 0000 – 9FFF FFFF
EMIF CE2†	256M	A000 0000 – AFFF FFFF
EMIF CE3†	256M	B000 0000 – BFFF FFFF
Reserved	1G	C000 0000 – FFFF FFFF

† The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space. To get 256MB of addressable memory, additional general-purpose output pin or external logic is required.

peripheral register descriptions

Table 3 through Table 14 identify the peripheral registers for the device by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents, bit names, and their descriptions, see the specific peripheral reference guide listed in the *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190).

Table 3. EMIF Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	GBLCTL	EMIF global control
0180 0004	CECTL1	EMIF CE1 space control
0180 0008	CECTL0	EMIF CE0 space control
0180 000C	−	Reserved
0180 0010	CECTL2	EMIF CE2 space control
0180 0014	CECTL3	EMIF CE3 space control
0180 0018	SDCTL	EMIF SDRAM control
0180 001C	SDTIM	EMIF SDRAM refresh control
0180 0020	SDEXT	EMIF SDRAM extension
0180 0024 − 0183 FFFF	−	Reserved

Table 4. L2 Cache Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 0000	CCFG	Cache configuration register
0184 4000	L2WBAR	L2 writeback base address register
0184 4004	L2WWC	L2 writeback word count register
0184 4010	L2WIBAR	L2 writeback-invalidate base address register
0184 4014	L2WIWC	L2 writeback-invalidate word count register
0184 4020	L1PIBAR	L1P invalidate base address register
0184 4024	L1PIWC	L1P invalidate word count register
0184 4030	L1DWIBAR	L1D writeback-invalidate base address register
0184 4034	L1DWIWC	L1D writeback-invalidate word count register
0184 5000	L2WB	L2 writeback all register
0184 5004	L2WBINV	L2 writeback-invalidate all register
0184 8200	MAR0	Controls CE0 range 8000 0000 − 80FF FFFF
0184 8204	MAR1	Controls CE0 range 8100 0000 − 81FF FFFF
0184 8208	MAR2	Controls CE0 range 8200 0000 − 82FF FFFF
0184 820C	MAR3	Controls CE0 range 8300 0000 − 83FF FFFF
0184 8240	MAR4	Controls CE1 range 9000 0000 − 90FF FFFF
0184 8244	MAR5	Controls CE1 range 9100 0000 − 91FF FFFF
0184 8248	MAR6	Controls CE1 range 9200 0000 − 92FF FFFF
0184 824C	MAR7	Controls CE1 range 9300 0000 − 93FF FFFF
0184 8280	MAR8	Controls CE2 range A000 0000 − A0FF FFFF
0184 8284	MAR9	Controls CE2 range A100 0000 − A1FF FFFF
0184 8288	MAR10	Controls CE2 range A200 0000 − A2FF FFFF
0184 828C	MAR11	Controls CE2 range A300 0000 − A3FF FFFF
0184 82C0	MAR12	Controls CE3 range B000 0000 − B0FF FFFF
0184 82C4	MAR13	Controls CE3 range B100 0000 − B1FF FFFF
0184 82C8	MAR14	Controls CE3 range B200 0000 − B2FF FFFF
0184 82CC	MAR15	Controls CE3 range B300 0000 − B3FF FFFF
0184 82D0 − 0187 FFFF	−	Reserved

peripheral register descriptions (continued)

Table 5. Interrupt Selector Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
019C 0000	MUXH	Interrupt multiplexer high	Selects which interrupts drive CPU interrupts 10−15 (INT10−INT15)
019C 0004	MUXL	Interrupt multiplexer low	Selects which interrupts drive CPU interrupts 4−9 (INT04−INT09)
019C 0008	EXTPOL	External interrupt polarity	Sets the polarity of the external interrupts (EXT_INT4−EXT_INT7)
019C 000C − 019F FFFF	−	Reserved	

Table 6. Device Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER DESCRIPTION	
019C 0200	DEVCFG	Device Configuration	This register allows the user control of the EMIF input clock source. For more detailed information on the device configuration register, see the Device Configurations section of this data sheet.
019C 0204 − 019F FFFF	−	Reserved	
N/A	CSR	CPU Control Status Register	Identifies which CPU and defines the silicon revision of the CPU. This register also offers the user control of device operation. For more detailed information on the CPU Control Status Register, see the CPU CSR Register Description section of this data sheet.

Table 7. EDMA Parameter RAM†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0000 − 01A0 0017	−	Parameters for Event 0 (6 words) or Reload/Link Parameters for other Event
01A0 0018 − 01A0 002F	−	Parameters for Event 1 (6 words) or Reload/Link Parameters for other Event
01A0 0030 − 01A0 0047	−	Parameters for Event 2 (6 words) or Reload/Link Parameters for other Event
01A0 0048 − 01A0 005F	−	Parameters for Event 3 (6 words) or Reload/Link Parameters for other Event
01A0 0060 − 01A0 0077	−	Parameters for Event 4 (6 words) or Reload/Link Parameters for other Event
01A0 0078 − 01A0 008F	−	Parameters for Event 5 (6 words) or Reload/Link Parameters for other Event
01A0 0090 − 01A0 00A7	−	Parameters for Event 6 (6 words) or Reload/Link Parameters for other Event
01A0 00A8 − 01A0 00BF	−	Parameters for Event 7 (6 words) or Reload/Link Parameters for other Event
01A0 00C0 − 01A0 00D7	−	Parameters for Event 8 (6 words) or Reload/Link Parameters for other Event
01A0 00D8 − 01A0 00EF	−	Parameters for Event 9 (6 words) or Reload/Link Parameters for other Event
01A0 00F0 − 01A0 00107	−	Parameters for Event 10 (6 words) or Reload/Link Parameters for other Event
01A0 0108 − 01A0 011F	−	Parameters for Event 11 (6 words) or Reload/Link Parameters for other Event
01A0 0120 − 01A0 0137	−	Parameters for Event 12 (6 words) or Reload/Link Parameters for other Event
01A0 0138 − 01A0 014F	−	Parameters for Event 13 (6 words) or Reload/Link Parameters for other Event
01A0 0150 − 01A0 0167	−	Parameters for Event 14 (6 words) or Reload/Link Parameters for other Event
01A0 0168 − 01A0 017F	−	Parameters for Event 15 (6 words) or Reload/Link Parameters for other Event
01A0 0180 − 01A0 0197	−	Reload/link parameters for Event 0−15
01A0 0198 − 01A0 01AF	−	Reload/link parameters for Event 0−15
...		...
01A0 07E0 − 01A0 07F7	−	Reload/link parameters for Event 0−15
01A0 07F8 − 01A0 07FF	−	Scratch pad area (2 words)

† The device has 85 EDMA parameters total: 16 Event/Reload parameters and 69 Reload-only parameters.

peripheral register descriptions (continued)

For more details on the EDMA parameter RAM 6-word parameter entry structure, see Figure 2.

	31	0	EDMA Parameter
Word 0	EDMA Channel Options Parameter (OPT)		OPT
Word 1	EDMA Channel Source Address (SRC)		SRC
Word 2	Array/Frame Count (FRMCNT)	Element Count (ELECNT)	CNT
Word 3	EDMA Channel Destination Address (DST)		DST
Word 4	Array/Frame Index (FRMIDX)	Element Index (ELEIDX)	IDX
Word 5	Element Count Reload (ELERLD)	Link Address (LINK)	RLD

Figure 2. EDMA Channel Parameter Entries (6 Words) for Each EDMA Event

Table 8. EDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0800 − 01A0 FEFC	−	Reserved
01A0 FF00	ESEL0	EDMA event selector 0
01A0 FF04	ESEL1	EDMA event selector 1
01A0 FF08 − 01A0 FF0B	−	Reserved
01A0 FF0C	ESEL3	EDMA event selector 3
01A0 FF1F − 01A0 FFDC	−	Reserved
01A0 FFE0	PQSR	Priority queue status register
01A0 FFE4	CIPR	Channel interrupt pending register
01A0 FFE8	CIER	Channel interrupt enable register
01A0 FFEC	CCER	Channel chain enable register
01A0 FFF0	ER	Event register
01A0 FFF4	EER	Event enable register
01A0 FFF8	ECR	Event clear register
01A0 FFFC	ESR	Event set register
01A1 0000 − 01A3 FFFF	–	Reserved

Table 9. Quick DMA (QDMA) and Pseudo Registers†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0200 0000	QOPT	QDMA options parameter register
0200 0004	QSRC	QDMA source address register
0200 0008	QCNT	QDMA frame count register
0200 000C	QDST	QDMA destination address register
0200 0010	QIDX	QDMA index register
0200 0014 − 0200 001C	−	Reserved
0200 0020	QSOPT	QDMA pseudo options register
0200 0024	QSSRC	QDMA pseudo source address register
0200 0028	QSCNT	QDMA pseudo frame count register
0200 002C	QSDST	QDMA pseudo destination address register
0200 0030	QSIDX	QDMA pseudo index register

† All the QDMA and Pseudo registers are write-accessible only

peripheral register descriptions (continued)

Table 10. PLL Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B7 C000	PLLPID	Peripheral identification register (PID) [0x00010801 for PLL Controller]
01B7 C004 − 01B7 C0FF	−	Reserved
01B7 C100	PLLCSR	PLL control/status register
01B7 C104 − 01B7 C10F	−	Reserved
01B7 C110	PLLM	PLL multiplier control register
01B7 C114	PLLDIV0	PLL controller divider 0 register
01B7 C118	PLLDIV1	PLL controller divider 1 register
01B7 C11C	PLLDIV2	PLL controller divider 2 register
01B7 C120	PLLDIV3	PLL controller divider 3 register
01B7 C124	OSCDIV1	Oscillator divider 1 register
01B7 C128 − 01B7 DFFF	−	Reserved

Table 11. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B0 0000	GPEN	GPIO enable register
01B0 0004	GPDIR	GPIO direction register
01B0 0008	GPVAL	GPIO value register
01B0 000C	−	Reserved
01B0 0010	GPDH	GPIO delta high register
01B0 0014	GPHM	GPIO high mask register
01B0 0018	GPDL	GPIO delta low register
01B0 001C	GPLM	GPIO low mask register
01B0 0020	GPGC	GPIO global control register
01B0 0024	GPPOL	GPIO interrupt polarity register
01B0 0028 − 01B0 3FFF	−	Reserved

Table 12. HPI Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
−	HPID	HPI data register	Host read/write access only
−	HPIA	HPI address register	Host read/write access only
0188 0000	HPIC	HPI control register	Both Host/CPU read/write access
0188 0001 − 018B FFFF	−	Reserved	

peripheral register descriptions (continued)

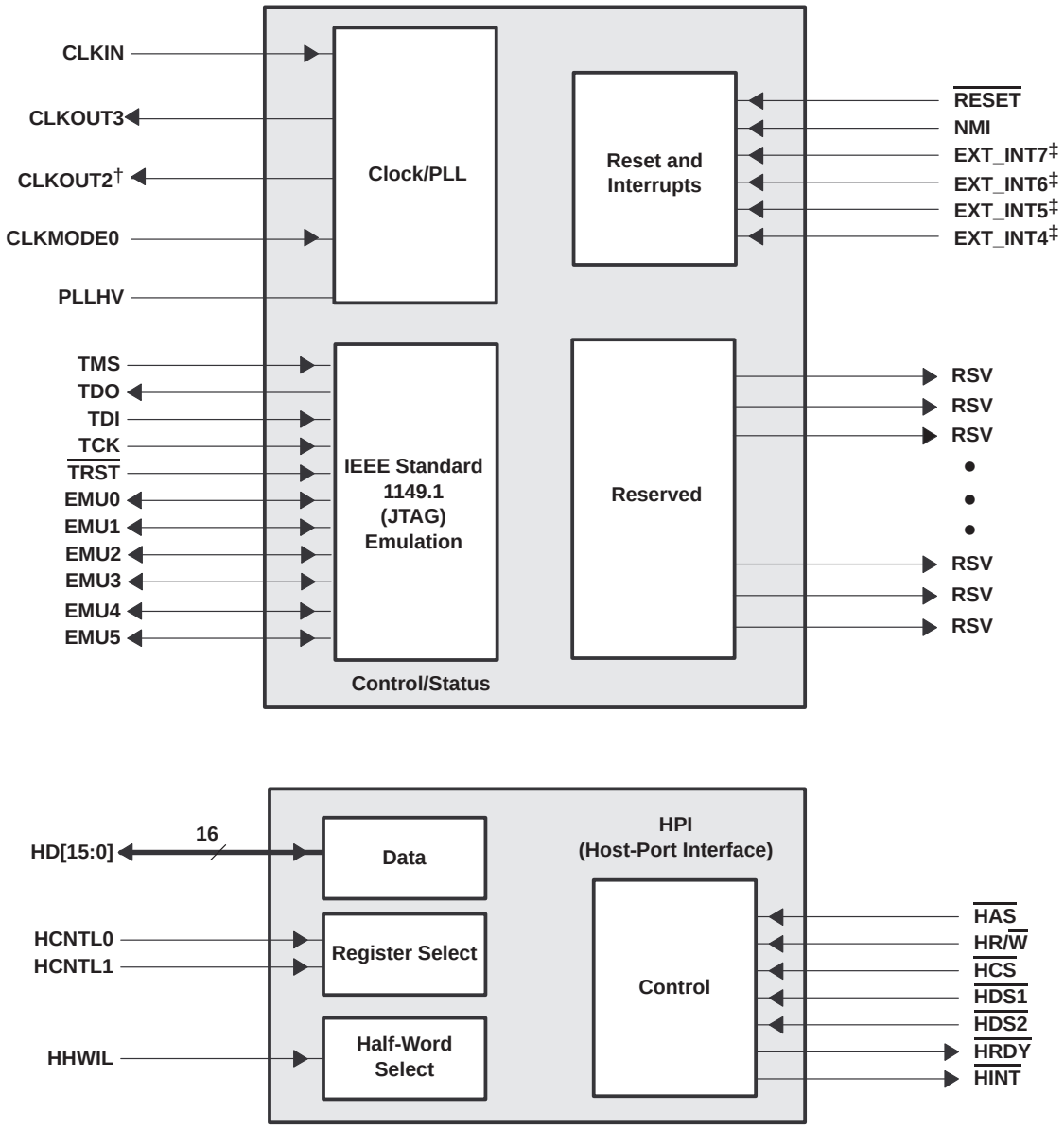
Table 13. Timer 0 and Timer 1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME	COMMENTS
TIMER 0	TIMER 1			
0194 0000	0198 0000	CTLx	Timer x control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0194 0004	0198 0004	PRDx	Timer x period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0194 0008	0198 0008	CNTx	Timer x counter register	Contains the current value of the incrementing counter.
0194 000C − 0197 FFFF	0198 000C − 019B FFFF	−	Reserved	−

Table 14. McBSP0 and McBSP1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER DESCRIPTION
McBSP0	McBSP1		
018C 0000	0190 0000	DRRx	McBSPx data receive register via Configuration Bus The CPU and EDMA controller can only read this register; they cannot write to it.
3000 0000 − 33FF FFFF	3400 0000 − 37FF FFFF	DRRx	McBSPx data receive register via Peripheral Data Bus
018C 0004	0190 0004	DXRx	McBSPx data transmit register via Configuration Bus
3000 0000 − 33FF FFFF	3400 0000 − 37FF FFFF	DXRx	McBSPx data transmit register via Peripheral Data Bus
018C 0008	0190 0008	SPCRx	McBSPx serial port control register
018C 000C	0190 000C	RCRx	McBSPx receive control register
018C 0010	0190 0010	XCRx	McBSPx transmit control register
018C 0014	0190 0014	SRGRx	McBSPx sample rate generator register
018C 0018	0190 0018	MCRx	McBSPx multichannel control register
018C 001C	0190 001C	RCERx	McBSPx receive channel enable register
018C 0020	0190 0020	XCERx	McBSPx transmit channel enable register
018C 0024	0190 0024	PCRx	McBSPx pin control register
018C 0028 − 018F FFFF	0190 0028 − 0193 FFFF	−	Reserved

signal groups description

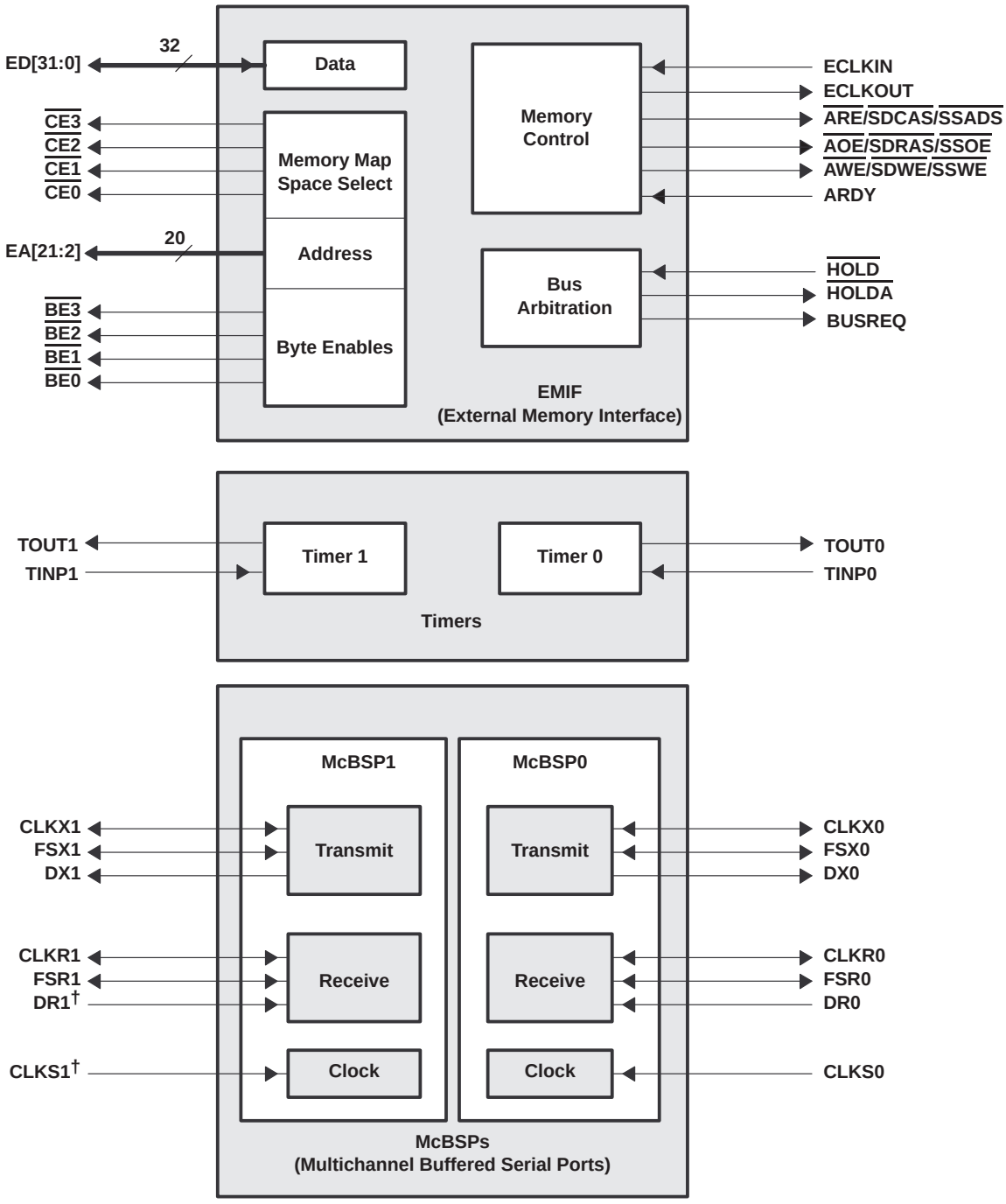


† For this device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Default function is CLKOUT2. To use this pin as GPIO, the GP2EN bit in the GPEN register and the GP2DIR bit in the GPDIR register must be properly configured.

‡ For this device, the external interrupts (EXT_INT[7−4]) go through the general-purpose input/output (GPIO) module. When used as interrupt inputs, the GP[7−4] pins must be configured as inputs (via the GPDIR register) and enabled (via the GPEN register) in addition to enabling the interrupts in the interrupt enable register (IER).

Figure 3. CPU (DSP Core) and Peripheral Signals

signal groups description (continued)



† For proper device operation, these pins must be externally pulled up with a 10-kΩ resistor.

Figure 4. Peripheral Signals

signal groups description (continued)

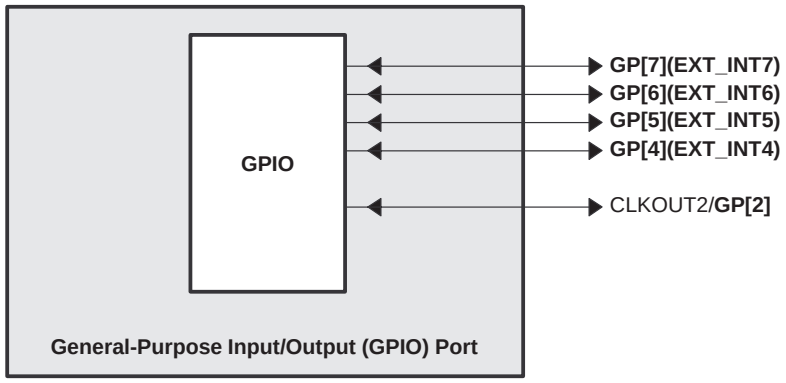


Figure 4. Peripheral Signals (Continued)

DEVICE CONFIGURATIONS

On this device, bootmode and certain device configurations/peripheral selections are determined at device reset. Also, other device configurations (e.g., EMIF input clock source) are software-configurable via the device configurations register (DEVCFG) [address location 0x019C0200] after device reset.

device configurations at device reset

Table 15 describes the C6711D device configuration pins, which are set up via internal or external pullup/pulldown resistors through the HPI data pins (HD[4:3], HD8, HD12) and CLKMODE0 pin. These configuration pins must be in the desired state until reset is released.

For proper device operation, ***do not*** oppose the HD [14, 13, 11:9, 7, 1, 0] pins with external pull−ups/pulldowns at reset.

For more details on these device configuration pins, see the Terminal Functions table of this data sheet.

Table 15. Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12, and CLKMODE0)†

CONFIGURATION PIN	GDP/ZDP	FUNCTIONAL DESCRIPTION
HD12‡	C15	EMIF Big Endian mode correctness ($\overline{\text{EMIFBE}}$) 0 – The EMIF data will always be presented on the ED[7:0] side of the bus, regardless of the endianess mode (Little/Big Endian). 1 − In Little Endian mode (HD8 =1), the 8-bit or 16-bit EMIF data will be present on the ED[7:0] side of the bus. In Big Endian mode (HD8 =0), the 8-bit or 16-bit EMIF data will be present on the ED[31:24] side of the bus [default]. EMIF Big Endian mode correctness is ***not*** supported on the C6711/11B/11C device. This new functionality does *not* affect systems using the current default value of HD12=1. For more detailed information on the big endian mode correctness, see the *EMIF Big Endian Mode Correctness* portion of this data sheet.
HD8‡	B17	Device Endian mode (LEND) 0 – System operates in Big Endian mode 1 − System operates in Little Endian mode (default)
HD[4:3] (BOOTMODE)‡	C19, C20	Bootmode Configuration Pins (BOOTMODE) 00 – $\overline{\text{HPI}}$ boot/Emulation boot 01 – $\overline{\text{CE1}}$ width 8-bit, Asynchronous external ROM boot with default $\overline{\text{timing}}$s (default mode) 10 − $\overline{\text{CE1}}$ width 16-bit, Asynchronous external ROM boot with default $\overline{\text{timing}}$s 11 − $\overline{\text{CE1}}$ width 32-bit, Asynchronous external ROM boot with default timings For more detailed information on these bootmode configurations, see the *bootmode* section of this data sheet.
CLKMODE0	C4	Clock generator input clock source select 0 – Reserved. Do not use. 1 − CLKIN square wave [default] For proper device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor.

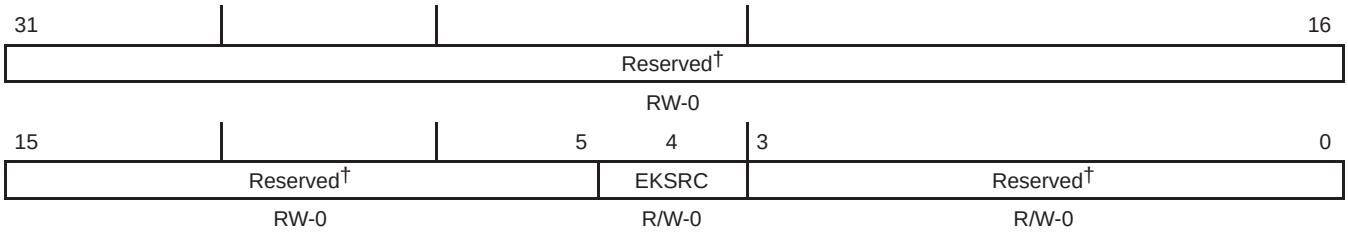
† All other HD pins *or* HD [15:13, 11:9, 7:5, 2:0] have pullups/pulldowns (IPUs or IPDs). For proper device operation, ***do not*** oppose the HD [14, 13, 11:9, 7, 1, 0] pins with external pull−ups/pulldowns at reset; however, the HD[15, 6, 5, 2] pins *can* be opposed and driven during reset.
‡ To ensure a proper logic level during reset when these pins are ***both*** routed out ***and*** 3−stated or not driven, it is recommended an external 10-kΩ pullup/pulldown resistor be included to sustain the IPU/IPD, respectively.

DEVICE CONFIGURATIONS (CONTINUED)

DEVCFG register description

The device configuration register (DEVCFG) allows the user control of the EMIF input clock source for the device. For more detailed information on the DEVCFG register control bits, see Table 16 and Table 17.

Table 16. Device Configuration Register (DEVCFG) [Address location: 0x019C0200 − 0x019C02FF]



Legend: R/W = Read/Write; -n = value after reset

† ***Do not*** write non-zero values to these bit locations.

Table 17. Device Configuration (DEVCFG) Register Selection Bit Descriptions

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. ***Do not*** write non-zero values to these bit locations.
4	EKSRC	EMIF input clock source bit. Determines which clock signal is used as the EMIF input clock. 0 = SYSCLK3 (from the clock generator) is the EMIF input clock source (default) 1 = ECLKIN external pin is the EMIF input clock source
3:0	Reserved	Reserved. ***Do not*** write non-zero values to these bit locations.

TERMINAL FUNCTIONS

The terminal functions table identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, see the Device Configurations section of this data sheet.

Terminal Functions

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
CLOCK/PLL				
CLKIN	A3	I	IPD	Clock Input
CLKOUT2 (/GP0[2])	Y12	O/Z	IPD	For this device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Clock output at half of device speed (**O/Z**) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] (I/O/Z). When the CLKOUT2 pin is enabled, the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin (All devices). CLK2EN = 0: CLKOUT2 is disabled CLK2EN = 1: CLKOUT2 enabled to clock [default]
CLKOUT3	D10	O	IPD	Clock output programmable by OSCDIV1 register in the PLL controller.
CLKMODE0	C4	I	IPU	Clock generator input clock source select 0 − Reserved. Do not use. 1 − CLKIN square wave [default] For proper device operation, this pin must be either left unconnected or externally pulled up with a 1-kΩ resistor.
PLLHV	C5	A		Analog power (3.3 V) for PLL
JTAG EMULATION				
TMS	B7	I	IPU	JTAG test-port mode select
TDO	A8	O/Z	IPU	JTAG test-port data out
TDI	A7	I	IPU	JTAG test-port data in
TCK	A6	I	IPU	JTAG test-port clock
$\overline{\text{TRST}}$§	B6	I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the *IEEE 1149.1 JTAG Compatibility Statement* section of this data sheet.
EMU5	B12	I/O/Z	IPU	Emulation pin 5. Reserved for future use, leave unconnected.
EMU4	C11	I/O/Z	IPU	Emulation pin 4. Reserved for future use, leave unconnected.
EMU3	B10	I/O/Z	IPU	Emulation pin 3. Reserved for future use, leave unconnected.

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

§ To ensure a proper logic level during reset when these pins are ***both*** routed out ***and*** 3−stated or not driven, it is recommended an external 10-kΩ pullup/pulldown resistor be included to sustain the IPU/IPD, respectively.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
JTAG EMULATION (CONTINUED)				
EMU2	D3	I/O/Z	IPU	Emulation pin 2. Reserved for future use, leave unconnected.
EMU1 EMU0	B9 D9	I/O/Z	IPU	For Emulation and normal operation, no external pullup/pulldown resistors are necessary. However for the Boundary Scan operation, pull down the EMU1 and EMU0 pins with a dedicated 1-kΩ resistor. Emulation [1:0] pins. • Select the device functional mode of operation EMU[1:0] Operation 00 Boundary Scan/Functional Mode (see Note) 01 Reserved 10 Reserved 11 Emulation/Functional Mode [default] (see the *IEEE 1149.1 JTAG Compatibility Statement* section of this data sheet) The DSP can be placed in Functional mode when the EMU[1:0] pins are configured for either Boundary Scan or Emulation. Note: When the EMU[1:0] pins are configured for Boundary Scan mode, the internal pulldown (IPD) on the $\overline{\text{TRST}}$ signal must ***not*** be opposed in order to operate in Functional mode. For the Boundary Scan mode drive EMU[1:0] *and* $\overline{\text{RESET}}$ pins low.
RESETS AND INTERRUPTS				
$\overline{\text{RESET}}$	A13	I	−−	Device reset. When using Boundary Scan mode on the device, drive the EMU[1:0] *and* $\overline{\text{RESET}}$ pins low. This pin does ***not*** have an IPU on this device.
NMI	C13	I	IPD	Nonmaskable interrupt • Edge-driven (rising edge) Any noise on the NMI pin may trigger an NMI interrupt; therefore, if the NMI pin is not used, it is recommended that the NMI pin be grounded versus relying on the IPD.
EXT_INT7	E3	I	IPU	General-purpose input/output pins (**I/O/Z**) which also function as external interrupts • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]), in addition to the GPIO registers.
EXT_INT6	D2			
EXT_INT5	C1			
EXT_INT4	C2			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ZDP	TYPE†	IPD/IPU‡	DESCRIPTION
HOST-PORT INTERFACE (HPI)				
$\overline{\text{HINT}}$	J20	O	IPU	Host interrupt (from DSP to host)
HCNTL1	G19	I	IPU	Host control − selects between control, address, or data registers
HCNTL0	G18	I	IPU	Host control − selects between control, address, or data registers
HHWIL	H20	I	IPU	Host half-word select − first or second half-word (not necessarily high or low order)
HR/$\overline{\text{W}}$	G20	I	IPU	Host read or write select
HD15	B14	I/O/Z	IPU	Host-port data • Used for transfer of data, address, and control • Also controls initialization of DSP modes at reset via pullup/pulldown resistors − Device Endian mode (HD8) 0 − Big Endian 1 − Little Endian EMIF Big Endian mode correctness ($\overline{\text{EMIFBE}}$) (HD12) 0 − The EMIF data will always be presented on the ED[7:0] side of the bus, regardless of the endianess mode (Little/Big Endian). 1 − In Little Endian mode (HD8 =1), the 8-bit or 16-bit EMIF data will be present on the ED[7:0] side of the bus. In Big Endian mode (HD8 =0), the 8-bit or 16-bit EMIF data will be present on the ED[31:24] side of the bus [default]. This new functionality does *not* affect systems using the curent default value of HD12=1. For more detailed information on the big endian mode correctness, see the *EMIF Big Endian Mode Correctness* portion of this data sheet. − Bootmode (HD[4:3]) 00 − $\overline{\text{HPI}}$ boot/Emulation boot 01 − $\overline{\text{CE1}}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 − $\overline{\text{CE1}}$ width 16-bit, Asynchronous external ROM boot with default timings 11 − $\overline{\text{CE1}}$ width 32-bit, Asynchronous external ROM boot with default timings Other HD pins (HD [15:13, 11:9, 7:5, 2:0]) have pullups/pulldowns (IPUs/IPDs). For proper device operation, ***do not*** oppose the HD [14, 13, 11:9, 7, 1, 0] pins with external pull−ups/pull-downs at reset; however, the HD[15, 6, 5, 2] pins *can* be opposed and driven during reset. **For more details, see the Device Configurations section of this data sheet.**
HD14§	C14		IPU	
HD13§	A15		IPU	
HD12§	C15		IPU	
HD11	A16		IPU	
HD10	B16		IPU	
HD9	C16		IPU	
HD8§	B17		IPU	
HD7	A18		IPU	
HD6	C17		IPU	
HD5	B18		IPU	
HD4§	C19		IPD	
HD3§	C20		IPU	
HD2	D18		IPU	
HD1	D20		IPU	
HD0	E20		IPU	
$\overline{\text{HAS}}$	E18	I	IPU	Host address strobe
$\overline{\text{HCS}}$	F20	I	IPU	Host chip select
EMIF − CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY¶				
$\overline{\text{HDS1}}$	E19	I	IPU	Host data strobe 1
$\overline{\text{HDS2}}$	F18	I	IPU	Host data strobe 2

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

§ To ensure a proper logic level during reset when these pins are ***both*** routed out ***and*** 3−stated or not driven, it is recommended an external 10-kΩ pullup/pulldown resistor be included to sustain the IPU/IPD, respectively.

¶ To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF − CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY¶ (CONTINUED)				
$\overline{\text{HRDY}}$	H19	O	IPD	Host ready (from DSP to host)
$\overline{\text{CE3}}$	V6	O/Z	IPU	Memory space enables • Enabled by bits 28 through 31 of the word address • Only one asserted during any external data access
$\overline{\text{CE2}}$	W6	O/Z	IPU	
$\overline{\text{CE1}}$	W18	O/Z	IPU	
$\overline{\text{CE0}}$	V17	O/Z	IPU	
$\overline{\text{BE3}}$	V5	O/Z	IPU	Byte-enable control • Decoded from the two lowest bits of the internal address • Byte-write enables for most types of memory • Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{\text{BE2}}$	Y4	O/Z	IPU	
$\overline{\text{BE1}}$	U19	O/Z	IPU	
$\overline{\text{BE0}}$	V20	O/Z	IPU	
EMIF − BUS ARBITRATION¶				
$\overline{\text{HOLDA}}$	J18	O	IPU	Hold-request-acknowledge to the host
$\overline{\text{HOLD}}$	J17	I	IPU	Hold request from the host
BUSREQ	J19	O	IPU	Bus request output
EMIF − ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL¶				
ECLKIN	Y11	I	IPD	External EMIF input clock source
ECLKOUT	Y10	O/Z	IPD	EMIF output clock depends on the EKSRC bit (DEVCFG.[4]) and on EKEN bit (GBLCTL.[5]) EKSRC = 0 – ECLKOUT is based on the internal SYSCLK3 signal from the clock generator (default). EKSRC = 1 – ECLKOUT is based on the the external EMIF input clock source pin (ECLKIN) EKEN = 0 – ECLKOUT held low EKEN = 1 – ECLKOUT enabled to clock (default)
$\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/ $\overline{\text{SSADS}}$	V11	O/Z	IPU	Asynchronous memory read enable/SDRAM column-address strobe/SBSRAM address strobe
$\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/ $\overline{\text{SSOE}}$	W10	O/Z	IPU	Asynchronous memory output enable/SDRAM row-address strobe/SBSRAM output enable
$\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/ $\overline{\text{SSWE}}$	V12	O/Z	IPU	Asynchronous memory write enable/SDRAM write enable/SBSRAM write enable
ARDY	Y5	I	IPU	Asynchronous memory ready input

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]
¶ To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF − ADDRESS¶				
EA21	U18	O/Z	IPU	EMIF external address
EA20	Y18			
EA19	W17			
EA18	Y16			
EA17	V16			
EA16	Y15			
EA15	W15			
EA14	Y14			
EA13	W14			
EA12	V14			
EA11	W13			
EA10	V10			
EA9	Y9			
EA8	V9			
EA7	Y8			
EA6	W8			
EA5	V8			
EA4	W7			
EA3	V7			
EA2	Y6			
EMIF − DATA¶				
ED31	N3	I/O/Z	IPU	External data
ED30	P3			
ED29	P2			
ED28	P1			
ED27	R2			
ED26	R3			
ED25	T2			
ED24	T1			
ED23	U3			
ED22	U1			
ED21	U2			
ED20	V1			
ED19	V2			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

¶ To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF − DATA (CONTINUED)¶				
ED18	Y3	I/O/Z	IPU	External data
ED17	W4			
ED16	V4			
ED15	T19			
ED14	T20			
ED13	T18			
ED12	R20			
ED11	R19			
ED10	P20			
ED9	P18			
ED8	N20			
ED7	N19			
ED6	N18			
ED5	M20			
ED4	M19			
ED3	L19			
ED2	L18			
ED1	K19			
ED0	K18			
TIMER 1				
TOUT1	F1	O	IPD	Timer 1 or general-purpose output
TINP1	F2	I	IPD	Timer 1 or general-purpose input
TIMER 0				
TOUT0	G1	O	IPD	Timer 0 or general-purpose output
TINP0	G2	I	IPD	Timer 0 or general-purpose input
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)				
CLKS1	E1	I	IPD	External clock source (as opposed to internal) On the device, this pin does ***not*** have an internal pulldown (IPD). For proper device operation, the CLKS1 pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin.
CLKR1	M1	I/O/Z	IPD	Receive clock
CLKX1	L3	I/O/Z	IPD	Transmit clock

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]
¶ To maintain signal integrity for the EMIF signals, serial termination resistors should be inserted into all EMIF output signal lines.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1) (CONTINUED)				
DR1	M2	I	IPU	Receive data On this device, this pin does **not** have an internal pullup (IPU). For proper device operation, the DR1 pin should either be driven externally at all times or be pulled up with a 10-kΩ resistor to a valid logic level. Because it is common for some ICs to 3-state their outputs at times, a 10-kΩ pullup resistor may be desirable even when an external device is driving the pin.
DX1	L2	O/Z	IPU	Transmit data
FSR1	M3	I/O/Z	IPD	Receive frame sync
FSX1	L1	I/O/Z	IPD	Transmit frame sync
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)				
CLKS0	K3	I	IPD	External clock source (as opposed to internal)
CLKR0	H3	I/O/Z	IPD	Receive clock
CLKX0	G3	I/O/Z	IPD	Transmit clock
DR0	J1	I	IPU	Receive data
DX0	H2	O/Z	IPU	Transmit data
FSR0	J3	I/O/Z	IPD	Receive frame sync
FSX0	H1	I/O/Z	IPD	Transmit frame sync
GENERAL-PURPOSE INPUT/OUTPUT (GPIO) MODULE				
CLKOUT2/ GP[2]	Y12	I/O/Z	IPD	For this device, the CLKOUT2 pin is multiplexed with the GP[2] pin. Clock output at half of device speed (**O/Z**) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] (I/O/Z). When the CLKOUT2 pin is enabled, the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin (All devices). CLK2EN = 0: CLKOUT2 is disabled CLK2EN = 1: CLKOUT2 enabled to clock [default]
GP[7](EXT_INT7)	E3	I/O/Z	IPU	General-purpose input/output pins (**I/O/Z**) which also function as external interrupts • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]), in addition to the GPIO registers.
GP[6](EXT_INT6)	D2			
GP[5](EXT_INT5)	C1			
GP[4](EXT_INT4)	C2			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	IPD/ IPU‡	DESCRIPTION
RESERVED FOR TEST				
RSV	C12		IPU	Reserved (leave unconnected, ***do not*** connect to power or ground). On this device, this pin does ***not*** have an IPU.
RSV	D12		IPU	On this device, this pin does ***not*** have an IPU. For proper device operation, the D12 pin **must** be externally pulled down with a 10-kΩ resistor.
RSV	A5		IPU	Reserved (leave unconnected, ***do not*** connect to power or ground)
RSV	N2			Reserved. For proper device operation, this pin **must** be externally pulled up with a 10-kΩ resistor.
RSV	N1			Reserved. For proper device operation, this pin **must** be externally pulled up with a 10-kΩ resistor.
RSV	B5			Reserved (leave unconnected, ***do not*** connect to power or ground)
RSV	D7		IPD	Reserved (leave unconnected, ***do not*** connect to power or ground)
RSV	A12			Reserved. [For new designs, it is recommended that this pin be connected directly to CV_{DD} (core power). For old designs, this can be left unconnected.
RSV	B11			Reserved [For new designs, it is recommended that this pin be connected directly to V_{SS} (ground). For old designs, this pin can be left unconnected.

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
‡ IPD = Internal pulldown, IPU = Internal pullup. [To oppose the supply rail on these IPD/IPU signal pins, use external pullup or pulldown resistors no greater than 4.4 kΩ and 2.0 kΩ, respectively.]

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS			
DV_{DD}	A17 B3 B8 B13 C10 D1 D16 D19 F3 H18 J2 M18 R1 R18 T3 U5 U7 U12 U16 V13 V15 V19 W3 W9 W12 Y7 Y17	S	3.3-V supply voltage (see the power-supply decoupling portion of this data sheet)
CV_{DD}	A4 A9 A10 B2 B19 C3 C7 C18 D5 D6	S	1.4-V supply voltage (-250) 1.20-V supply voltage [See Note] (see the power-supply decoupling portion of this data sheet) Note: This value is compatible with existing 1.26−V designs.

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)			
CV_{DD}	D11 D14 D15 F4 F17 K1 K4 K17 L4 L17 L20 R4 R17 U6 U10 U11 U14 U15 V3 V18 W2 W19	S	1.4-V supply voltage (-250) 1.20-V supply voltage [See Note] (see the power-supply decoupling portion of this data sheet) Note: This value is compatible with existing 1.26−V designs.
GROUND PINS			
V_{SS}	A1 A2 A11 A14 A19 A20 B1 B4 B15 B20 C6 C8 C9 D4 D8	GND	Ground pins

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)			
V_{SS}	D13 D17 E2 E4 E17 F19 G4 G17 H4 H17 J4 J9 J10 J11 J12 K2 K9 K10 K11 K12 K20 L9 L10 L11 L12 M4 M9 M10 M11 M12 M17 N4 N17 P4 P17 P19 T4 T17	GND	Ground pins# The center thermal balls (J9−J12, K9−K12, L9−L12, M9−M12) [shaded] are all tied to ground and act as both electrical grounds and thermal relief (thermal dissipation).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)
# Shaded pin numbers denote the center thermal balls for the GDP package.

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. GDP/ ZDP	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)			
V_{SS}	U4	GND	Ground pins
	U8		
	U9		
	U13		
	U17		
	U20		
	W1		
	W5		
	W11		
	W16		
	W20		
	Y1		
	Y2		
	Y13		
	Y19		
	Y20		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal (PLL Filter)

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE): including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

device support

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. (e.g., **TMS**320C6711DGDP250). Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

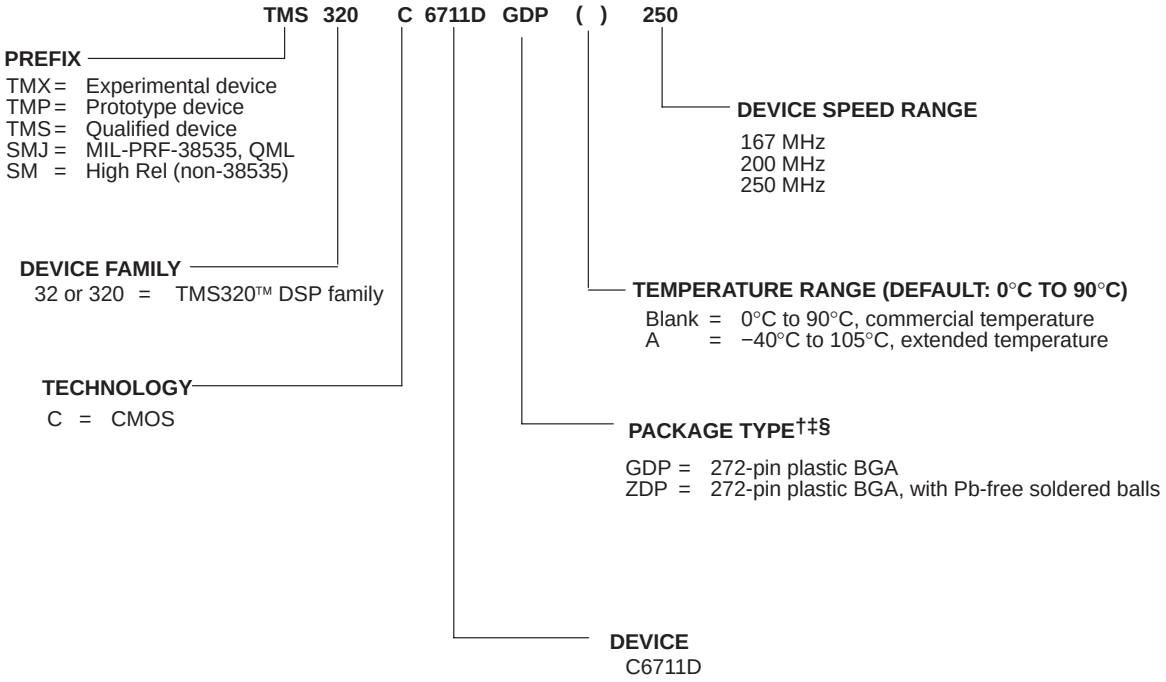
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GDP), the temperature range (for example, blank is the default commercial temperature range and A is the extended temperature range), and the device speed range in megahertz (for example, -167 is 167 MHz).

The ZDP package, like the GDP package, is a 272-ball plastic BGA *only* with Pb-free balls. For device part numbers and further ordering information for TMS320C6711D in the GDP and ZDP package types, see the TI website (http://www.ti.com) or contact your TI sales representative.

device and development-support tool nomenclature (continued)



† BGA = Ball Grid Array
‡ The ZDP mechanical package designator represents the version of the GDP with Pb−Free soldered balls. The ZDP package devices are supported in the same speed grades as the GDP package devices (***available upon request***).
§ For actual device part numbers (P/Ns) and ordering information, see the Mechanical Data section of this document or the TI website (www.ti.com).

Figure 5. TMS320C6711D DSP Device Nomenclature

documentation support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* [hereafter referred to as the C6000 PRG Overview] (literature number SPRU190) provides an overview and briefly describes the functionality of the peripherals available on the C6000™ DSP platform of devices. This document also includes a table listing the peripherals available on the C6000 devices along with literature numbers and hyperlinks to the associated peripheral documents. These C6711D peripherals, except the PLL, are similar to the peripherals on the TMS320C6711 and TMS320C64x devices; therefore, see the TMS320C6711 (C6711 or C67x) peripheral information, and in some cases, where indicated, see the TMS320C6711 (C6711 or TMS320C67x™ or C67x) peripheral information, and in some cases, where indicated, see the C64x information in the C6000 PRG Overview (literature number SPRU190).

TMS320C6000 DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide (literature number SPRU233) describes the functionality of the PLL peripheral available on the C6711C and C6711D devices.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the TMS320C62x™/TMS320C67x™ devices, associated development tools, and third-party support.

The *Migrating from TMS320C6211B/6711B to TMS320C6711C* application report (literature number SPRA837) describes the differences and issues of interest related to migration from the Texas Instruments TMS320C6211, TMS320C6211B, TMS320C6711, and TMS320C6711B devices, GFN packages, to the TMS320C6711C device, GDP package.

The *TMS320C6711/TMS320C6711B/TMS320C6711C/TMS320C6711D Digital Signal Processors Silicon Errata (C6711 Silicon Revisions 1.0, 1.2, and 1.3; C6711B Silicon Revisions 2.0 and 2.1;* and *C6711C Silicon Revision 1.1; and C6711D Silicon Revision 2.0)* [literature number SPRZ173K or later] categorizes and describes the known exceptions to the functional specifications and usage notes for the TMS320C6711, TMS320C6711B, TMS320C6711C, and TMS320C6711D DSP devices.

The *TMS320C6711D, C6712D, C6713B Power Consumption Summary* application report (literature number SPRA889A or later) discusses the power consumption for user applications with the TMS320C6713B, TMS320C6712D, and TMS320C6711D DSP devices.

The *Using IBIS Models for Timing Analysis* application report (literature number SPRA839) describes how to properly use IBIS models to attain accurate timing analysis for a given system.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

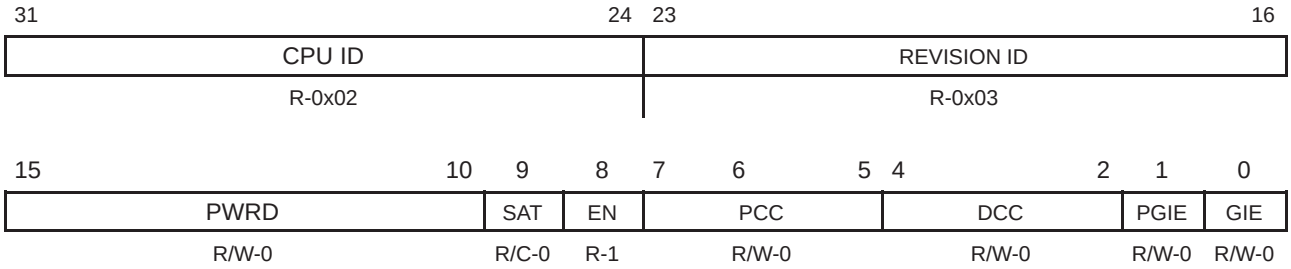
See the Worldwide Web URL for the application reports *How To Begin Development Today with the TMS320C6211 DSP* (literature number SPRA474) and *How To Begin Development with the TMS320C6711 DSP* (literature number SPRA522), which describe in more detail the similarities/differences between the C6211 and C6711 C6000™ DSP devices.

TMS320C62x is a trademark of Texas Instruments.

CPU CSR register description

The CPU control status register (CSR) contains the CPU ID and CPU Revision ID (bits 16−31) as well as the status of the device power-down modes [PWRD field (bits 15−10)], program and data cache control modes, the endian bit (EN, bit 8) and the global interrupt enable (GIE, bit 0) and previous GIE (PGIE, bit 1). Figure 6 and Table 18 identify the bit fields in the CPU CSR register.

For more detailed information on the bit fields in the CPU CSR register, see the *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) and the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).



Legend: R = Readable by the MVC instruction, R/W = Readable/Writeable by the MVC instruction; W = Read/write; -*n* = value after reset, -x = undefined value after reset, C = Clearable by the MVC instruction

Figure 6. CPU Control Status Register (CPU CSR)

CPU CSR register description (continued)

Table 18. CPU CSR Register Bit Field Description

BIT #	NAME	DESCRIPTION
31:24	CPU ID	CPU ID + REV ID. Read only. Identifies which CPU is used and defines the silicon revision of the CPU. CPU ID + REVISION ID (31:16) are combined for a value of **0x0203**
23:16	REVISION ID	
15:10	PWRD	Control power-down modes. The values are always read as zero. 000000 = no power-down (default) 001001 = PD1, wake-up by an enabled interrupt 010001 = PD1, wake-up by an enabled or not enabled interrupt 011010 = PD2, wake-up by a device reset 011100 = PD3, wake-up by a device reset Others = Reserved
9	SAT	Saturate bit. Set when any unit performs a saturate. This bit can be cleared only by the MVC instruction and can be set only by a functional unit. The set by the a functional unit has priority over a clear (by the MVC instruction) if they occur on the same cycle. The saturate bit is set one full cycle (one delay slot) after a saturate occurs. This bit will not be modified by a conditional instruction whose condition is false.
8	EN	Endian bit. This bit is read-only. Depicts the device endian mode. 0 = Big Endian mode. 1 = Little Endian mode [default].
7:5	PCC	Program Cache control mode. L1D, Level 1 Program Cache 000/010 = Cache Enabled / Cache accessed and updated on reads. All other PCC values reserved.
4:2	DCC	Data Cache control mode. L1D, Level 1 Data Cache 000/010 = Cache Enabled / 2-Way Cache All other DCC values reserved
1	PGIE	Previous GIE (global interrupt enable); saves the Global Interrupt Enable (GIE) when an interrupt is taken. Allows for proper nesting of interrupts. 0 = Previous GIE value is 0. (default) 1 = Previous GIE value is 1.
0	GIE	Global interrupt enable bit. Enables (1) or disables (0) all interrupts except the reset interrupt and NMI (nonmaskable interrupt). 0 = Disables all interrupts (except the reset interrupt and NMI) [default] 1 = Enables all interrupts (except the reset interrupt and NMI)

cache configuration (CCFG) register description

The device includes an enhancement to the cache configuration (CCFG) register. A “P” bit (CCFG.31) allows the programmer to select the priority of accesses to L2 memory originating from the transfer crossbar (TC) over accesses originating from the L1D memory system. An important class of TC accesses is EDMA transfers, which move data to or from the L2 memory. While the EDMA normally has no issue accessing L2 memory due to the high hit rates on the L1D memory system, there are pathological cases where certain CPU behavior could block the EDMA from accessing the L2 memory for long enough to cause a missed deadline when transferring data to a peripheral such as the McASP or McBSP. This can be avoided by setting the P bit to “1” because the EDMA will assume a higher priority than the L1D memory system when accessing L2 memory.

For more detailed information on the P-bit function and for silicon advisories concerning EDMA L2 memory accesses blocked, see the *TMS320C6711/TMS320C6711B/TMS320C6711C/TMS320C6711D Digital Signal Processors Silicon Errata* (literature number SPRZ173K or later).

31	30 10	9	8	7 3	2 0
P	Reserved	IP	ID	Reserved	L2MODE
R/W-0	R-x	W-0	W-0	R-0 0000	R/W-000

Legend: R = Readable; R/W = Readable/Writeable; -*n* = value after reset; -x = undefined value after reset

Figure 7. Cache Configuration Register (CCFG)

Table 19. CCFG Register Bit Field Description

BIT #	NAME	DESCRIPTION
31	P	L1D requestor priority to L2 bit. P = 0: L1D requests to L2 higher priority than TC requests P = 1: TC requests to L2 higher priority than L1D requests
30:10	Reserved	Reserved. Read-only, writes have no effect.
9	IP	Invalidate L1P bit. 0 = Normal L1P operation 1 = All L1P lines are invalidated
8	ID	Invalidate L1D bit. 0 = Normal L1D operation 1 = All L1D lines are invalidated
7:3	Reserved	Reserved. Read-only, writes have no effect.
2:0	L2MODE	L2 operation mode bits (L2MODE). 000b = L2 Cache disabled (All SRAM mode) [64K SRAM] 001b = 1-way Cache (16K L2 Cache) / [48K SRAM] 010b = 2-way Cache (32K L2 Cache) / [32K SRAM] 011b = 3-way Cache (48K L2 Cache) / [16K SRAM] 111b = 4-way Cache (64K L2 Cache) / [no SRAM] All others Reserved

interrupt sources and interrupt selector

The C67x DSP core on the device supports 16 prioritized interrupts, which are listed in Table 20. The highest priority interrupt is INT_00 (dedicated to RESET) while the lowest priority is INT_15. The first four interrupts are non-maskable and fixed. The remaining interrupts (4−15) are maskable and default to the interrupt source listed in Table 20. However, their interrupt source may be reprogrammed to any one of the sources listed in Table 21 (Interrupt Selector). Table 21 lists the selector value corresponding to each of the alternate interrupt sources. The selector choice for interrupts 4−15 is made by programming the corresponding fields (listed in Table 20) in the MUXH (address 0x019C0000) and MUXL (address 0x019C0004) registers.

Table 20. DSP Interrupts

DSP INTERRUPT NUMBER	INTERRUPT SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT INTERRUPT EVENT
INT_00	−	−	RESET
INT_01	−	−	NMI
INT_02	−	−	Reserved
INT_03	−	−	Reserved
INT_04	MUXL[4:0]	00100	GPINT4†
INT_05	MUXL[9:5]	00101	GPINT5†
INT_06	MUXL[14:10]	00110	GPINT6†
INT_07	MUXL[20:16]	00111	GPINT7†
INT_08	MUXL[25:21]	01000	EDMAINT
INT_09	MUXL[30:26]	01001	EMUDTDMA
INT_10	MUXH[4:0]	00011	SDINT
INT_11	MUXH[9:5]	01010	EMURTDXRX
INT_12	MUXH[14:10]	01011	EMURTDXTX
INT_13	MUXH[20:16]	00000	DSPINT
INT_14	MUXH[25:21]	00001	TINT0
INT_15	MUXH[30:26]	00010	TINT1

Table 21. Interrupt Selector

INTERRUPT SELECTOR VALUE (BINARY)	INTERRUPT EVENT	MODULE
00000	DSPINT	HPI
00001	TINT0	Timer 0
00010	TINT1	Timer 1
00011	SDINT	EMIF
00100	GPINT4†	GPIO
00101	GPINT5†	GPIO
00110	GPINT6†	GPIO
00111	GPINT7†	GPIO
01000	EDMAINT	EDMA
01001	EMUDTDMA	Emulation
01010	EMURTDXRX	Emulation
01011	EMURTDXTX	Emulation
01100	XINT0	McBSP0
01101	RINT0	McBSP0
01110	XINT1	McBSP1
01111	RINT1	McBSP1
10000	GPINT0	GPIO

† Interrupt Events GPINT4, GPINT5, GPINT6, and GPINT7 are outputs from the GPIO module (GP). They originate from the device pins GP[4](EXT_INT4), GP[5](EXT_INT5), GP[6](EXT_INT6), and GP[7](EXT_INT7). These pins can be used as edge-sensitive EXT_INTx with polarity controlled by the External Interrupt Polarity Register (EXTPOL.[3:0]). The corresponding pins must first be *enabled* in the GPIO module by setting the corresponding enable bits in the GP Enable Register (GPEN.[7:4]), and configuring them as *inputs* in the GP Direction Register (GPDIR.[7:4]). These interrupts can be controlled through the GPIO module in addition to the simple EXTPOL.[3:0] bits. For more information on interrupt control via the GPIO module, see the *TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number SPRU584).

EDMA module and EDMA selector

The C67x EDMA for the device also supports up to 16 EDMA channels. Four of the sixteen channels (channels 8−11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices. On the device, the user, through the EDMA selector registers, can control the EDMA channels servicing peripheral devices.

The EDMA selector registers are located at addresses 0x01A0FF00 (ESEL0), 0x01A0FF04 (ESEL1), and 0x01A0FF0C (ESEL3). These EDMA selector registers control the mapping of the EDMA events to the EDMA channels. Each EDMA event has an assigned EDMA selector code (see Table 23). By loading each EVTSELx register field with an EDMA selector code, users can map any desired EDMA event to any specified EDMA channel. Table 22 lists the default EDMA selector value for each EDMA channel.

See Table 24 and Table 25 for the EDMA Event Selector registers and their associated bit descriptions.

Table 22. EDMA Channels

EDMA CHANNEL	EDMA SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT EDMA EVENT
0	ESEL0[5:0]	000000	DSPINT
1	ESEL0[13:8]	000001	TINT0
2	ESEL0[21:16]	000010	TINT1
3	ESEL0[29:24]	000011	SDINT
4	ESEL1[5:0]	000100	GPINT4†
5	ESEL1[13:8]	000101	GPINT5†
6	ESEL1[21:16]	000110	GPINT6†
7	ESEL1[29:24]	000111	GPINT7†
8	–	–	TCC8 (Chaining)
9	–	–	TCC9 (Chaining)
10	–	–	TCC10 (Chaining)
11	–	–	TCC11 (Chaining)
12	ESEL3[5:0]	001100	XEVT0
13	ESEL3[13:8]	001101	REVT0
14	ESEL3[21:16]	001110	XEVT1
15	ESEL3[29:24]	001111	REVT1

Table 23. EDMA Selector

EDMA SELECTOR CODE (BINARY)	EDMA EVENT	MODULE
000000	DSPINT	HPI
000001	TINT0	TIMER0
000010	TINT1	TIMER1
000011	SDINT	EMIF
000100	GPINT4†	GPIO
000101	GPINT5†	GPIO
000110	GPINT6†	GPIO
000111	GPINT7†	GPIO
001000	Reserved	
001001	Reserved	
001010	GPINT2	GPIO
001011	Reserved	
001100	XEVT0	McBSP0
001101	REVT0	McBSP0
001110	XEVT1	McBSP1
001111	REVT1	McBSP1
010000−111111	Reserved	

† The GPINT[4−7] interrupt events are sourced from the GPIO module via the external interrupt capable GP[4−7] pins.

EDMA module and EDMA selector (continued)

Table 24. EDMA Event Selector Registers (ESEL0, ESEL1, and ESEL3)

ESEL0 Register (0x01A0 FF00)

31 30	29 28	27 24	23 22	21 20	19 16
Reserved	EVTSEL3		Reserved	EVTSEL2	
R−0	R/W−00 0011b		R−0	R/W−00 0010b	

15 14	13 12	11 8	7 6	5 4	3 0
Reserved	EVTSEL1		Reserved	EVTSEL0	
R−0	R/W−00 0001b		R−0	R/W−00 0000b	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL1 Register (0x01A0 FF04)

31 30	29 28	27 24	23 22	21 20	19 16
Reserved	EVTSEL7		Reserved	EVTSEL6	
R−0	R/W−00 0111b		R−0	R/W−00 0110b	

15 14	13 12	11 8	7 6	5 4	3 0
Reserved	EVTSEL5		Reserved	EVTSEL4	
R−0	R/W−00 0101b		R−0	R/W−00 0100b	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL3 Register (0x01A0 FF0C)

31 30	29 28	27 24	23 22	21 20	19 16
Reserved	EVTSEL15		Reserved	EVTSEL14	
R−0	R/W−00 1111b		R−0	R/W−00 1110b	

15 14	13 12	11 8	7 6	5 4	3 0
Reserved	EVTSEL13		Reserved	EVTSEL12	
R−0	R/W−00 1101b		R−0	R/W−00 1100b	

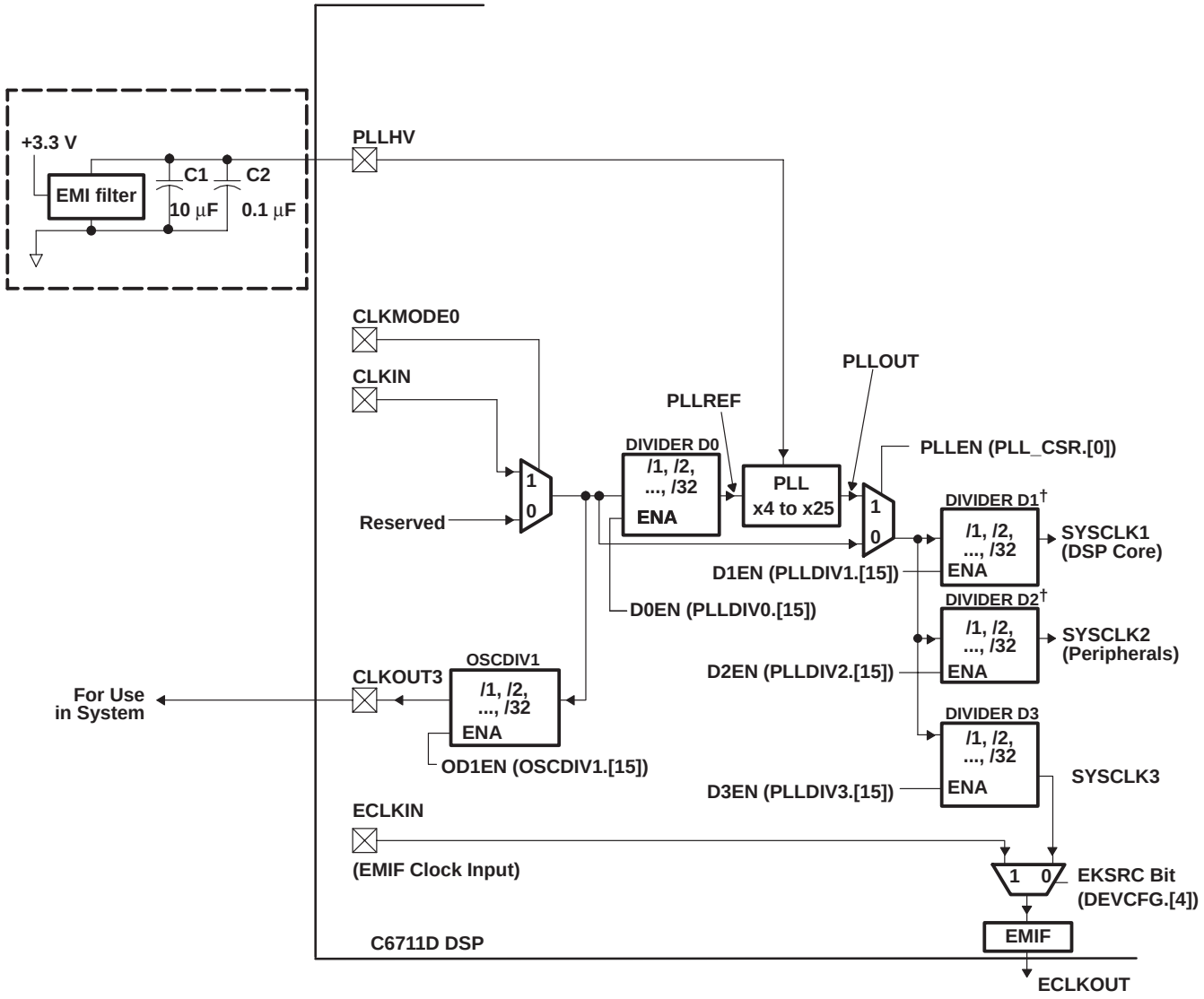
Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 25. EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description

BIT #	NAME	DESCRIPTION
31:30 23:22 15:14 7:6	Reserved	Reserved. Read-only, writes have no effect.
29:24 21:16 13:8 5:0	EVTSELx	EDMA event selection bits for channel x. Allows mapping of the EDMA events to the EDMA channels. The EVTSEL0 through EVTSEL15 bits correspond to the channels 0 to 15, respectively. These EVTSELx fields are user−selectable. By configuring the EVTSELx fields to the EDMA selector value of the desired EDMA sync event number (see Table 23), users can map any EDMA event to the EDMA channel. For example, if EVTSEL15 is programmed to 00 0001b (the EDMA selector code for TINT0), then channel 15 is triggered by Timer0 TINT0 events.

PLL and PLL controller

The device includes a PLL and a flexible PLL controller peripheral consisting of a prescaler (D0) and four dividers (OSCDIV1, D1, D2, and D3). The PLL controller is able to generate different clocks for different parts of the system (i.e., DSP core, Peripheral Data Bus, External Memory Interface, McASP, and other peripherals). Figure 8 illustrates the PLL, the PLL controller, and the clock generator logic.



† Dividers D1 and D2 must never be disabled. Never write a "0" to the D1EN or D2EN bits in the PLLDIV1 and PLLDIV2 registers.

NOTES: A. Place all PLL external components (C1, C2, and the EMI Filter) as close to the C67x™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.

B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI Filter).

C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.

D. EMI filter manufacturer TDK part number ACF451832-333, -223, -153, -103. Panasonic part number EXCCET103U.

Figure 8. PLL and Clock Generator Logic

PLL and PLL controller (continued)

The PLL Reset Time is the amount of wait time needed when resetting the PLL (writing PLLRST=1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL Reset Time value, see Table 26. The PLL Lock Time is the amount of time from when PLLRST = 0 with PLLEN = 0 (PLL out of reset, but still bypassed) to when the PLLEN bit can be safely changed to “1” (switching from bypass to the PLL path), see Table 26 and Figure 8.

Under some operating conditions, the maximum PLL Lock Time may vary from the specified typical value. For the PLL Lock Time values, see Table 26.

Table 26. PLL Lock and Reset Times

	MIN	TYP	MAX	UNIT
PLL Lock Time		75	187.5	µs
PLL Reset Time	125			ns

Table 27 shows the device’s CLKOUT signals, how they are derived and by what register control bits, and the default settings. For more details on the PLL, see the PLL and Clock Generator Logic diagram (Figure 8).

Table 27. CLKOUT Signals, Default Settings, and Control

CLOCK OUTPUT SIGNAL NAME	DEFAULT SETTING (ENABLED or DISABLED)	CONTROL BIT(s) (Register)	DESCRIPTION
CLKOUT2	ON (ENABLED)	D2EN = 1 (PLLDIV2.[15]) CK2EN = 1 (EMIF GBLCTL.[3])	SYSCLK2 selected [default]
CLKOUT3	ON (ENABLED)	OD1EN = 1 (OSCDIV1.[15])	Derived from CLKIN
ECLKOUT	ON (ENABLED); derived from SYSCLK3	EKSRC = 0 (DEVCFG.[4]) EKEN = 1 (EMIF GBLCTL.[5])	SYSCLK3 selected [default]. To select ECLKIN as source: EKSRC = 1 (DEVCFG.[4]) and EKEN = 1 (EMIF GBLCTL.[5])

This input clock is directly available as an internal high-frequency clock source that may be divided down by a programmable divider OSCDIV1 (/1, /2, /3, ..., /32) and output on the CLKOUT3 pin for other use in the system.

Figure 8 shows that the input clock source may be divided down by divider PLLDIV0 (/1, /2, ..., /32) and then multiplied up by a factor of x4, x5, x6, and so on, up to x25.

Either the input clock (PLLEN = 0) or the PLL output (PLLEN = 1) then serves as the high-frequency reference clock for the rest of the DSP system. The DSP core clock, the peripheral bus clock, and the EMIF clock may be divided down from this high-frequency clock (each with a unique divider) . For example, with a 40-MHz input, if the PLL output is configured for 400 MHz, the DSP core may be operated at 200 MHz (/2) while the EMIF may be configured to operate at a rate of 75 MHz (/6). Note that there is a specific minimum and maximum reference clock (PLLREF) and output clock (PLLOUT) for the block labeled PLL in Figure 8, as well as for the DSP core, peripheral bus, and EMIF. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). See Table 28 for the PLL clocks input and output frequency ranges.

PLL and PLL controller (continued)

Table 28. PLL Clock Frequency Ranges†‡

CLOCK SIGNAL	GDPA−167, ZDPA-167 GDP-200, ZDP−200		UNIT
	MIN	MAX	
PLLREF (PLLEN = 1)	12	100	MHz
PLLOUT	140	600	MHz
SYSCLK1	−	Device Speed (DSP Core)	MHz
SYSCLK3 (EKSRC = 0)	−	100	MHz

† SYSCLK2 rate ***must*** be exactly half of SYSCLK1.
‡ Also see the electrical specification (timing requirements and switching characteristics parameters) in the Input and Output Clocks section of this data sheet.

The EMIF itself may be clocked by an external reference clock via the ECLKIN pin or can be generated on-chip as SYSCLK3. SYSCLK3 is derived from divider D3 off of PLLOUT (see Figure 8, PLL and Clock Generator Logic). The EMIF clock selection is programmable via the EKSRC bit in the DEVCFG register.

The settings for the PLL multiplier and each of the dividers in the clock generation block may be reconfigured via software at run time. If either the input to the PLL changes due to D0, CLKMODE0, or CLKIN, or if the PLL multiplier is changed, then software must enter bypass first and stay in bypass until the PLL has had enough time to lock (see electrical specifications). For the programming procedure, see the *TMS320C6000 DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide* (literature number SPRU233).

SYSCLK2 is the internal clock source for peripheral bus control. SYSCLK2 (Divider D2) ***must*** be programmed to be half of the SYSCLK1 rate. For example, if D1 is configured to divide-by-2 mode (/2), then D2 ***must*** be programmed to divide-by-4 mode (/4). SYSCLK2 is also tied directly to CLKOUT2 pin (see Figure 8).

During the programming transition of Divider D1 and Divider D2 (resulting in SYSCLK1 and SYSCLK2 output clocks, see Figure 8), the order of programming the PLLDIV1 and PLLDIV2 registers must be observed to ensure that SYSCLK2 always runs at half the SYSCLK1 rate or slower. For example, if the divider ratios of D1 and D2 are to be changed from /1, /2 (respectively) to /5, /10 (respectively) then, the PLLDIV2 register must be programmed before the PLLDIV1 register. The transition ratios become /1, /2; /1, /10; and then /5, /10. If the divider ratios of D1 and D2 are to be changed from /3, /6 to /1, /2 then, the PLLDIV1 register must be programmed before the PLLDIV2 register. The transition ratios, for this case, become /3, /6; /1, /6; and then /1, /2. The final SYSCLK2 rate ***must*** be exactly half of the SYSCLK1 rate.

Note that Divider D1 and Divider D2 must ***always*** be enabled (i.e., D1EN and D2EN bits are set to “1” in the PLLDIV1 and PLLDIV2 registers).

The PLL Controller registers should be modified only by the CPU or via emulation. The HPI should ***not*** be used to directly access the PLL Controller registers.

For detailed information on the clock generator (PLL Controller registers) and their associated software bit descriptions, see Table 29 through Table 32.

PLL and PLL controller (continued)

PLLCSR Register (0x01B7 C100)

31	28	27	24	23	20	19	16
Reserved							
R−0							

15	12	11	8	7	6	5	4	3	2	1	0
Reserved					STABLE	Reserved		PLLRST	Reserved	PLLPWRDN	PLLEN
R−0					R−x	R−0		RW−1	R/W−0	R/W−0b	RW−0

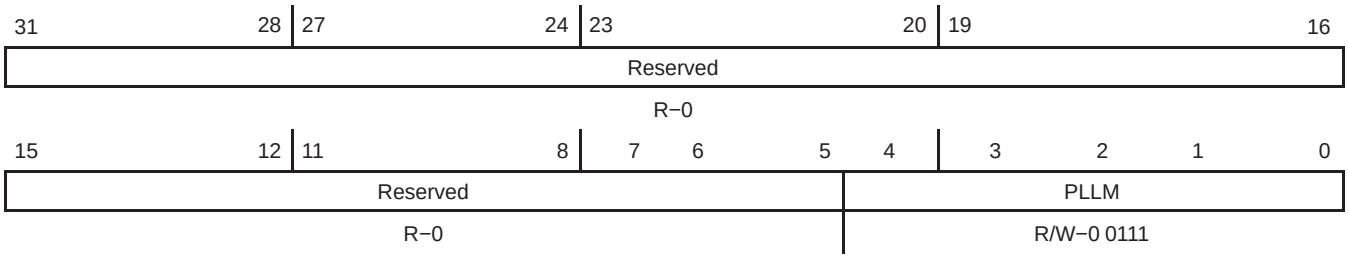
Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 29. PLL Control/Status Register (PLLCSR)

BIT #	NAME	DESCRIPTION
31:7	Reserved	Reserved. Read-only, writes have no effect.
6	STABLE	Oscillator Input Stable. This bit indicates if the OSCIN/CLKIN input has stabilized. 0 – OSCIN/CLKIN input not yet stable. Oscillator counter is not finished counting (default). 1 – OSCIN/CLKIN input stable.
5:4	Reserved	Reserved. Read-only, writes have no effect.
3	PLLRST	Asserts RESET to PLL 0 – PLL Reset Released. 1 – PLL Reset Asserted (default).
2	Reserved	Reserved. The user ***must*** write a “0” to this bit.
1	PLLPWRDN	Select PLL Power Down 0 – PLL Operational (default). 1 – PLL Placed in Power-Down State.
0	PLLEN	PLL Mode Enable 0 – Bypass Mode (default). PLL disabled. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock. 1 – PLL Enabled. Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output.

PLL and PLL controller (continued)

PLLM Register (0x01B7 C110)



Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 30. PLL Multiplier Control Register (PLLM)

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLM	PLL multiply mode [default is x7 (0 0111)]. 00000 = Reserved 10000 = x16 00001 = Reserved 10001 = x17 00010 = Reserved 10010 = x18 00011 = Reserved 10011 = x19 00100 = x4 10100 = x20 00101 = x5 10101 = x21 00110 = x6 10110 = x22 00111 = x7 10111 = x23 01000 = x8 11000 = x24 01001 = x9 11001 = x25 01010 = x10 11010 = Reserved 01011 = x11 11011 = Reserved 01100 = x12 11100 = Reserved 01101 = x13 11101 = Reserved 01110 = x14 11110 = Reserved 01111 = x15 11111 = Reserved PLLM select values 00000 through 00011 and 11010 through 11111 are *not* supported.

PLL and PLL controller (continued)

PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 Registers (0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively)

31 – 28	27 – 24	23 – 20	19 – 16
Reserved			
R−0			

15	14 – 12	11 – 8	7 – 5	4	3 – 0
DxEN	Reserved			PLLDIVx	
R/W−1	R−0			R/W−x xxxx†	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

† Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1 (0 0000), /1 (0 0000), /2 (0 0001), and /2 (0 0001), respectively.

CAUTION:
D1, and D2 should never be disabled. D3 should only be disabled if ECLKIN is used.

Table 31. PLL Wrapper Divider x Registers (Prescaler Divider D0 and Post-Scaler Dividers D1, D2, and D3)‡

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	DxEN	Divider Dx Enable (where x denotes 0 through 3). 0 – Divider x Disabled. No clock output. 1 – Divider x Enabled (default). **These divider-enable bits are device-specific and must be set to 1 to enable.**
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLDIVx	PLL Divider Ratio [Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1, /1, /2, and /2, respectively]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

‡ Note that SYSCLK2 *must* run at half the rate of SYSCLK1. Therefore, the divider ratio of D2 must be two times slower than D1. For example, if D1 is set to /2, then D2 *must* be set to /4.

PLL and PLL controller (continued)

OSCDIV1 Register (0x01B7 C124)

31	28	27	24	23	20	19	16
Reserved							
R−0							

15	14	12	11	8	7	5	4	3	2	1	0
OD1EN	Reserved						OSCDIV1				
R/W−1	R−0						R/W−0 0111				

Legend: R = Read only, R/W = Read/Write; -n = value after reset

The OSCDIV1 register controls the oscillator divider 1 for CLKOUT3. The CLKOUT3 signal does ***not*** go through the PLL path.

Table 32. Oscillator Divider 1 Register (OSCDIV1)

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	OD1EN	Oscillator Divider 1 Enable. 0 – Oscillator Divider 1 Disabled. 1 – Oscillator Divider 1 Enabled (default).
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	OSCDIV1	Oscillator Divider 1 Ratio [default is /8 (0 0111)]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

general-purpose input/output (GPIO)

To use the GP[7:4, 2] software-configurable GPIO pins, the GPxEN bits in the GP Enable (GPEN) Register and the GPxDIR bits in the GP Direction (GPDIR) Register must be properly configured.

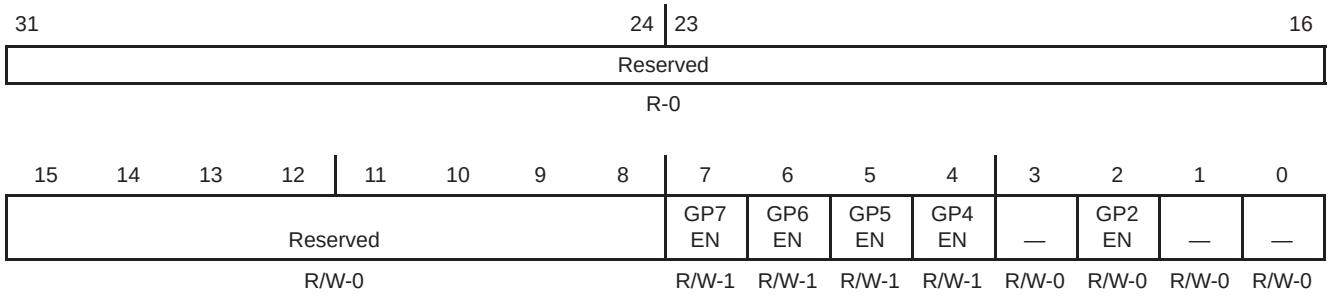
GPxEN = 1 GP[x] pin is enabled

GPxDIR = 0 GP[x] pin is an input

GPxDIR = 1 GP[x] pin is an output

where “x” represents one of the 7 through 4, or 2 GPIO pins

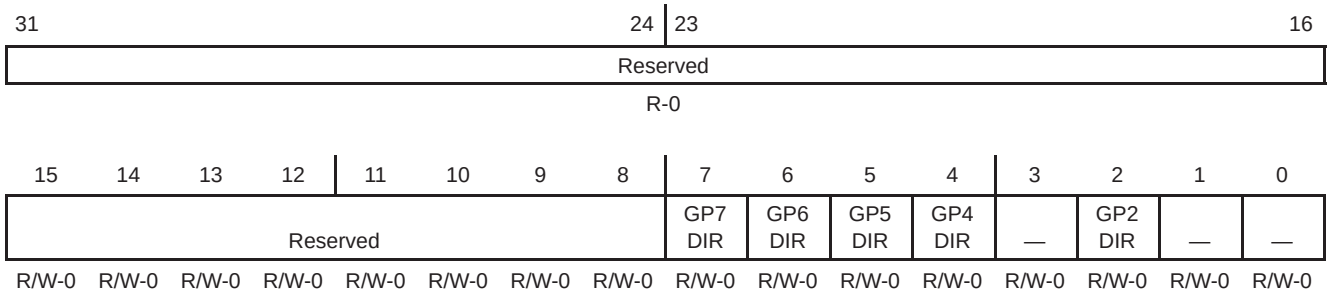
Figure 9 shows the GPIO enable bits in the GPEN register for the device. To use any of the GPx pins as general-purpose input/output functions, the corresponding GPxEN bit must be set to “1” (enabled). Default values are device-specific, so refer to Figure 9 for the C6711D default configuration.



Legend: R/W = Readable/Writeable; -*n* = value after reset, -x = undefined value after reset

Figure 9. GPIO Enable Register (GPEN) [Hex Address: 01B0 0000]

Figure 10 shows the GPIO direction bits in the GPDIR register. This register determines if a given GPIO pin is an input or an output providing the corresponding GPxEN bit is enabled (set to “1”) in the GPEN register. By default, all the GPIO pins are configured as input pins.



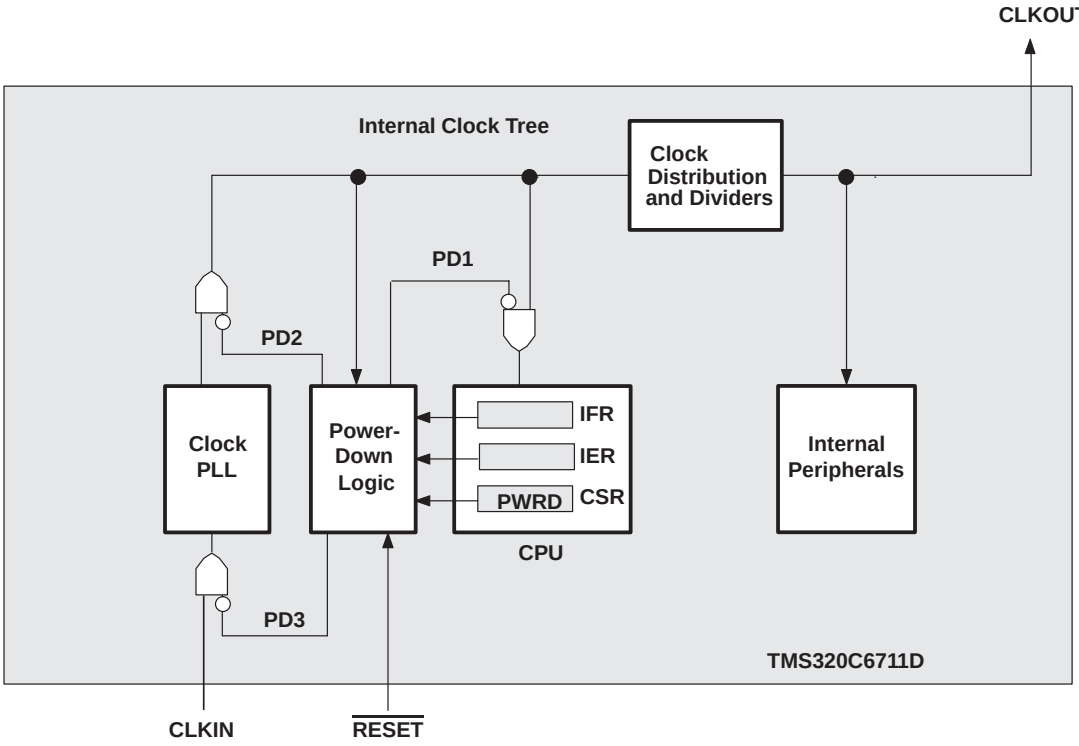
Legend: R/W = Readable/Writeable; -*n* = value after reset, -x = undefined value after reset

Figure 10. GPIO Direction Register (GPDIR) [Hex Address: 01B0 0004]

For more detailed information on general-purpose inputs/outputs (GPIOs), see the *TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide* (literature number SPRU584).

power-down mode logic

Figure 11 shows the power-down mode logic on the device.



† External input clocks, with the exception of CLKOUT3 and CLKIN, are *not* gated by the power-down mode logic.

Figure 11. Power-Down Mode Logic†

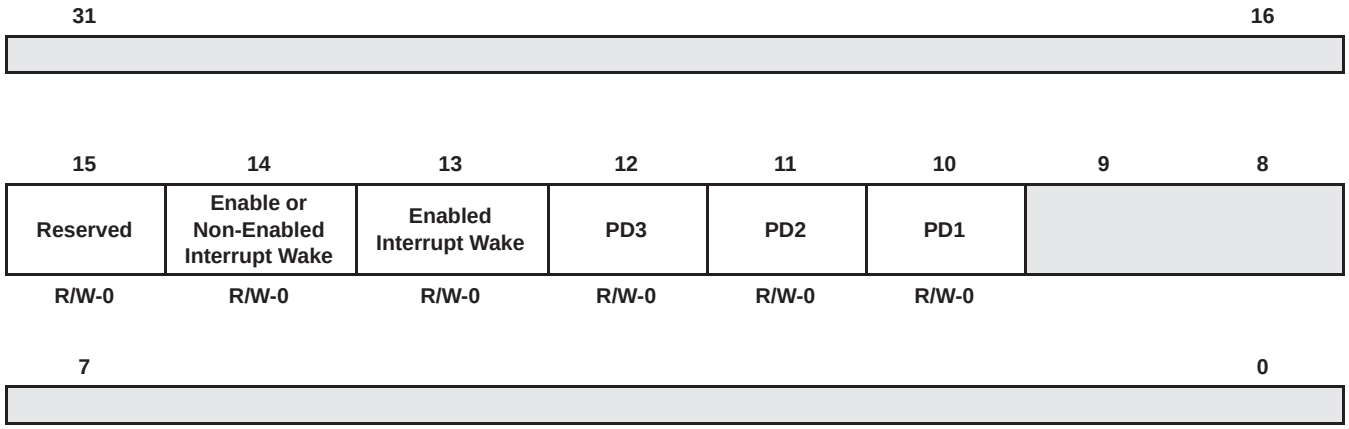
triggering, wake-up, and effects

The device includes a programmable PLL which allows software control of PLL bypass via the PLLEN bit in the PLLCSR register. With this enhanced functionality come some additional considerations when entering power−down modes.

The power−down modes (PD2 and PD3) function by disabling the PLL to stop clocks to the C6711D device. However, if the PLL is bypassed (PLLEN = 0), the device will still receive clocks from the external clock input (CLKIN). Therefore, bypassing the PLL makes the power−down modes PD2 and PD3 ineffective. The PLL needs to be enabled by writing a “1” to PLLEN bit (PLLCSR.0) before being able to enter either PD3 (CSR.11) or PD2 (CSR.10) in order for these modes to have an effect.

For the TMS320C6711D device, it is recommended to use the PLLPWDN bit (PLLCSR.1) to enter a deep power−down state equivalent to PD3 since the PLLPWDN bit takes full advantage of the PLL power−down feature.

The power−down modes (PD1, PD2, and PD3) and their wake−up methods are programmed by setting the PWRD field (bits 15−10) of the control status register (CSR). The PWRD field of the CSR is shown in Figure 12 and described in Table 33. When writing to the CSR, all bits of the PWRD field should be set at the same time. Logic 0 should be used when “writing” to the reserved bit (bit 15) of the PWRD field. The CSR is discussed in detail in the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).



Legend: R/W−x = Read/write reset value

NOTE: The shadowed bits are not part of the power-down logic discussion and therefore are not covered here. For information on these other bit fields in the CSR register, see the *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189).

Figure 12. PWRD Field of the CSR Register

A delay of up to nine clock cycles may occur after the instruction that sets the PWRD bits in the CSR before the PD mode takes effect. As best practice, NOPs should be padded after the PWRD bits are set in the CSR to account for this delay.

If PD1 mode is terminated by a non-enabled interrupt, the program execution returns to the instruction where PD1 took effect. If PD1 mode is terminated by an enabled interrupt, the interrupt service routine will be executed first, then the program execution returns to the instruction where PD1 took effect. In the case with an enabled interrupt, the GIE bit in the CSR and the NMIE bit in the interrupt enable register (IER) must also be set in order for the interrupt service routine to execute; otherwise, execution returns to the instruction where PD1 took effect upon PD1 mode termination by an enabled interrupt.

PD2 and PD3 modes can only be aborted by device reset. Table 33 summarizes all the power-down modes.

Table 33. Characteristics of the Power-Down Modes

PRWD FIELD (BITS 15−10)	POWER-DOWN MODE	WAKE-UP METHOD	EFFECT ON CHIP'S OPERATION
000000	No power-down	—	—
001001	PD1	Wake by an enabled interrupt	CPU halted (except for the interrupt logic) Power-down mode blocks the internal clock inputs at the boundary of the CPU, preventing most of the CPU's logic from switching. During PD1, EDMA transactions can proceed between peripherals and internal memory.
010001	PD1	Wake by an enabled or non-enabled interrupt	
011010	PD2†	Wake by a device reset	Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire chip being halted. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off.
011100	PD3†	Wake by a device reset	Input clock to the PLL stops generating clocks. All register and internal RAM contents are preserved. All functional I/O freeze in the last state when the PLL clock is turned off. Following reset, the PLL needs time to re−lock, just as it does following power−up. Wake−up from PD3 takes longer than wake−up from PD2 because the PLL needs to be re−locked, just as it does following power−up. It is recommended to use the PLLPWDN bit (PLLCSR.1) as an alternative to PD3.
All others	Reserved	—	—

† When entering PD2 and PD3, all functional I/O remains in the previous state. However, for peripherals which are asynchronous in nature or peripherals with an external clock source, output signals may transition in response to stimulus on the inputs. Under these conditions, peripherals will not operate according to specifications.

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time (>1 second) if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. The core supply should be powered up prior to (and powered down after) the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

A dual-power supply with simultaneous sequencing can be used to eliminate the delay between core and I/O power up. A Schottky diode can also be used to tie the core rail to the I/O rail (see Figure 13).

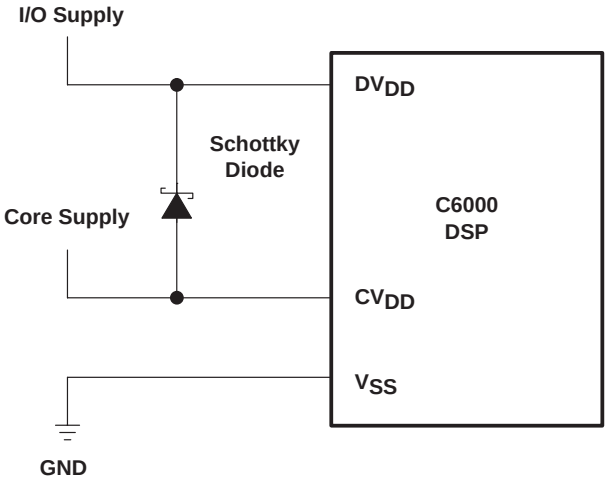


Figure 13. Schottky Diode Diagram

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

power-supply decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. Assuming 0603 caps, the user should be able to fit a total of 60 caps — 30 for the core supply and 30 for the I/O supply. These caps need to be close (no more than 1.25 cm maximum distance) to the DSP to be effective. Physically smaller caps are better, such as 0402, but the size needs to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime needs to be considered.

IEEE 1149.1 JTAG compatibility statement

The TMS320C6711D DSP requires that both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ resets be asserted upon power up to be properly initialized. While $\overline{\text{RESET}}$ initializes the DSP core, $\overline{\text{TRST}}$ initializes the DSP's emulation logic. Both resets are required for proper operation.

Note: $\overline{\text{TRST}}$ is synchronous and ***must*** be clocked by TCLK; otherwise, BSCAN may not respond as expected after $\overline{\text{TRST}}$ is asserted.

While both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ need to be asserted upon power up, only $\overline{\text{RESET}}$ needs to be released for the DSP to boot properly. $\overline{\text{TRST}}$ may be asserted indefinitely for normal operation, keeping the JTAG port interface and DSP's emulation logic in the reset state. $\overline{\text{TRST}}$ only needs to be released when it is necessary to use a JTAG controller to debug the DSP or exercise the DSP's boundary scan functionality.

The TMS320C6711D DSP includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of an external pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the DSP after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations.

Following the release of $\overline{\text{RESET}}$, the low-to-high transition of $\overline{\text{TRST}}$ must be "seen" to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either Boundary Scan mode or Emulation mode. For more detailed information, see the terminal functions section of this data sheet.

Note: The DESIGN−WARNING section of the TMS320C6711D BSDL file contains information and constraints regarding proper device operation while in Boundary Scan Mode.

For more detailed information on the C6711D JTAG emulation, see the *TMS320C6000 DSP Designing for JTAG Emulation Reference Guide* (literature number SPRU641).

EMIF device speed

The maximum EMIF speed on the device is 100 MHz. TI recommends utilizing I/O buffer information specification (IBIS) to analyze all AC timings to determine if the maximum EMIF speed is achievable for a given board layout. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839).

For ease of design evaluation, Table 34 contains IBIS simulation results showing the maximum EMIF-SDRAM interface speeds for the given example boards (TYPE) and SDRAM speed grades. Timing analysis should be performed to verify that all AC timings are met for the specified board layout. Other configurations are also possible, but again, timing analysis must be done to verify proper AC timings.

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (see the Terminal Functions table for the EMIF output signals).

Table 34. Example Boards and Maximum EMIF Speed

BOARD CONFIGURATION			SDRAM SPEED GRADE	MAXIMUM ACHIEVABLE EMIF-SDRAM INTERFACE SPEED
TYPE	EMIF INTERFACE COMPONENTS	BOARD TRACE		
1-Load Short Traces	One bank of one 32-Bit SDRAM	1 to 3-inch traces with proper termination resistors; Trace impedance ~ 50 Ω	143 MHz 32-bit SDRAM (−7)	100 MHz
			166 MHz 32-bit SDRAM (−6)	For short traces, SDRAM data output hold time on these SDRAM speed grades cannot meet EMIF input hold time requirement (see NOTE 1).
			183 MHz 32-bit SDRAM (−55)	
			200 MHz 32-bit SDRAM (−5)	
2-Loads Short Traces	One bank of two 16-Bit SDRAMs	1.2 to 3 inches from EMIF to each load, with proper termination resistors; Trace impedance ~ 78 Ω	125 MHz 16-bit SDRAM (−8E)	100 MHz
			133 MHz 16-bit SDRAM (−75)	100 MHz
			143 MHz 16-bit SDRAM (−7E)	100 MHz
			167 MHz 16-bit SDRAM (−6A)	100 MHz
			167 MHz 16-bit SDRAM (−6)	100 MHz
3-Loads Short Traces	One bank of two 16-Bit SDRAMs One bank of buffer	1.2 to 3 inches from EMIF to each load, with proper termination resistors; Trace impedance ~ 78 Ω	125 MHz 16-bit SDRAM (−8E)	For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1).
			133 MHz 16-bit SDRAM (−75)	100 MHz
			143 MHz 16-bit SDRAM (−7E)	100 MHz
			167 MHz 16-bit SDRAM (−6A)	100 MHz
			167 MHz 16-bit SDRAM (−6)	For short traces, EMIF cannot meet SDRAM input hold requirement (see NOTE 1).
3-Loads Long Traces	One bank of one 32-Bit SDRAM One bank of one 32-Bit SBSRAM One bank of buffer	4 to 7 inches from EMIF; Trace impedance ~ 63 Ω	143 MHz 32-bit SDRAM (−7)	83 MHz
			166 MHz 32-bit SDRAM (−6)	83 MHz
			183 MHz 32-bit SDRAM (−55)	83 MHz
			200 MHz 32-bit SDRAM (−5)	SDRAM data output hold time cannot meet EMIF input hold requirement (see NOTE 1).

NOTE 1: Results are based on IBIS simulations for the given example boards (**TYPE**). Timing analysis should be performed to determine if timing requirements can be met for the particular system.

EMIF big endian mode correctness

The HD8 pin device endian mode (LENDIAN) selects the endian mode of operation (Little or Big Endian). For the device, Little Endian is the default setting.

The HD12 pin (EMIF Big Endian Mode Correctness) [$\overline{\text{EMIFBE}}$] enhancement allows the flexibility to change the EMIF data placement on the EMIF bus.

When using the default setting of HD12 = 1, the EMIF will present 8-bit and 16-bit data on the ED[7:0] side of the bus if using Little Endian mode (HD8 = 1) and to the ED[31:24] side of the bus if using Big Endian mode. Figure 14 shows the mapping of 16-bit and 8-bit devices with EMIF endianness correction.

EMIF DATA LINES (PINS) WHERE DATA PRESENT			
ED[31:24] ($\overline{\text{BE3}}$)	**ED[23:16] ($\overline{\text{BE2}}$)**	**ED[15:8] ($\overline{\text{BE1}}$)**	**ED[7:0] ($\overline{\text{BE0}}$)**
32-Bit Device in Any Endianness Mode			
16-Bit Device in Big Endianness Mode		16-Bit Device in Little Endianness Mode	
8-Bit Device in Big Endianness Mode			8-Bit Device in Little Endianness Mode

Figure 14. 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 1)

When HD12 = 0, enabling EMIF endianness correction, the EMIF will present 8-bit and 16-bit data on the ED[7:0] side of the bus, regardless of the endianess mode (see Figure 15).

EMIF DATA LINES (PINS) WHERE DATA PRESENT			
ED[31:24] ($\overline{\text{BE3}}$)	**ED[23:16] ($\overline{\text{BE2}}$)**	**ED[15:8] ($\overline{\text{BE1}}$)**	**ED[7:0] ($\overline{\text{BE0}}$)**
32-Bit Device in Any Endianness Mode			
		16-Bit Device in **Any** Endianness Mode	
			8-Bit Device in **Any** Endianness Mode

Figure 15. 16/8-Bit EMIF Big Endian Mode Correctness Mapping (HD12 = 0)

This *new* endianness correction functionality does not affect systems using the default value of HD12=1.

This *new* feature does *not* affect systems operating in Little Endian mode.

bootmode

The C67x™ device resets using the active-low signal $\overline{\text{RESET}}$ and the internal reset signal. While $\overline{\text{RESET}}$ is low, the internal reset is also asserted and the device is held in reset and is initialized to the prescribed reset state. Refer to reset timing for reset timing characteristics and states of device pins during reset. The release of the internal reset signal (see the Reset Phase 3 discussion in the Reset Timing section of this data sheet) starts the processor running with the prescribed device configuration and boot mode.

The device has three types of boot modes:

- Host boot

  If host boot is selected, upon release of internal reset, the CPU is internally “stalled” while the remainder of the device is released. During this period, an external host can initialize the CPU’s memory space as necessary through the host interface, including internal configuration registers, such as those that control the EMIF or other peripherals. Once the host is finished with all necessary initialization, it must set the DSPINT bit in the HPIC register to complete the boot process. This transition causes the boot configuration logic to bring the CPU out of the “stalled” state. The CPU then begins execution from address 0. The DSPINT condition is not latched by the CPU, because it occurs while the CPU is still internally “stalled”. Also, DSPINT brings the CPU out of the “stalled” state only if the host boot process is selected. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP if required. After the CPU is out of the “stalled” state, the CPU needs to clear the DSPINT, otherwise, no more DSPINTs can be received.

- Emulation boot

  Emulation boot mode is a variation of host boot. In this mode, it is not necessary for a host to load code or to set DSPINT to release the CPU from the “stalled” state. Instead, the emulator will set DSPINT if it has not been previously set so that the CPU can begin executing code from address 0. Prior to beginning execution, the emulator sets a breakpoint at address 0. This prevents the execution of invalid code by halting the CPU prior to executing the first instruction. Emulation boot is a good tool in the debug phase of development.

- EMIF boot (using default ROM timings)

  Upon the release of internal reset, the 1K-Byte ROM code located in the beginning of $\overline{\text{CE1}}$ is copied to address 0 by the EDMA using the default ROM timings, while the CPU is internally “stalled”. The data should be stored in the endian format that the system is using. The boot process also lets you choose the width of the ROM. In this case, the EMIF automatically assembles consecutive 8-bit bytes or 16-bit half-words to form the 32-bit instruction words to be copied. The transfer is automatically done by the EDMA as a single-frame block transfer from the ROM to address 0. After completion of the block transfer, the CPU is released from the “stalled” state and start running from address 0.

reset

A hardware reset ($\overline{\text{RESET}}$) is required to place the DSP into a known good state out of power−up. The $\overline{\text{RESET}}$ signal can be asserted (pulled low) prior to ramping the core and I/O voltages or after the core and I/O voltages have reached their proper operating conditions. As a best practice, reset should be held low during power−up. Prior to deasserting $\overline{\text{RESET}}$ (low−to−high transition), the core and I/O voltages should be at their proper operating conditions and CLKIN should also be running at the correct frequency.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, CV_{DD} (see Note 2) . . . . . − 0.3 V to 1.8 V
Supply voltage range, DV_{DD} (see Note 2) . . . . . −0.3 V to 4 V
Input voltage range . . . . . −0.3 V to DV_{DD} + 0.5 V
Output voltage range . . . . . −0.3 V to DV_{DD} + 0.5 V
Operating case temperature ranges, T_C (default) . . . . . 0°C to 90°C
(A version) [C6711DGDPA and C6711DZDPA] . . . −40°C to105°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to V_{SS}.

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core	−250 only	1.33	1.4	1.47	V
			1.14§	1.20§	1.32	V
DV_{DD}	Supply voltage, I/O		3.13	3.3	3.47	V
V_{SS}	Supply ground		0	0	0	V
V_{IH}	High-level input voltage	All signals except CLKS1, DR1, and $\overline{\text{RESET}}$	2			V
		CLKS1, DR1, and $\overline{\text{RESET}}$	2			
V_{IL}	Low-level input voltage	All signals except CLKS1, DR1, and $\overline{\text{RESET}}$			0.8	V
		CLKS1, DR1, and $\overline{\text{RESET}}$			0.3*DV_{DD}	
I_{OH}	High-level output current¶	All signals except ECLKOUT, CLKOUT2, CLKS1, and DR1			–8	mA
		ECLKOUT and CLKOUT2			–16	
I_{OL}	Low-level output current¶	All signals except ECLKOUT, CLKOUT2, CLKS1, and DR1			8	mA
		ECLKOUT and CLKOUT2			16	mA
		CLKS1 and DR1			3	mA
T_C	Operating case temperature	Default	0		90	°C
V_{OS}	Maximum voltage during overshoot (See Figure 19)				4#	V
V_{US}	Maximum voltage during undershoot (See Figure 20)				–0.7#	V
T_C	Operating case temperature	A version (C6711DGDPA and C6711DZDPA)	–40		105	°C

‡ The core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.

§ These values are compatible with existing 1.26−V designs.

¶ Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see the device-specific IBIS models.

The absolute maximum ratings should *not* be exceeded for more than 30% of the cycle period.

electrical characteristics over recommended ranges of supply voltage and operating case temperature† (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All signals except CLKS1 and DR1	DV_{DD} = MIN, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	All signals except CLKS1 and DR1	DV_{DD} = MIN, I_{OL} = MAX			0.4	V
		CLKS1 and DR1				0.4	
I_I	Input current	All signals except CLKS1 and DR1	V_I = V_{SS} to DV_{DD}			±170	uA
		CLKS1 and DR1				±10	uA
I_{OZ}	Off-state output current	All signals except CLKS1 and DR1	V_O = DV_{DD} or 0 V			±170	uA
		CLKS1 and DR1				±10	uA
I_{DD2V}	Core supply current‡		GDP, CV_{DD} = 1.4-V, CPU clock = 250 MHz		810		mA
			GDP/ZDP, CV_{DD} = 1.26-V, CPU clock = 200 MHz		560		
			GDPA/ZDPA, CV_{DD} = 1.26-V, CPU clock = 167 MHz		475		
I_{DD3V}	I/O supply current‡		DV_{DD} = 3.3-V, EMIF speed = 100 MHz		75		mA
C_i	Input capacitance					7	pF
C_o	Output capacitance					7	pF

† For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

‡ For this device, these currents were measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. This model represents a device performing high-DSP-activity operations 50% of the time, and the remainder performing low-DSP-activity operations. The high/low-DSP-activity models are defined as follows:

High-DSP-Activity Model:

CPU: 8 instructions/cycle with 2 LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions; L1 Program Memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit-switching)]

McBSP: 2 channels at E1 rate

Timers: 2 timers at maximum rate

Low-DSP-Activity Model:

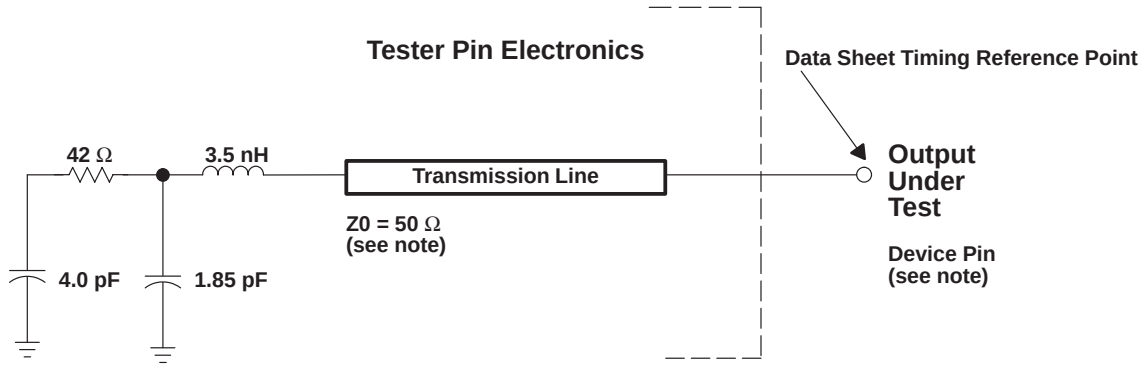
CPU: 2 instructions/cycle with 1 LDH instruction [L1 Data Memory: 16 bits/cycle; L1 Program Memory: 256 bits per 4 cycles; L2/EMIF EDMA: None]

McBSP: 2 channels at E1 rate

Timers: 2 timers at maximum rate

The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6711D/12D/13B Power Consumption Summary* application report (literature number SPRA889A).

PARAMETER MEASUREMENT INFORMATION



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 16. Test Load Circuit for AC Timing Measurements

signal transition levels

All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.

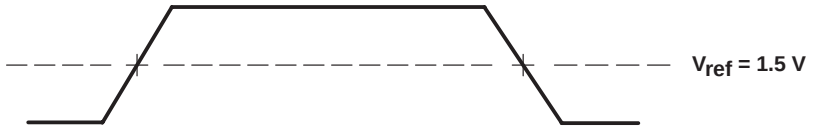


Figure 17. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, and V_{OL} MAX and V_{OH} MIN for output clocks.

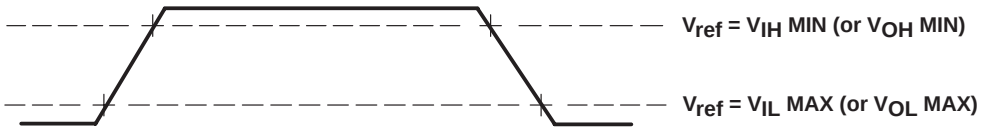


Figure 18. Rise and Fall Transition Time Voltage Reference Levels

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

AC transient rise/fall time specifications

Figure 19 and Figure 20 show the AC transient specifications for Rise and Fall Time. For device-specific information on these values, refer to the Recommended Operating Conditions section of this Data Sheet.

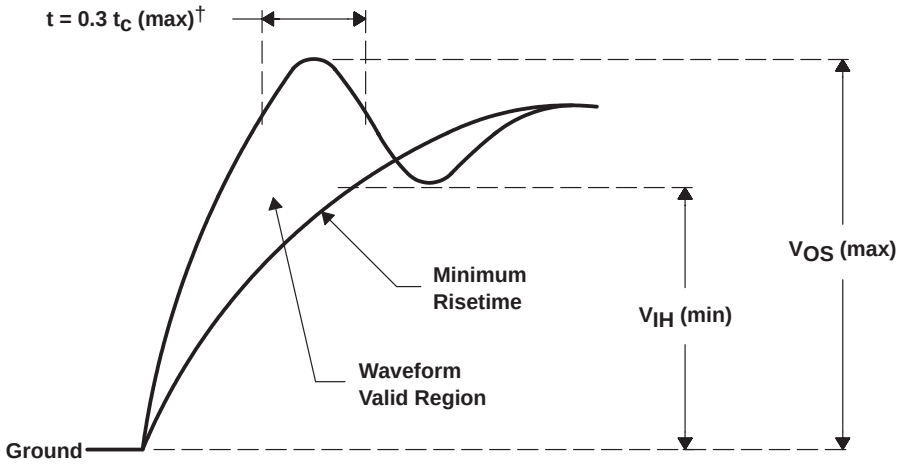


Figure 19. AC Transient Specification Rise Time

† t_c = the peripheral cycle time.

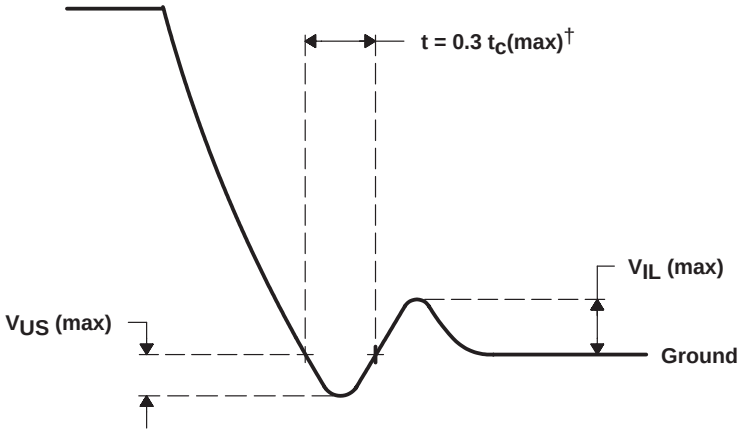


Figure 20. AC Transient Specification Fall Time

† t_c = the peripheral cycle time.

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

timing parameters and board routing analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

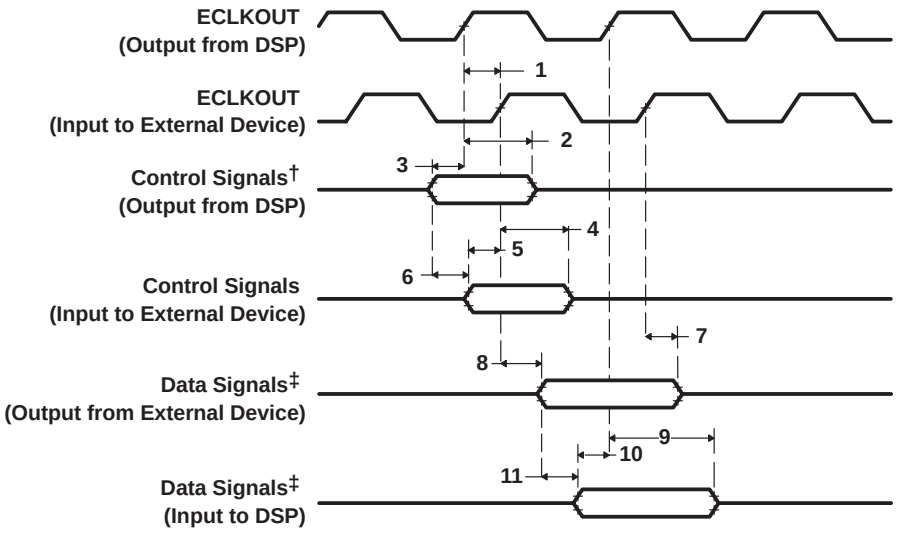
For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see Table 35 and Figure 21).

Figure 21 represents a general transfer between the DSP and an external device. The figure also represents board route delays and how they are perceived by the DSP and the external device.

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

Table 35. Board-Level Timings Example (see Figure 21)

NO.	DESCRIPTION
1	Clock route delay
2	Minimum DSP hold time
3	Minimum DSP setup time
4	External device hold time requirement
5	External device setup time requirement
6	Control signal route delay
7	External device hold time
8	External device access time
9	DSP hold time requirement
10	DSP setup time requirement
11	Data route delay



† Control signals include data for Writes.
‡ Data signals are generated during Reads from an external device.

Figure 21. Board-Level Input/Output Timings

INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN†‡§ (see Figure 22)

NO.			GDPA-167, ZDPA−167				−200				UNIT
			PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN	6	83.3	6.7		5	83.3	6.7		ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.4C		0.4C		0.4C		0.4C		ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.4C		0.4C		0.4C		0.4C		ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN		5		5		5		5	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
§ See the *PLL and PLL controller* section of this data sheet.

timing requirements for CLKIN†‡§ (see Figure 22)

NO.			−250				UNIT
			PLL MODE (PLLEN = 1)		BYPASS MODE (PLLEN = 0)		
			MIN	MAX	MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN	4	83.3	6.7		ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high	0.4C		0.4C		ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low	0.4C		0.4C		ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN		5		5	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ C = CLKIN cycle time in nanoseconds (ns). For example, when CLKIN frequency is 40 MHz, use C = 25 ns.
§ See the *PLL and PLL controller* section of this data sheet.

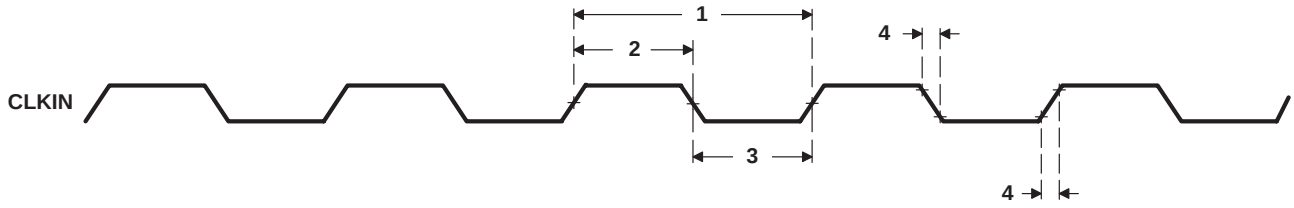


Figure 22. CLKIN Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT2†‡ (see Figure 23)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{c(CKO2)}$	Cycle time, CLKOUT2	C2 − 0.8	C2 + 0.8	ns
2	$t_{w(CKO2H)}$	Pulse duration, CLKOUT2 high	(C2/2) − 0.8	(C2/2) + 0.8	ns
3	$t_{w(CKO2L)}$	Pulse duration, CLKOUT2 low	(C2/2) − 0.8	(C2/2) + 0.8	ns
4	$t_{t(CKO2)}$	Transition time, CLKOUT2		2	ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
‡ C2 = CLKOUT2 period in ns. CLKOUT2 period is determined by the PLL controller output SYSCLK2 period, which ***must*** be set to CPU period divide-by-2.

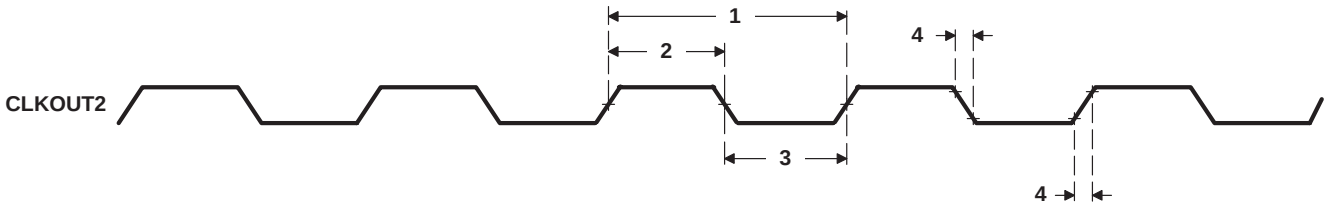
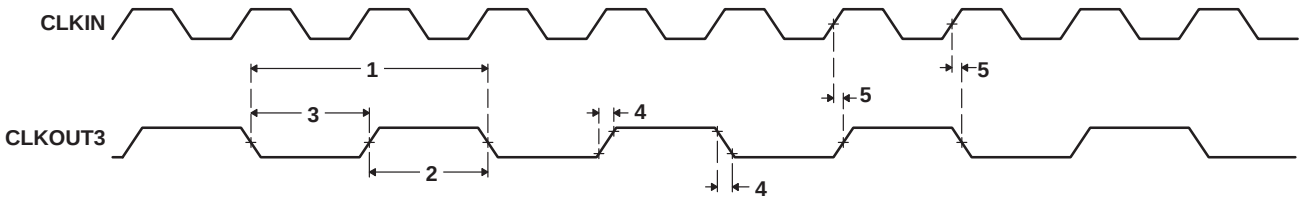


Figure 23. CLKOUT2 Timings

switching characteristics over recommended operating conditions for CLKOUT3†§ (see Figure 24)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{c(CKO3)}$	Cycle time, CLKOUT3	C3 − 0.9	C3 + 0.9	ns
2	$t_{w(CKO3H)}$	Pulse duration, CLKOUT3 high	(C3/2) − 0.9	(C3/2) + 0.9	ns
3	$t_{w(CKO3L)}$	Pulse duration, CLKOUT3 low	(C3/2) − 0.9	(C3/2) + 0.9	ns
4	$t_{t(CKO3)}$	Transition time, CLKOUT3		3	ns
5	$t_{d(CLKINH-CKO3V)}$	Delay time, CLKIN high to CLKOUT3 valid	1.5	7.5	ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
‡ C3 = CLKOUT3 period in ns. CLKOUT3 period is a divide-down of the CPU clock, configurable via the OSCDIV1 register. For more details, see PLL and PLL controller.



NOTE A: For this example, the CLKOUT3 frequency is CLKIN divide-by-2.

Figure 24. CLKOUT3 Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

timing requirements for ECLKIN† (see Figure 25)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{c(EKI)}$	Cycle time, ECLKIN	10		ns
2	$t_{w(EKIH)}$	Pulse duration, ECLKIN high	4.5		ns
3	$t_{w(EKIL)}$	Pulse duration, ECLKIN low	4.5		ns
4	$t_{t(EKI)}$	Transition time, ECLKIN		3	ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

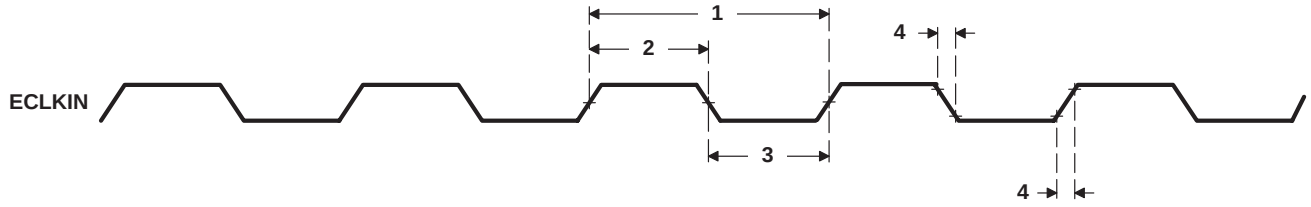


Figure 25. ECLKIN Timings

switching characteristics over recommended operating conditions for ECLKOUT‡§¶ (see Figure 26)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{c(EKO)}$	Cycle time, ECLKOUT	E − 0.9	E + 0.9	ns
2	$t_{w(EKOH)}$	Pulse duration, ECLKOUT high	EH − 0.9	EH + 0.9	ns
3	$t_{w(EKOL)}$	Pulse duration, ECLKOUT low	EL − 0.9	EL + 0.9	ns
4	$t_{t(EKO)}$	Transition time, ECLKOUT		2	ns
5	$t_{d(EKIH-EKOH)}$	Delay time, ECLKIN high to ECLKOUT high	1	6.5	ns
6	$t_{d(EKIL-EKOL)}$	Delay time, ECLKIN low to ECLKOUT low	1	6.5	ns

‡ The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
§ E = ECLKIN period in ns
¶ EH is the high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

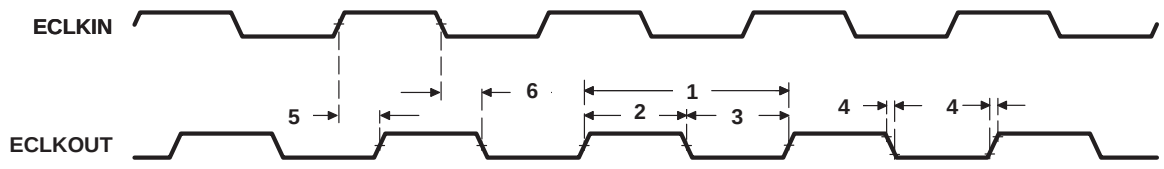


Figure 26. ECLKOUT Timings

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles†‡§ (see Figure 27−Figure 28)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
3	$t_{su(EDV-AREH)}$	Setup time, EDx valid before $\overline{ARE}$ high	6.5		ns
4	$t_{h(AREH-EDV)}$	Hold time, EDx valid after $\overline{ARE}$ high	1		ns
6	$t_{su(ARDY-EKOH)}$	Setup time, ARDY valid before ECLKOUT high	3		ns
7	$t_{h(EKOH-ARDY)}$	Hold time, ARDY valid after ECLKOUT high	2.3		ns

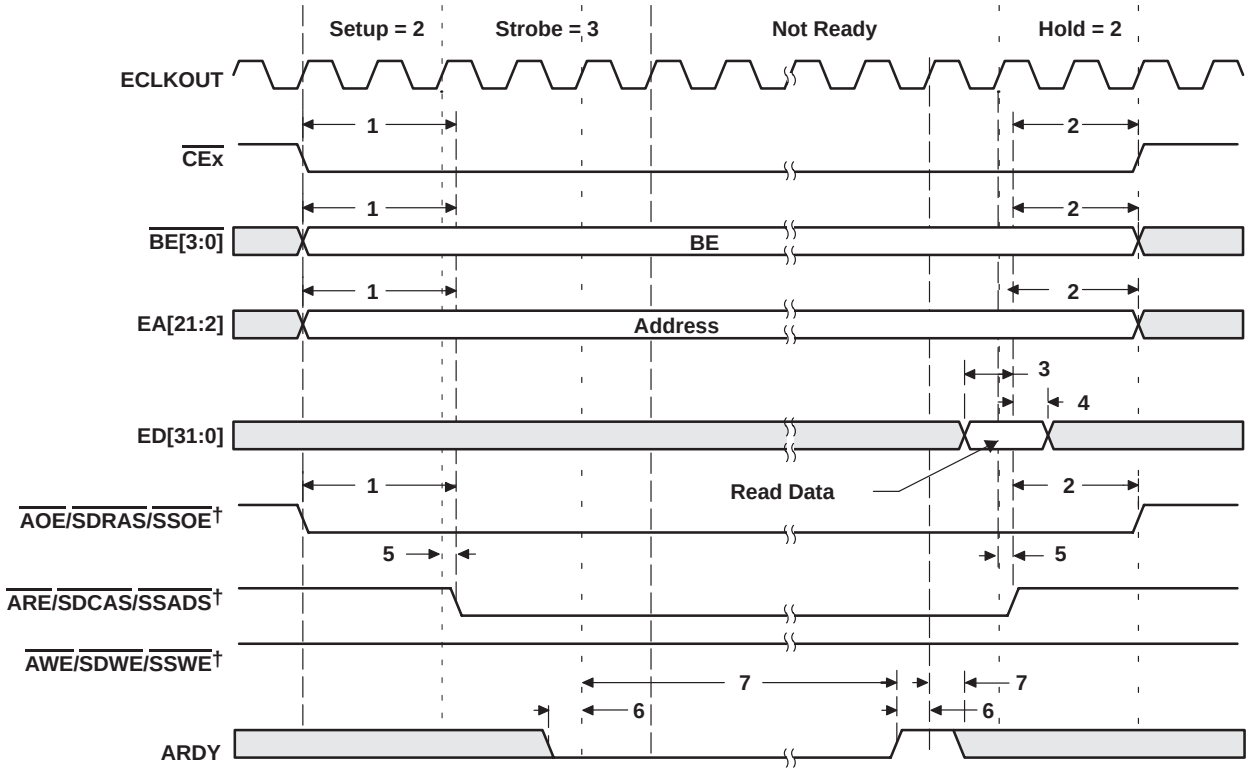
† To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.
‡ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
§ E = ECLKOUT period in ns

switching characteristics over recommended operating conditions for asynchronous memory cycles†‡§ (see Figure 27–Figure 28)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{osu(SELV-AREL)}$	Output setup time, select signals valid to $\overline{ARE}$ low	RS*E − 1.7		ns
2	$t_{oh(AREH-SELIV)}$	Output hold time, $\overline{ARE}$ high to select signals invalid	RH*E − 1.7		ns
5	$t_{d(EKOH-AREV)}$	Delay time, ECLKOUT high to $\overline{ARE}$ valid	1.5	7	ns
8	$t_{osu(SELV-AWEL)}$	Output setup time, select signals valid to $\overline{AWE}$ low	WS*E − 1.7		ns
9	$t_{oh(AWEH-SELIV)}$	Output hold time, $\overline{AWE}$ high to select signals and EDx invalid	WH*E − 1.7		ns
10	$t_{d(EKOH-AWEV)}$	Delay time, ECLKOUT high to $\overline{AWE}$ valid	1.5	7	ns
11	$t_{osu(EDV-AWEL)}$	Output setup time, ED valid to $\overline{AWE}$ low	(WS−1)*E − 1.7		ns

† RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.
‡ E = ECLKOUT period in ns
§ Select signals include: $\overline{CEx}$, $\overline{BE[3:0]}$, EA[21:2], and $\overline{AOE}$.

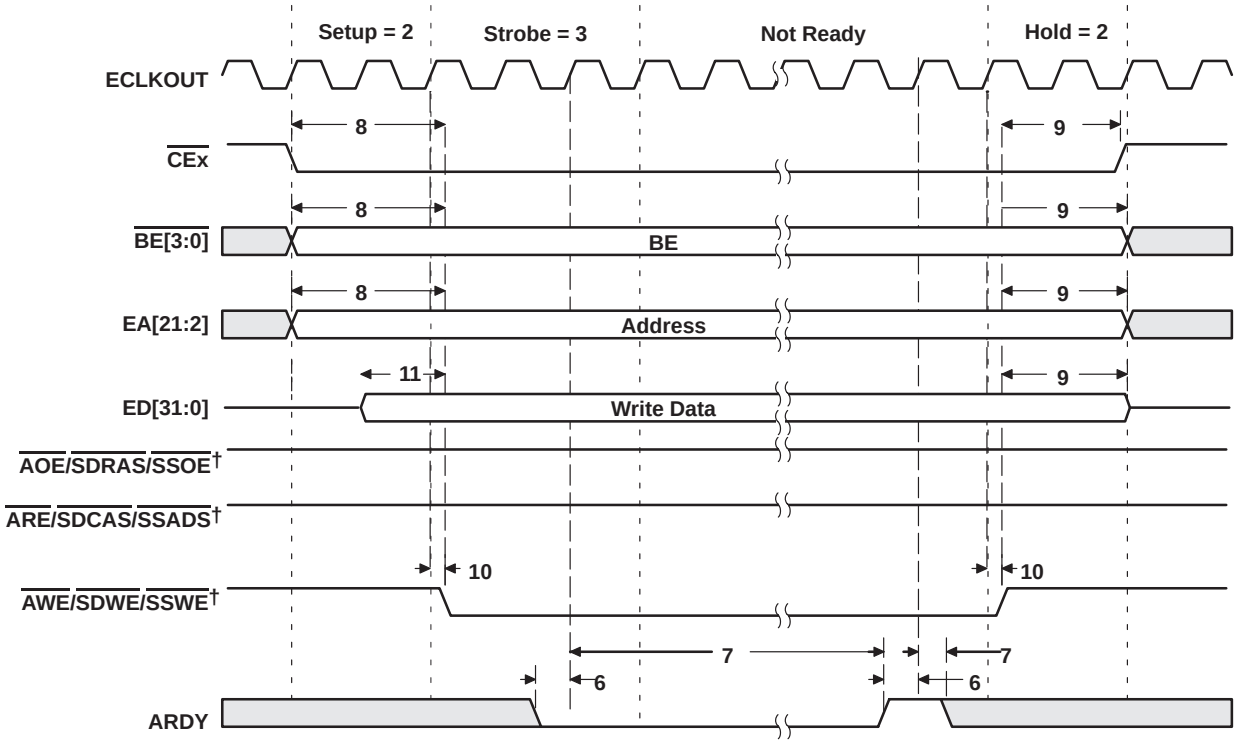
ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

Figure 27. Asynchronous Memory Read Timing

ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

Figure 28. Asynchronous Memory Write Timing

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles† (see Figure 29)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
6	$t_{su(EDV-EKOH)}$	Setup time, read EDx valid before ECLKOUT high	1.5		ns
7	$t_{h(EKOH-EDV)}$	Hold time, read EDx valid after ECLKOUT high	2.5		ns

† The SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

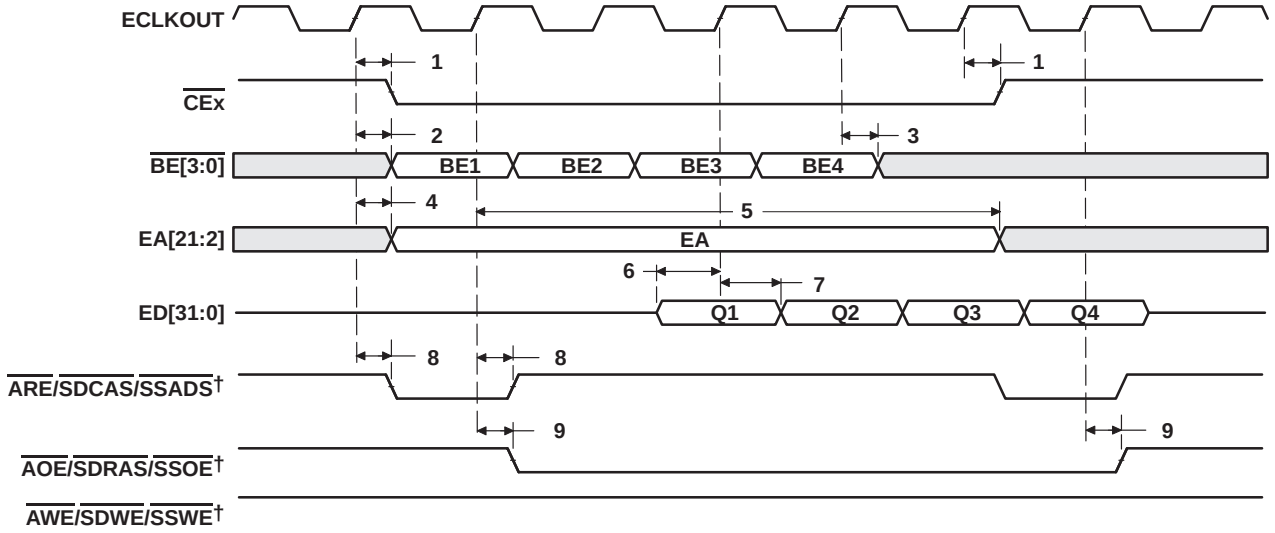
switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles†‡ (see Figure 29 and Figure 30)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{d(EKOH-CEV)}$	Delay time, ECLKOUT high to $\overline{CE}$x valid	1.2	7	ns
2	$t_{d(EKOH-BEV)}$	Delay time, ECLKOUT high to $\overline{BE}$x valid		7	ns
3	$t_{d(EKOH-BEIV)}$	Delay time, ECLKOUT high to $\overline{BE}$x invalid	1.2		ns
4	$t_{d(EKOH-EAV)}$	Delay time, ECLKOUT high to EAx valid		7	ns
5	$t_{d(EKOH-EAIV)}$	Delay time, ECLKOUT high to EAx invalid	1.2		ns
8	$t_{d(EKOH-ADSV)}$	Delay time, ECLKOUT high to $\overline{ARE}$/$\overline{SDCAS}$/$\overline{SSADS}$ valid	1.2	7	ns
9	$t_{d(EKOH-OEV)}$	Delay time, ECLKOUT high to, $\overline{AOE}$/$\overline{SDRAS}$/$\overline{SSOE}$ valid	1.2	7	ns
10	$t_{d(EKOH-EDV)}$	Delay time, ECLKOUT high to $\overline{ED}$x valid		7	ns
11	$t_{d(EKOH-EDIV)}$	Delay time, ECLKOUT high to $\overline{ED}$x invalid	1.2		ns
12	$t_{d(EKOH-WEV)}$	Delay time, ECLKOUT high to $\overline{AWE}$/$\overline{SDWE}$/$\overline{SSWE}$ valid	1.2	7	ns

† The SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

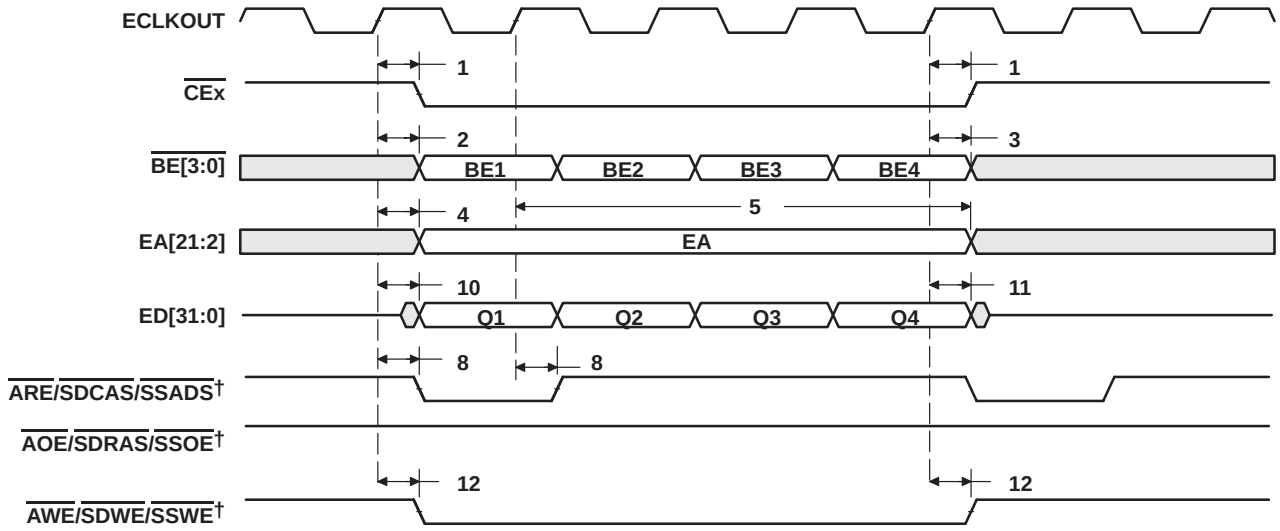
‡ $\overline{ARE}$/$\overline{SDCAS}$/$\overline{SSADS}$, $\overline{AOE}$/$\overline{SDRAS}$/$\overline{SSOE}$, and $\overline{AWE}$/$\overline{SDWE}$/$\overline{SSWE}$ operate as $\overline{SSADS}$, $\overline{SSOE}$, and $\overline{SSWE}$, respectively, during SBSRAM accesses.

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 29. SBSRAM Read Timing



† ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 30. SBSRAM Write Timing

SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles† (see Figure 31)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
6	$t_{su(EDV-EKOH)}$	Setup time, read EDx valid before ECLKOUT high	1.5		ns
7	$t_{h(EKOH-EDV)}$	Hold time, read EDx valid after ECLKOUT high	2.5		ns

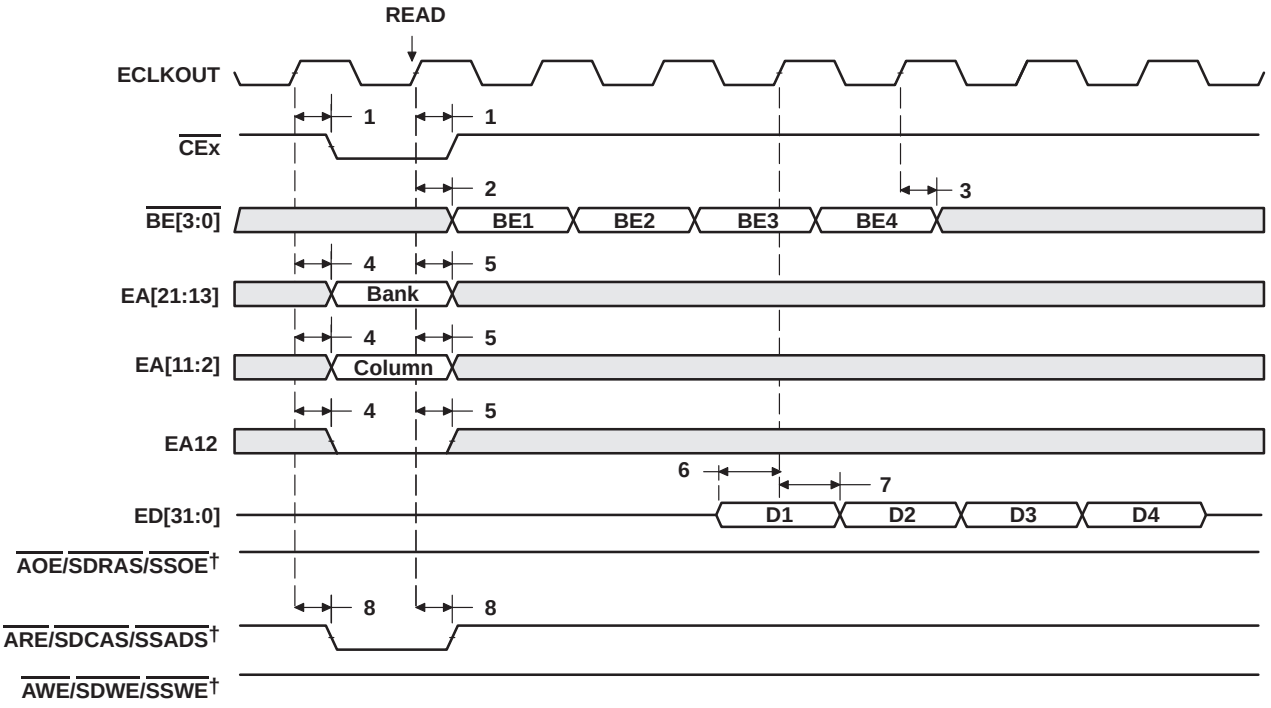
† The SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

switching characteristics over recommended operating conditions for synchronous DRAM cycles†‡ (see Figure 31−Figure 37)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{d(EKOH-CEV)}$	Delay time, ECLKOUT high to $\overline{CEx}$ valid	1.5	7	ns
2	$t_{d(EKOH-BEV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ valid		7	ns
3	$t_{d(EKOH-BEIV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ invalid	1.5		ns
4	$t_{d(EKOH-EAV)}$	Delay time, ECLKOUT high to EAx valid		7	ns
5	$t_{d(EKOH-EAIV)}$	Delay time, ECLKOUT high to EAx invalid	1.5		ns
8	$t_{d(EKOH-CASV)}$	Delay time, ECLKOUT high to $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$ valid	1.5	7	ns
9	$t_{d(EKOH-EDV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ valid		7	ns
10	$t_{d(EKOH-EDIV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ invalid	1.5		ns
11	$t_{d(EKOH-WEV)}$	Delay time, ECLKOUT high to $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ valid	1.5	7	ns
12	$t_{d(EKOH-RAS)}$	Delay time, ECLKOUT high to, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ valid	1.5	7	ns

† The SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

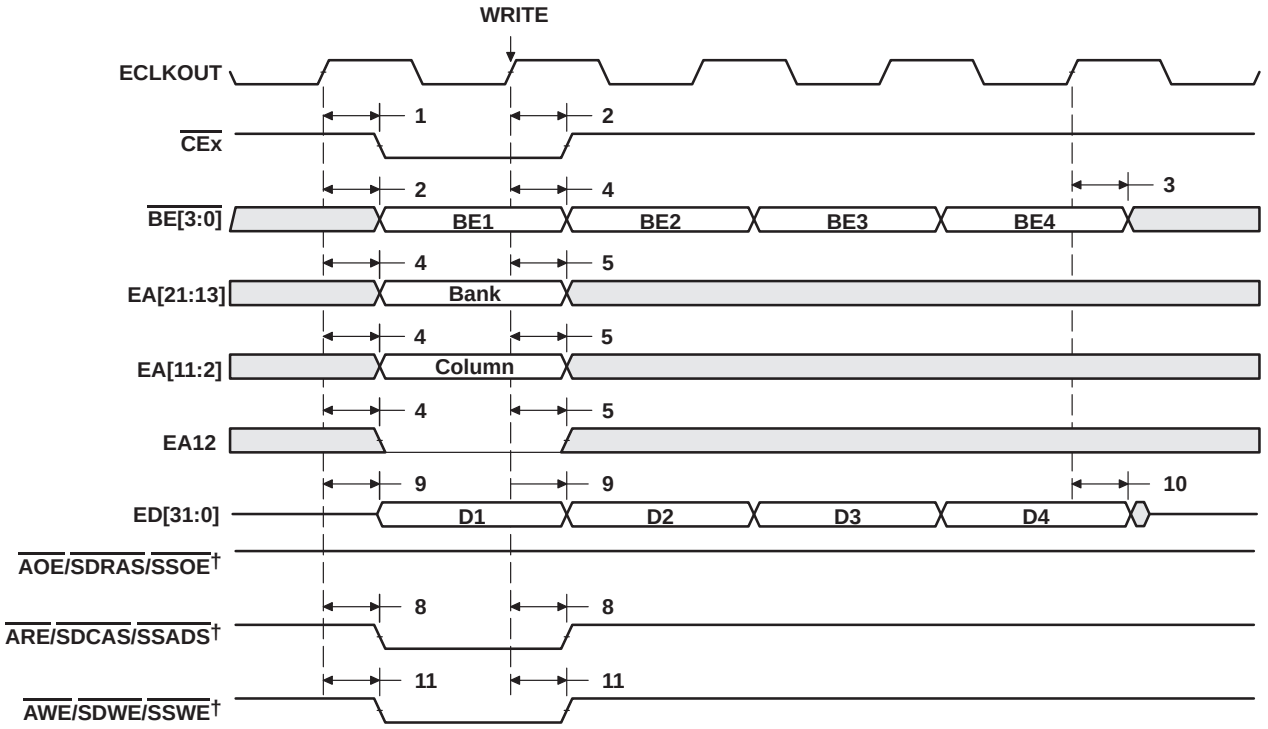
‡ $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$, and $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ operate as $\overline{SDCAS}$, $\overline{SDWE}$, and $\overline{SDRAS}$, respectively, during SDRAM accesses.



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 31. SDRAM Read Command (CAS Latency 3)

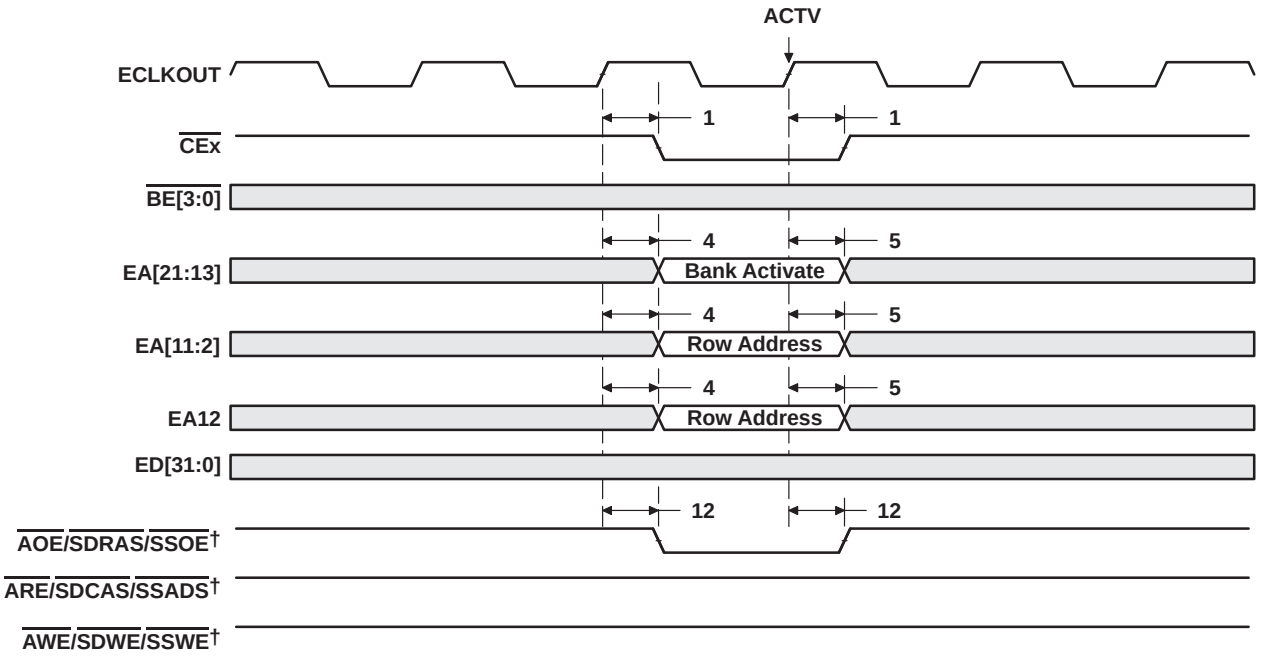
SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

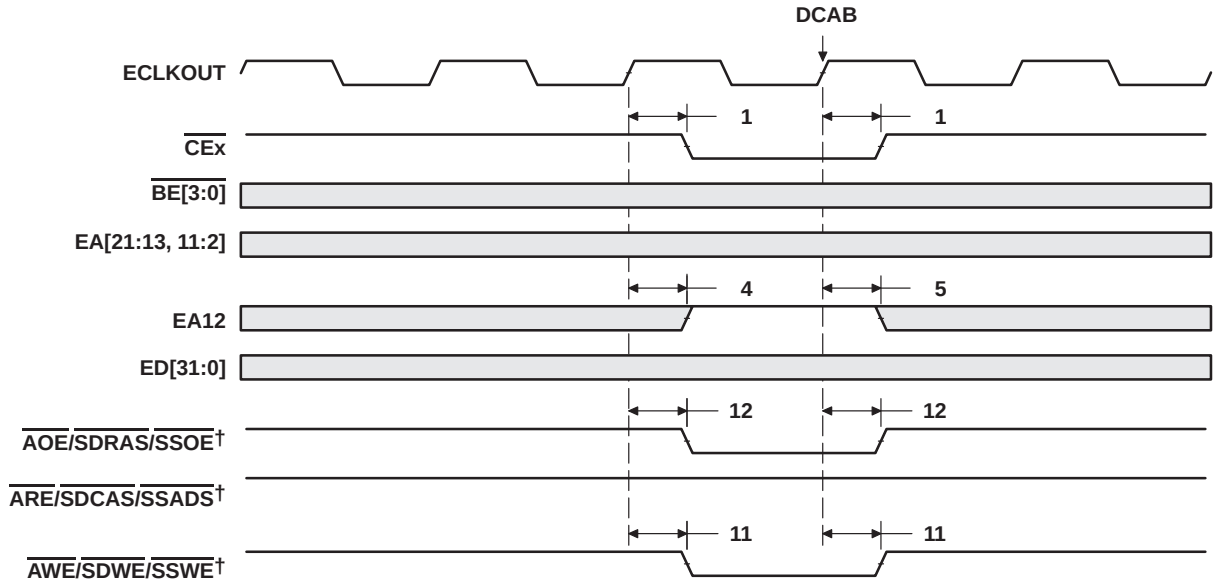
Figure 32. SDRAM Write Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

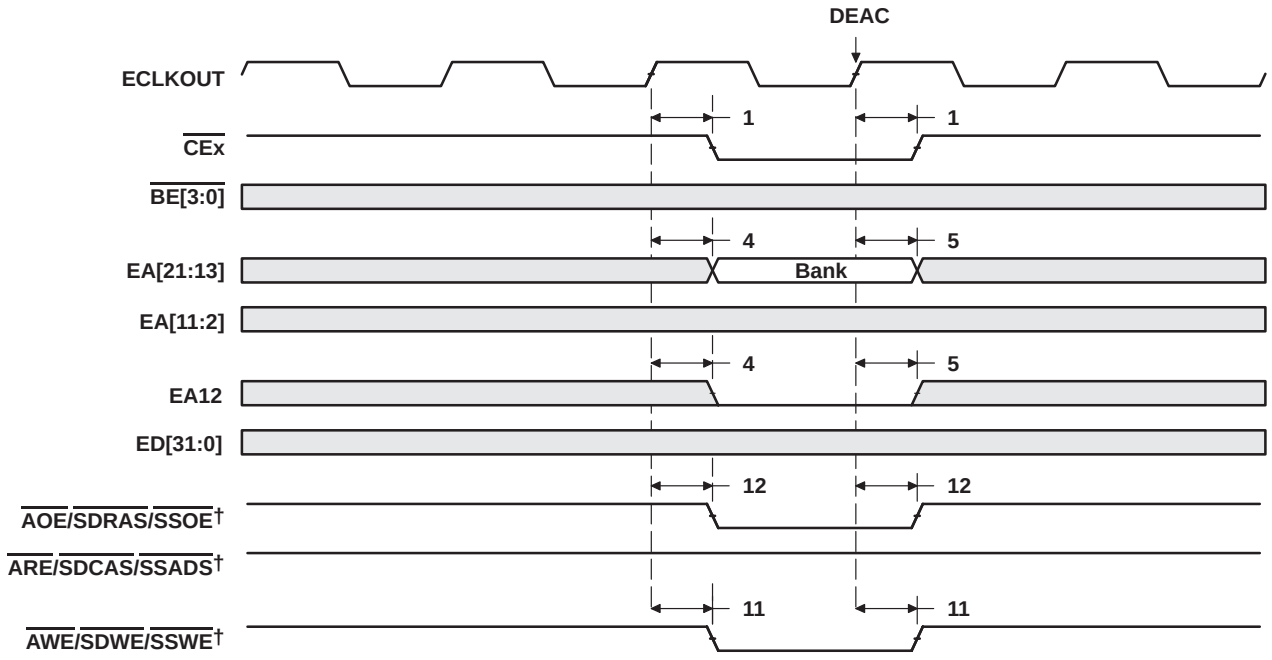
Figure 33. SDRAM ACTV Command



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

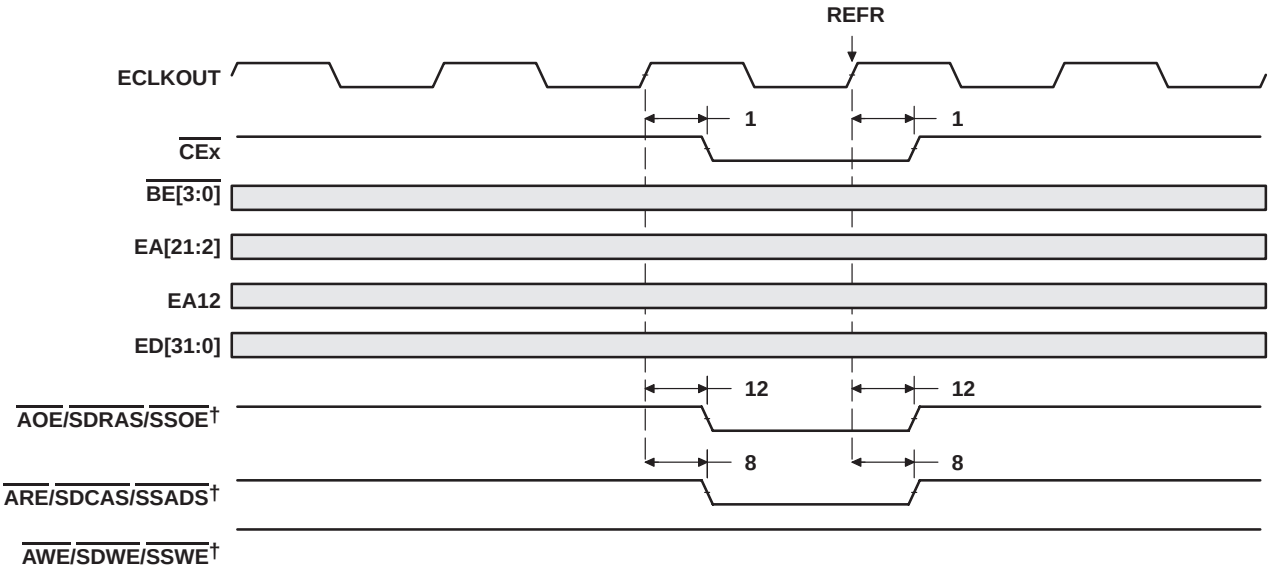
Figure 34. SDRAM DCAB Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

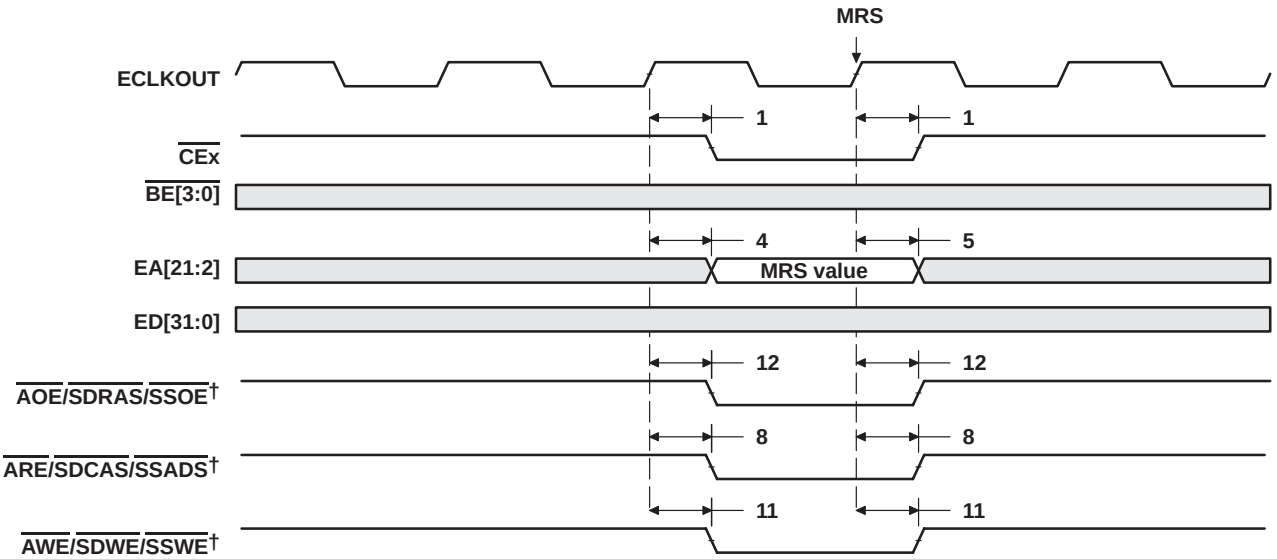
Figure 35. SDRAM DEAC Command



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 36. SDRAM REFR Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 37. SDRAM MRS Command

HOLD/HOLDA TIMING

timing requirements for the HOLD/HOLDA cycles† (see Figure 38)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
3	$t_{h(HOLDAL-HOLDL)}$	Hold time, HOLD low after HOLDA low	E		ns

† E = ECLKIN period in ns

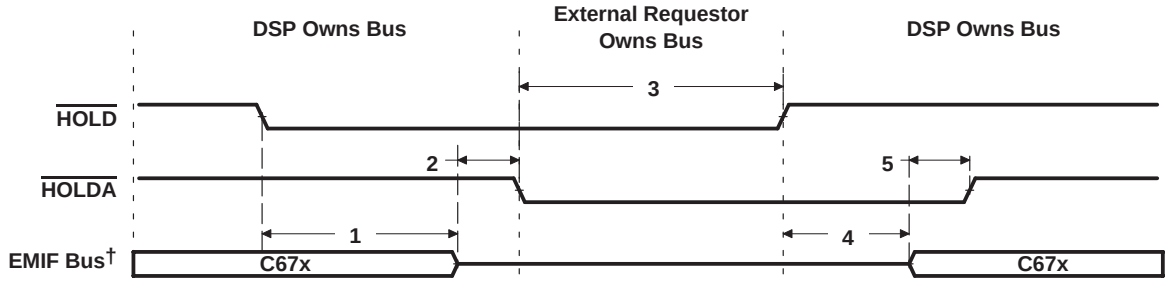
switching characteristics over recommended operating conditions for the HOLD/HOLDA cycles†‡ (see Figure 38)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{d(HOLDL-EMHZ)}$	Delay time, HOLD low to EMIF Bus high impedance	2E	§	ns
2	$t_{d(EMHZ-HOLDAL)}$	Delay time, EMIF Bus high impedance to HOLDA low	0	2E	ns
4	$t_{d(HOLDH-EMLZ)}$	Delay time, HOLD high to EMIF Bus low impedance	2E	7E	ns
5	$t_{d(EMLZ-HOLDAH)}$	Delay time, EMIF Bus low impedance to HOLDA high	0	2E	ns

† E = ECLKIN period in ns

‡ EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.

§ All pending EMIF transactions are allowed to complete before HOLDA is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.



† EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.

Figure 38. HOLD/HOLDA Timing

BUSREQ TIMING

switching characteristics over recommended operating conditions for the BUSREQ cycles (see Figure 39)

NO.	PARAMETER		GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{d(EKOH-BUSRV)}$	Delay time, ECLKOUT high to BUSREQ valid	1.5	7.2	ns

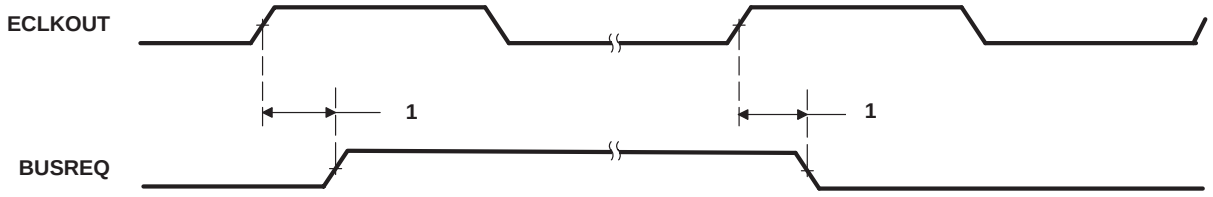


Figure 39. BUSREQ Timing

RESET TIMING

timing requirements for reset†‡ (see Figure 40)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{w(RST)}$	Pulse duration, $\overline{\text{RESET}}$	100		ns
13	$t_{su(HD)}$	Setup time, HD boot configuration bits valid before $\overline{\text{RESET}}$ high§	2P		ns
14	$t_{h(HD)}$	Hold time, HD boot configuration bits valid after $\overline{\text{RESET}}$ high§	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

‡ The PLL is bypassed immediately after the device comes out of reset. The PLL Controller can be programmed to change the PLL mode in software. For more detailed information on the PLL Controller, see the *TMS320C6000 DSP Software-Programmable Phase-Lock Loop (PLL) Controller Reference Guide* (literature number SPRU233).

§ The Boot and device configurations bits are latched asynchronously when RESET is transitioning high. The Boot and device configurations bits consist of: HD[8, 4:3].

switching characteristics over recommended operating conditions during reset¶ (see Figure 40)

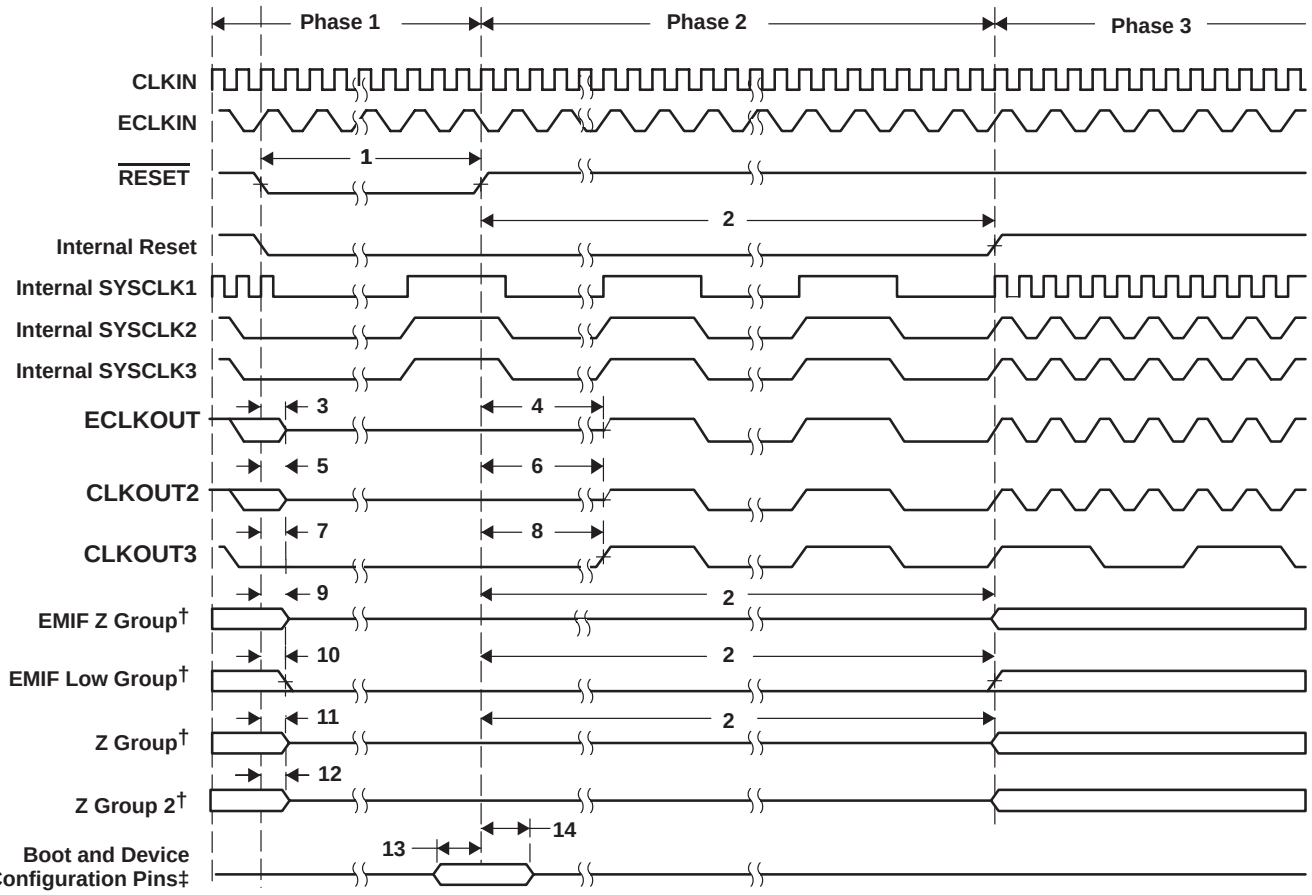
NO.	PARAMETER			GDPA-167 ZDPA−167 −200 −250		UNIT
				MIN	MAX	
2	$t_{d(RSTH-ZV)}$	Delay time, external $\overline{\text{RESET}}$ high to internal reset high and all signal groups valid#‖	CLKMODE0 = 1		512 x CLKIN period	ns
3	$t_{d(RSTL-ECKOL)}$	Delay time, $\overline{\text{RESET}}$ low to ECLKOUT high impedance		0		ns
4	$t_{d(RSTH-ECKOV)}$	Delay time, $\overline{\text{RESET}}$ high to ECLKOUT valid			6P	ns
5	$t_{d(RSTL-CKO2IV)}$	Delay time, $\overline{\text{RESET}}$ low to CLKOUT2 high impedance		0		ns
6	$t_{d(RSTH-CKO2V)}$	Delay time, $\overline{\text{RESET}}$ high to CLKOUT2 valid			6P	ns
7	$t_{d(RSTL-CKO3L)}$	Delay time, $\overline{\text{RESET}}$ low to CLKOUT3 low		0		ns
8	$t_{d(RSTH-CKO3V)}$	Delay time, $\overline{\text{RESET}}$ high to CLKOUT3 valid			6P	ns
9	$t_{d(RSTL-EMIFZHZ)}$	Delay time, $\overline{\text{RESET}}$ low to EMIF Z group high impedance‖		0		ns
10	$t_{d(RSTL-EMIFLIV)}$	Delay time, $\overline{\text{RESET}}$ low to EMIF low group (BUSREQ) invalid‖		0		ns
11	$t_{d(RSTL-Z1HZ)}$	Delay time, $\overline{\text{RESET}}$ low to Z group 1 high impedance‖		0		ns
12	$t_{d(RSTL-Z2HZ)}$	Delay time, $\overline{\text{RESET}}$ low to Z group 2 high impedance‖		0		ns

¶ P = 1/CPU clock frequency in ns.
Note that while internal reset is asserted low, the CPU clock (SYSCLK1) period is equal to the input clock (CLKIN) period multiplied by 8. For example, if the CLKIN period is 20 ns, then the CPU clock (SYSCLK1) period is 20 ns x 8 = 160 ns. Therefore, P = SYSCLK1 = 160 ns while internal reset is asserted.

The internal reset is stretched exactly 512 x CLKIN cycles if CLKIN is used (CLKMODE0 = 1). If the input clock (CLKIN) is not stable when RESET is deasserted, the actual delay time may vary.

‖ EMIF Z group consists of: EA[21:2], ED[31:0], $\overline{\text{CE}}$[3:0], $\overline{\text{BE}}$[3:0], $\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/$\overline{\text{SSADS}}$, $\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/$\overline{\text{SSWE}}$, $\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/$\overline{\text{SSOE}}$ and $\overline{\text{HOLDA}}$
EMIF low group consists of: BUSREQ
Z group 1 consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.
Z group 2 consists of: All other HPI and GPIO signals

RESET TIMING (CONTINUED)



† EMIF Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, AOE/SDRAS/SSOE and HOLDA
EMIF low group consists of: BUSREQ
Z group 1 consists of: CLKR0, CLKR1, CLKX0, CLKX1, FSR0, FSR1, FSX0, FSX1, DX0, DX1, TOUT0, and TOUT1.
Z group 2 consists of: All other HPI and GPIO signals
‡ Boot and device configurations consist of: HD[8, 4:3].

Figure 40. Reset Timing

Reset Phase 1: The RESET pin is asserted. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 2: The RESET pin is deasserted but the internal reset is stretched. During this time, all internal clocks are running at the CLKIN frequency divide-by-8. The CPU is also running at the CLKIN frequency divide-by-8.

Reset Phase 3: Both the RESET pin and internal reset are deasserted. During this time, all internal clocks are running at their default divide-down frequency of CLKIN. The CPU clock (SYSCLK1) is running at CLKIN frequency. The peripheral clock (SYSCLK2) is running at CLKIN frequency divide-by-2. The EMIF internal clock source (SYSCLK3) is running at CLKIN frequency divide-by-2. SYSCLK3 is reflected on the ECLKOUT pin (when EKSRC bit = 0 [default]). CLKOUT3 is running at CLKIN frequency divide-by-8.

EXTERNAL INTERRUPT TIMING

timing requirements for external interrupts† (see Figure 41)

NO.			GDPA-167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{w(ILOW)}$	Width of the NMI interrupt pulse low	2P		ns
		Width of the EXT_INT interrupt pulse low	4P		ns
2	$t_{w(IHIGH)}$	Width of the NMI interrupt pulse high	2P		ns
		Width of the EXT_INT interrupt pulse high	4P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

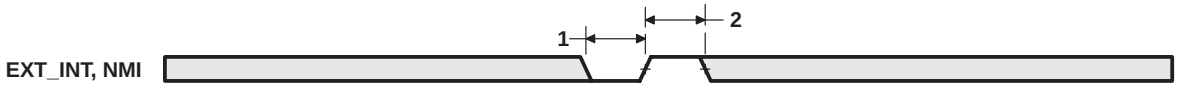


Figure 41. External/NMI Interrupt Timing

HOST-PORT INTERFACE TIMING

timing requirements for host-port interface cycles†‡ (see Figure 42, Figure 43, Figure 44, and Figure 45)

NO.			GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before $\overline{\text{HSTROBE}}$ low	5		ns
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after $\overline{\text{HSTROBE}}$ low	4		ns
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{\text{HSTROBE}}$ low (host **read** access)	4P		ns
		Pulse duration, $\overline{\text{HSTROBE}}$ low (host **write** access)	4P		ns
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses	4P		ns
10	$t_{su(SELV-HASL)}$	Setup time, select signals§ valid before $\overline{\text{HAS}}$ low	5		ns
11	$t_{h(HASL-SELV)}$	Hold time, select signals§ valid after $\overline{\text{HAS}}$ low	3		ns
12	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	5		ns
13	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	3		ns
14	$t_{h(HRDYL-HSTBL)}$	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	2		ns
18	$t_{su(HASL-HSTBL)}$	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	2		ns
19	$t_{h(HSTBL-HASL)}$	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	2		ns

† $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
§ Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$, and HHWIL.

HOST-PORT INTERFACE TIMING (CONTINUED)

switching characteristics over recommended operating conditions during host-port interface cycles†‡ (see Figure 42, Figure 43, Figure 44, and Figure 45)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
5	$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ to $\overline{HRDY}$§	1	12	ns
6	$t_{d(HSTBL-HRDYH)}$	Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ high¶	3	12	ns
7	$t_{d(HSTBL-HDLZ)}$	Delay time, $\overline{HSTROBE}$ low to HD low impedance for an HPI read	2		ns
8	$t_{d(HDV-HRDYL)}$	Delay time, HD valid to $\overline{HRDY}$ low	2P − 4		ns
9	$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after $\overline{HSTROBE}$ high	3	12	ns
15	$t_{d(HSTBH-HDHZ)}$	Delay time, $\overline{HSTROBE}$ high to HD high impedance	3	12	ns
16	$t_{d(HSTBL-HDV)}$	Delay time, $\overline{HSTROBE}$ low to HD valid	3	12.5	ns
17	$t_{d(HSTBH-HRDYH)}$	Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ high#	3	12	ns

† $\overline{HSTROBE}$ refers to the following logical operation on $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$: [NOT($\overline{HDS1}$ XOR $\overline{HDS2}$)] OR $\overline{HCS}$.

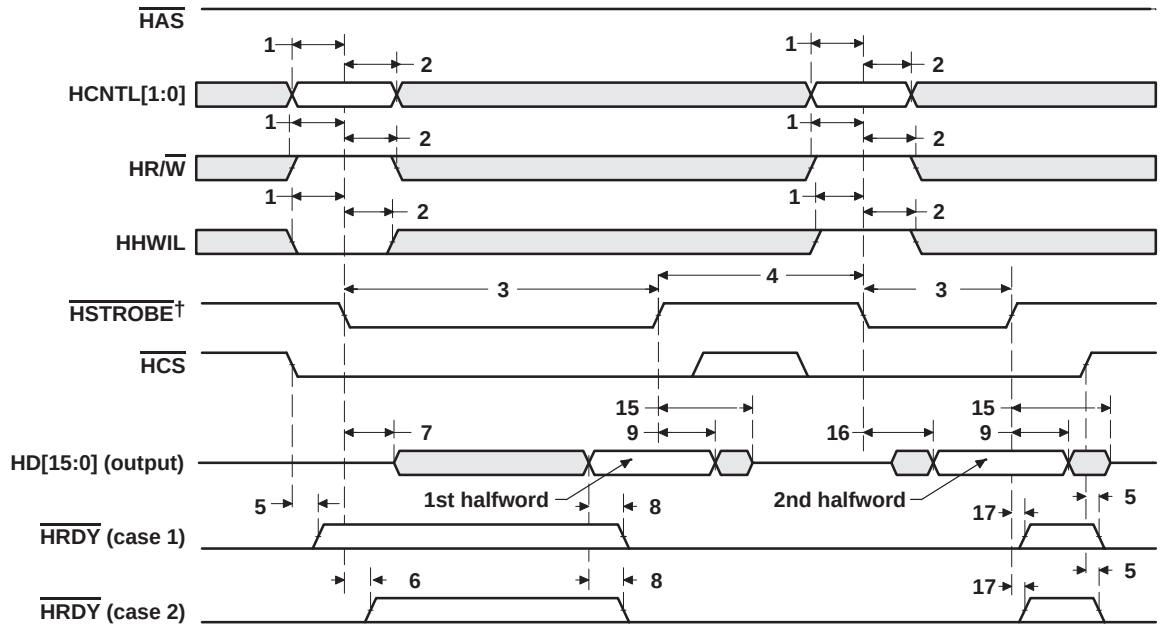
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

§ $\overline{HCS}$ enables $\overline{HRDY}$, and $\overline{HRDY}$ is always low when $\overline{HCS}$ is high. The case where $\overline{HRDY}$ goes high when $\overline{HCS}$ falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

¶ This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of $\overline{HSTROBE}$, the HPI sends the request to the EDMA internal address generation hardware, and $\overline{HRDY}$ remains high until the EDMA internal address generation hardware loads the requested data into HPID.

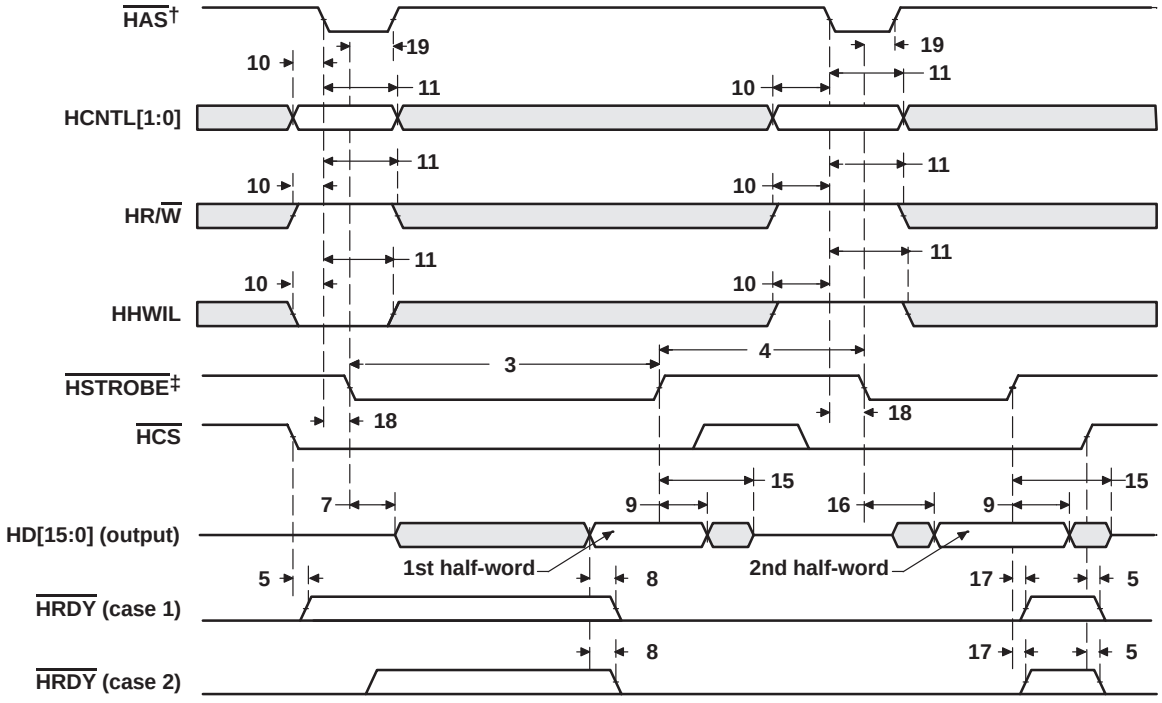
This parameter is used after the second half-word of an HPID write or autoincrement read. $\overline{HRDY}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{HRDY}$ signal.

HOST-PORT INTERFACE TIMING (CONTINUED)



† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 42. HPI Read Timing (HAS Not Used, Tied High)



† For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
‡ HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 43. HPI Read Timing (HAS Used)

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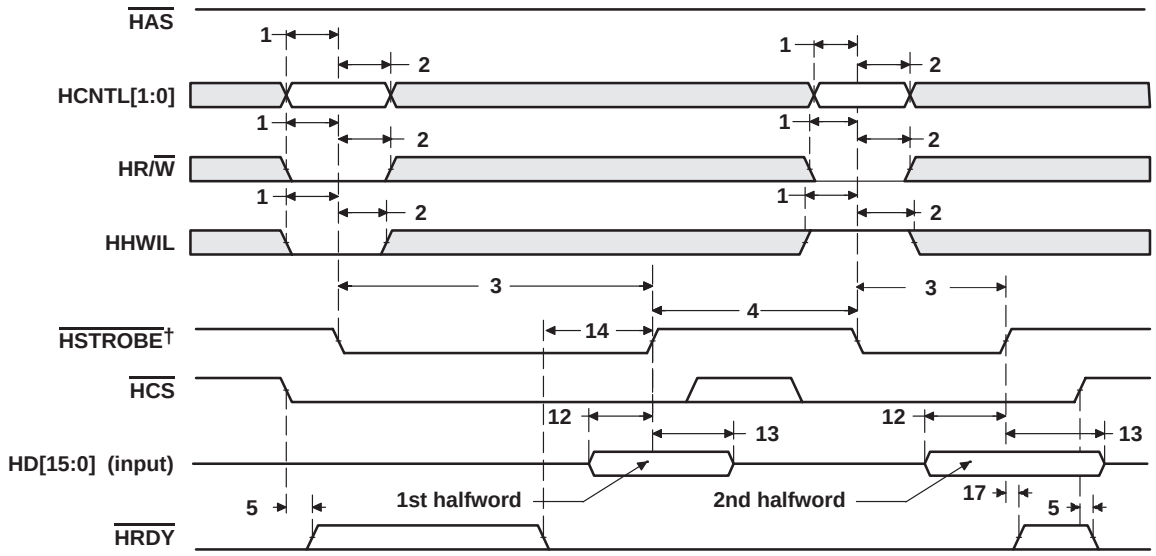
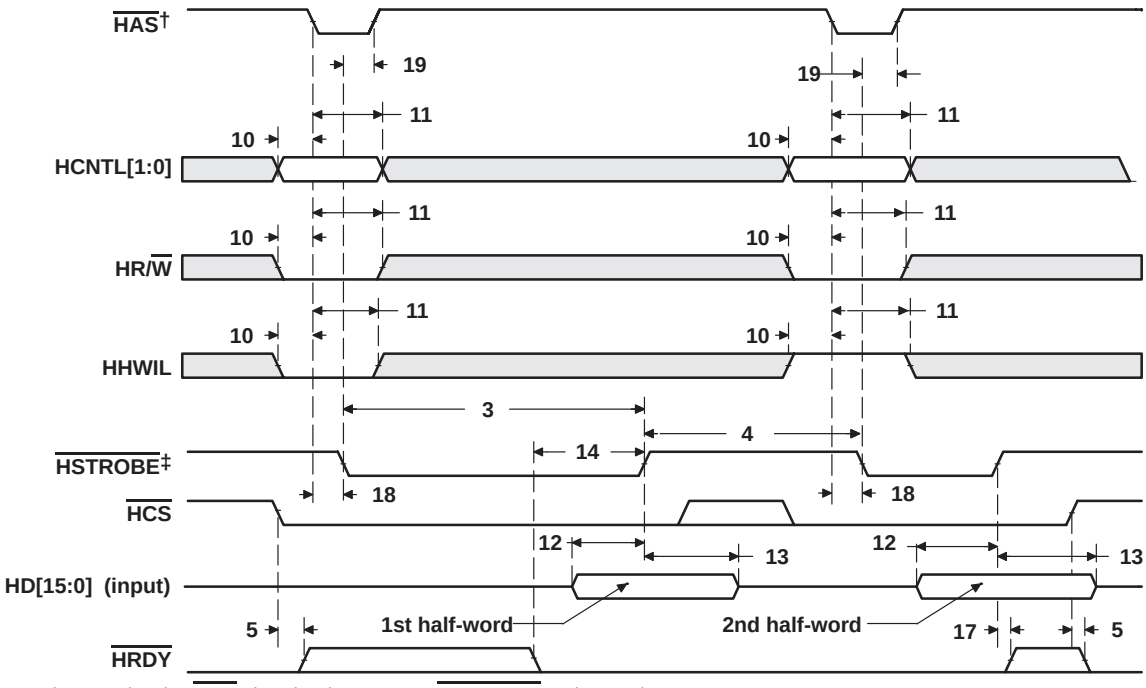
HOST-PORT INTERFACE TIMING (CONTINUED)



† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 44. HPI Write Timing (HAS Not Used, Tied High)



† For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
‡ HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 45. HPI Write Timing (HAS Used)

MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP†‡ (see Figure 46)

NO.				GDPA−167 ZDPA−167 −200 −250		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P§		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	0.5*$t_{c(CKRX)}$ −1¶		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	9		ns
			CLKR ext	1		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	6		ns
			CLKR ext	3		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	8		ns
			CLKR ext	0		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	3		ns
			CLKR ext	4		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	9		ns
			CLKX ext	1		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	6		ns
			CLKX ext	3		

† CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

§ The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 200-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 167 MHz (P = 6 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

¶ This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP†‡ (see Figure 46)

NO.	PARAMETER			GDPA−167 ZDPA−167 −200 −250		UNIT
				MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input		1.8	10	ns
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	2P§¶		ns
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C − 1#	C + 1#	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	−2	3	ns
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	−2	3	ns
			CLKX ext	2	9	
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	−1	4	ns
			CLKX ext	1.5	10	
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	−3.2 + D1‖	4 + D2‖	ns
			CLKX ext	0.5 + D1‖	10+ D2‖	
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int	−1	7.5	ns
			FSX ext	2	11.5	

† CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ Minimum delay times also represent minimum output hold times.

§ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

¶ The minimum CLKR/X period is twice the CPU cycle time (2P) and not faster than 75 Mbps (13.3 ns). This means that the maximum bit rate for communications between the McBSP and other devices is 75 Mbps for 167-MHz and 200-MHz CPU clocks or 50 Mbps for 100-MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 67 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 15 ns (67 MHz), whichever value is larger. For example, when running parts at 167 MHz (P = 6 ns), use 15 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

# C = H or L
S = sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see ¶ footnote above).

‖ Extra delay from CLKX high to DX valid applies *only* to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 2P, D2 = 4P

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

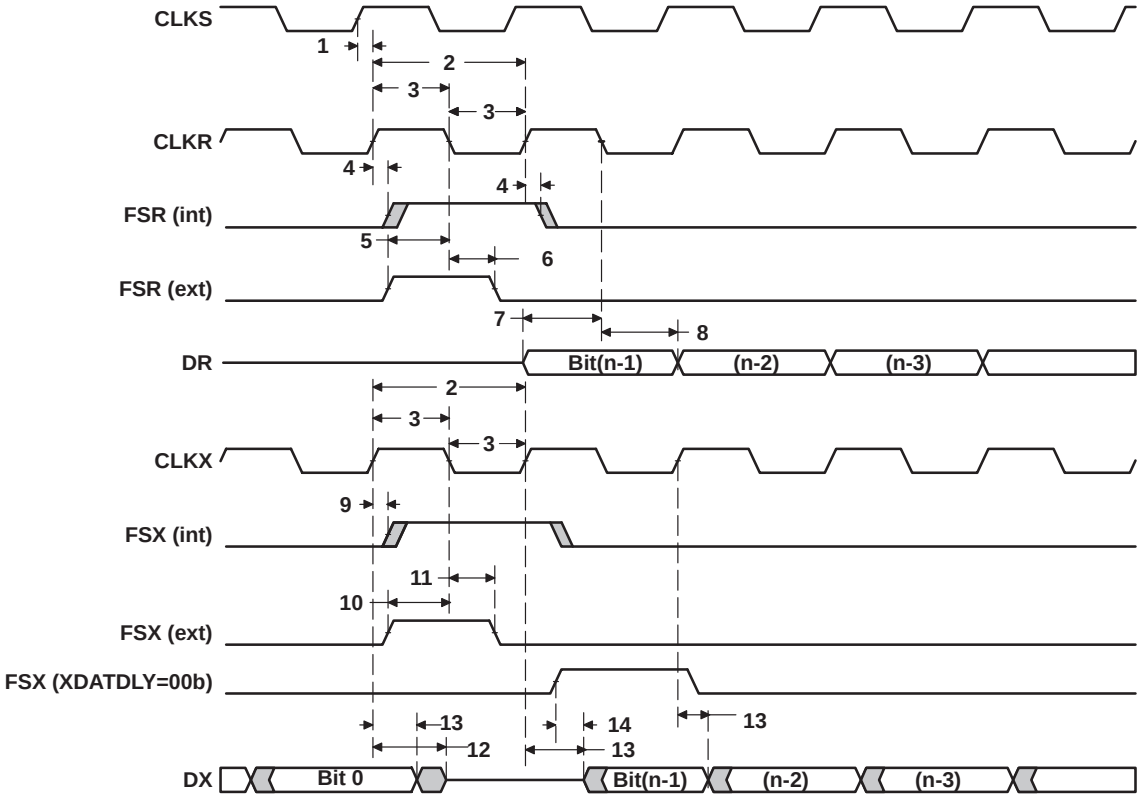


Figure 46. McBSP Timings

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for FSR when GSYNC = 1 (see Figure 47)

NO.			GDPA−167, ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high	4		ns
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high	4		ns

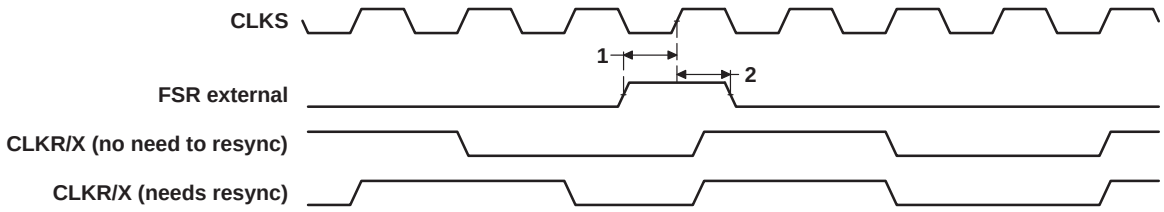


Figure 47. FSR Timing When GSYNC = 1

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 48)

NO.			GDPA−167, ZDPA−167 −200 −250				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	12		2 − 6P		ns
5	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 48)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	T − 2	T + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	L − 2	L + 3			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	L − 2	L + 3			ns
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			2P + 3	6P + 17	ns
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

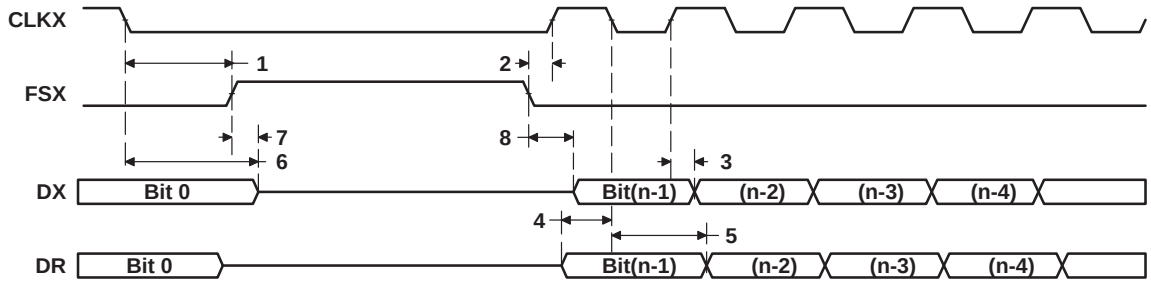


Figure 48. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 49)

NO.			GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 49)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	L − 2	L + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	T − 2	T + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	H − 2	H + 6.5	4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

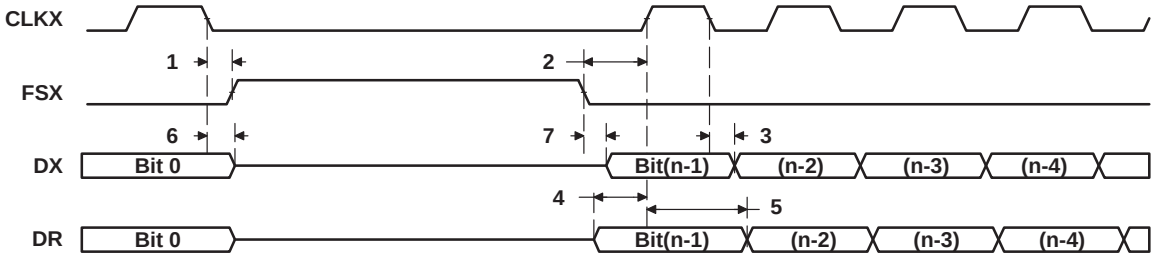


Figure 49. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 50)

NO.		GDPA-167 ZDPA−167 −200 −250				UNIT
		MASTER		SLAVE		
		MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$ Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 50)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶	T − 2	T + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	H − 2	H + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	H − 2	H + 3			ns
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			2P + 3	6P + 17	ns
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

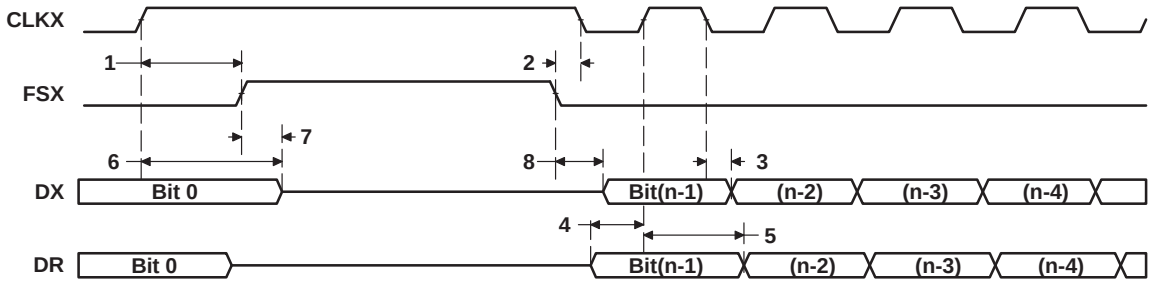


Figure 50. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 51)

NO.			GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 51)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶	H − 2	H + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	T − 2	T + 3			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	L − 2	L + 6.5	4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

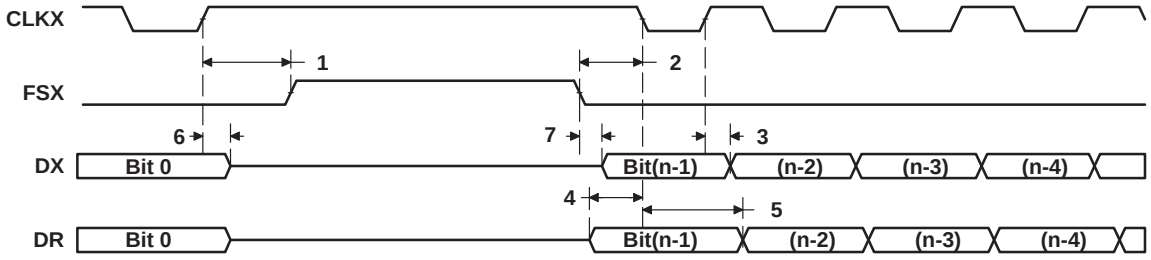


Figure 51. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

TIMER TIMING

timing requirements for timer inputs† (see Figure 52)

NO.			GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{w(TINPH)}$	Pulse duration, TINP high	2P		ns
2	$t_{w(TINPL)}$	Pulse duration, TINP low	2P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

switching characteristics over recommended operating conditions for timer outputs† (see Figure 52)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
3	$t_{w(TOUTH)}$	Pulse duration, TOUT high	4P − 3		ns
4	$t_{w(TOUTL)}$	Pulse duration, TOUT low	4P − 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.

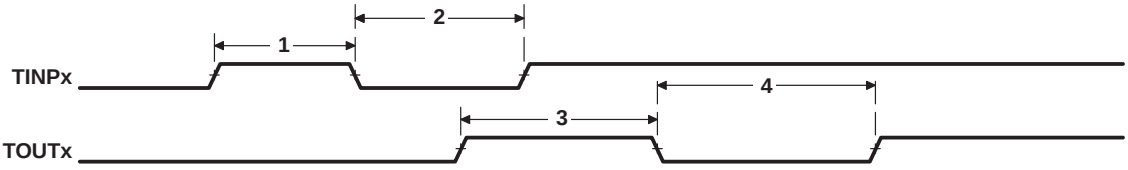


Figure 52. Timer Timing

GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING

timing requirements for GPIO inputs†‡ (see Figure 53)

NO.			GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	4P		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	4P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
‡ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the DSP recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to at least 24P to allow the DSP enough time to access the GPIO register through the CFGBUS.

switching characteristics over recommended operating conditions for GPIO outputs†§ (see Figure 53)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	12P − 3		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	12P − 3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 250 MHz, use P = 4 ns.
§ The number of CFGBUS cycles between two back-to-back CFGBUS writes to the GPIO register is 12 SYSCLK1 cycles; therefore, the minimum GPOx pulse width is 12P.

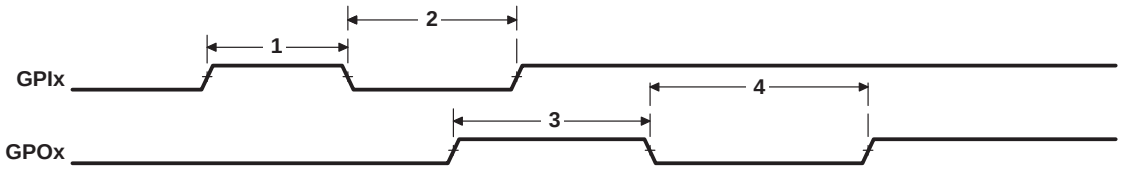


Figure 53. GPIO Port Timing

JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 54)

NO.			GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	35		ns
3	$t_{su(TDIV-TCKH)}$	Setup time, TDI/TMS/$\overline{TRST}$ valid before TCK high	10		ns
4	$t_{h(TCKH-TDIV)}$	Hold time, TDI/TMS/$\overline{TRST}$ valid after TCK high	7		ns

switching characteristics over recommended operating conditions for JTAG test port (see Figure 54)

NO.	PARAMETER		GDPA−167 ZDPA−167 −200 −250		UNIT
			MIN	MAX	
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	15	ns

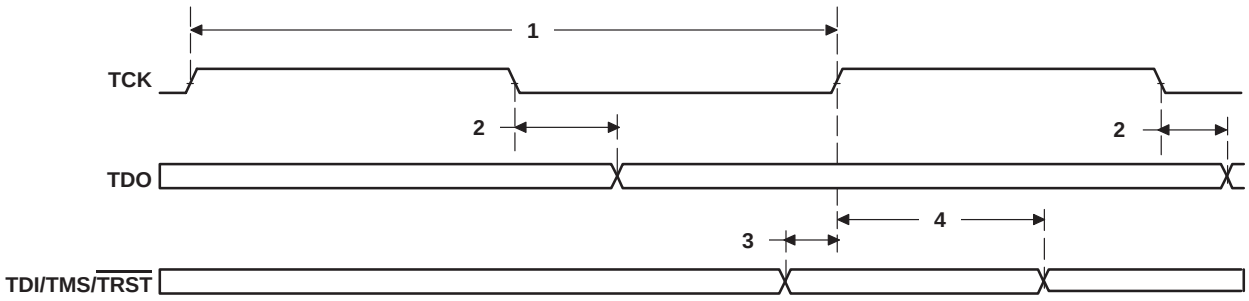


Figure 54. JTAG Test-Port Timing

MECHANICAL DATA

package thermal resistance characteristics

The following tables show the thermal resistance characteristics for the GDP and ZDP mechanical packages.

thermal resistance characteristics (S-PBGA package) for GDP

NO			°C/W	Air Flow (m/s)†
Two Signals, Two Planes (4-Layer Board)				
1	$R\Theta_{JC}$	Junction-to-case	9.7	N/A
2	Psi_{JT}	Junction-to-package top	1.5	0.0
3	$R\Theta_{JB}$	Junction-to-board	19	N/A
4	$R\Theta_{JA}$	Junction-to-free air	22	0.0
5	$R\Theta_{JA}$	Junction-to-free air	21	0.5
6	$R\Theta_{JA}$	Junction-to-free air	20	1.0
7	$R\Theta_{JA}$	Junction-to-free air	19	2.0
8	$R\Theta_{JA}$	Junction-to-free air	18	4.0
9	Psi_{JB}	Junction-to-board	16	0.0

† m/s = meters per second

thermal resistance characteristics (S-PBGA package) for ZDP

NO			°C/W	Air Flow (m/s)†
Two Signals, Two Planes (4-Layer Board)				
1	$R\Theta_{JC}$	Junction-to-case	9.7	N/A
2	Psi_{JT}	Junction-to-package top	1.5	0.0
3	$R\Theta_{JB}$	Junction-to-board	19	N/A
4	$R\Theta_{JA}$	Junction-to-free air	22	0.0
5	$R\Theta_{JA}$	Junction-to-free air	21	0.5
6	$R\Theta_{JA}$	Junction-to-free air	20	1.0
7	$R\Theta_{JA}$	Junction-to-free air	19	2.0
8	$R\Theta_{JA}$	Junction-to-free air	18	4.0
9	Psi_{JB}	Junction-to-board	16	0.0

† m/s = meters per second

packaging information

The following packaging information and addendum reflect the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

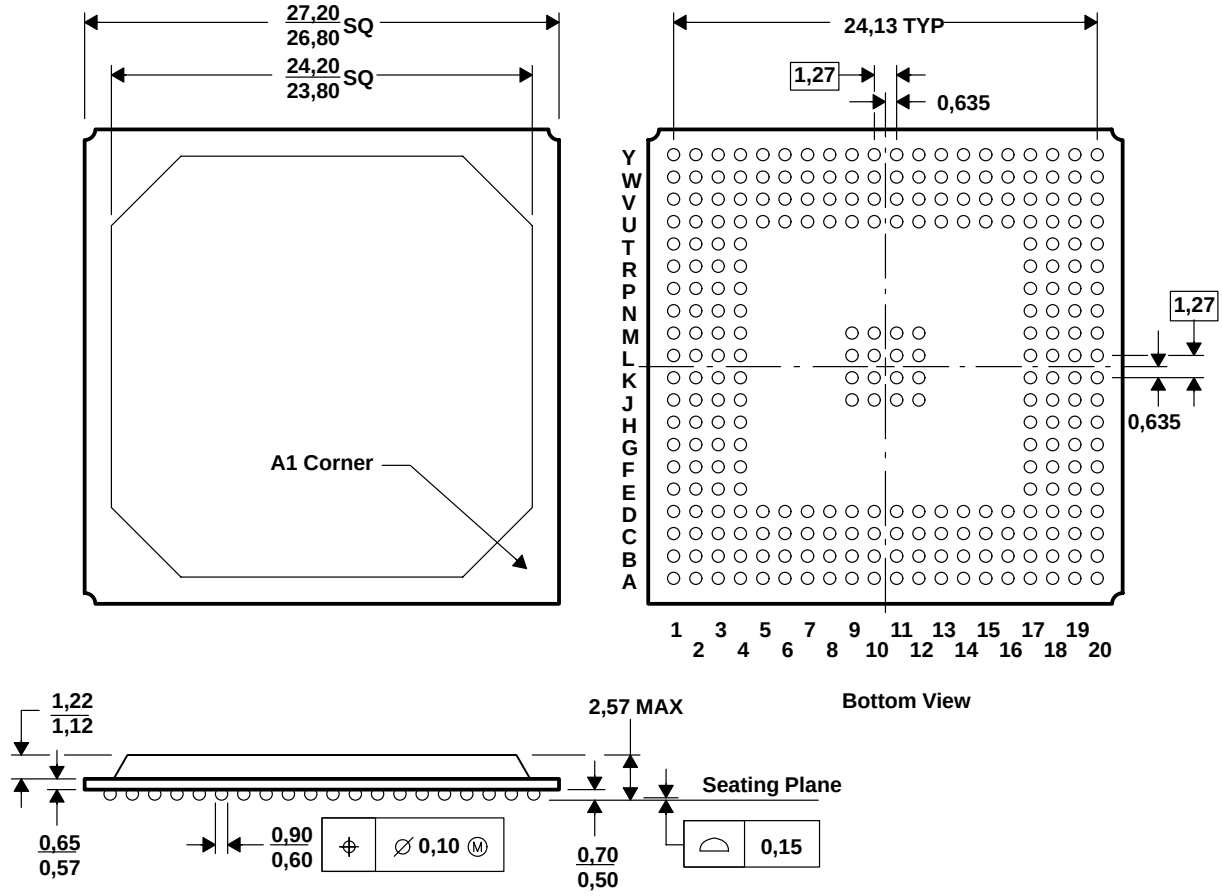
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMS320C6711DGDP200	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168 HR
TMS320C6711DGDP250	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168 HR
TMS320C6711DZDP200	ACTIVE	BGA	ZDP	272	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR
TMS320C6711DZDP250	ACTIVE	BGA	ZDP	272	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR
TMS32C6711DGDPA167	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168 HR
TMS32C6711DZDPA167	ACTIVE	BGA	ZDP	272	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZDP (S–PBGA–N272) **PLASTIC BALL GRID ARRAY**



4204398/A 04/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151
D. This package is lead-free.

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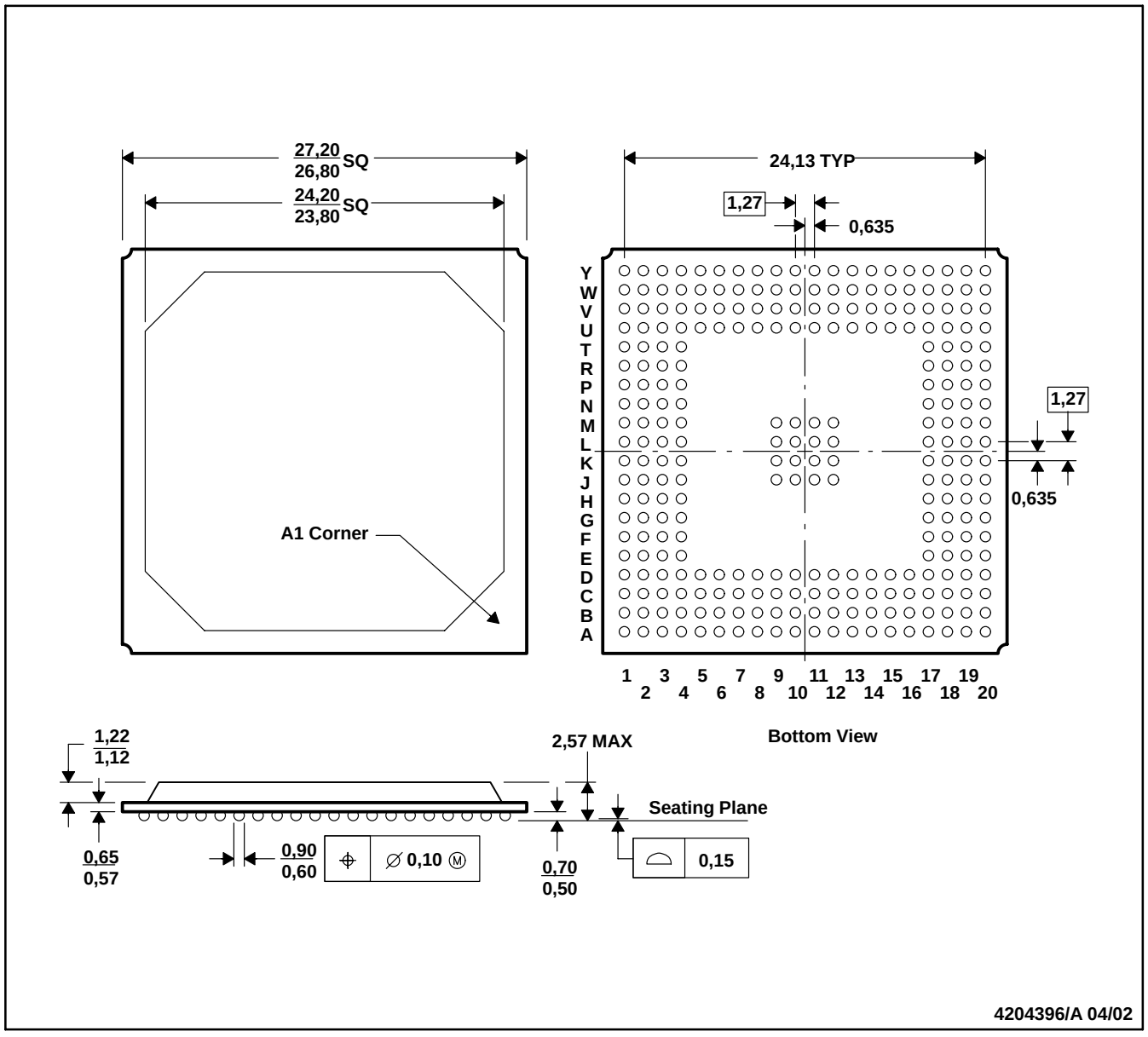
GDP (S–PBGA–N272) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151

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