

Silicon diffused power transistors

BUT12; BUT12A

High-voltage, high-speed, glass-passivated npn power transistors in a TO220 envelope intended for use in converters, inverters, switching regulators, motor control systems, etc.

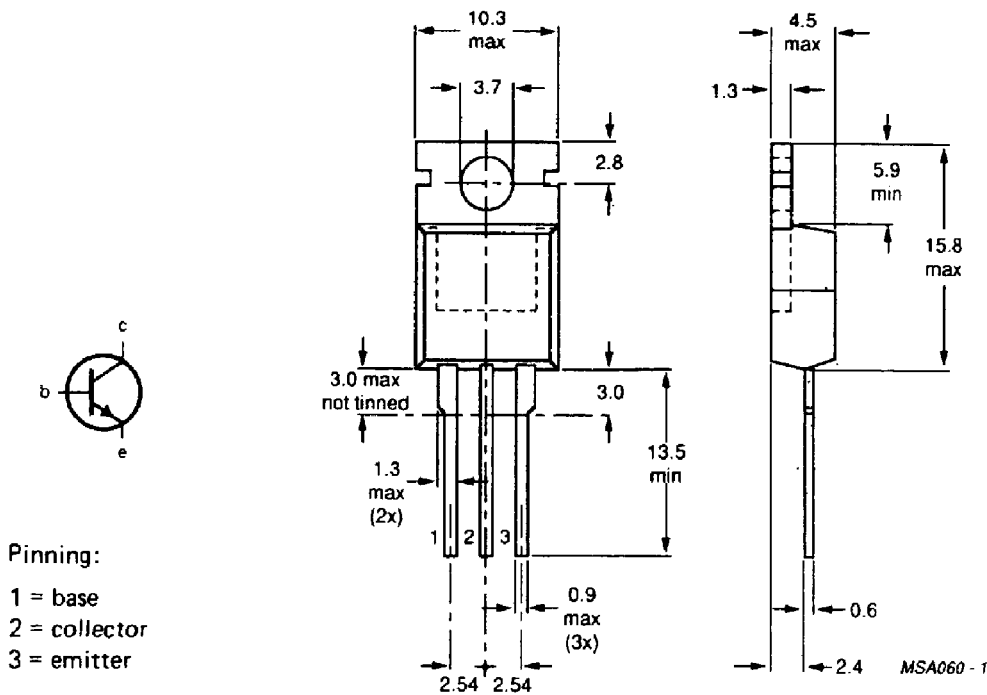
QUICK REFERENCE DATA

		BUT12	BUT12A
Collector-emitter voltage			
peak value; $V_{BE} = 0$	$V_{CESM}$	max. 850	1000 V
open base	$V_{CEO}$	max. 400	450 V
Collector-emitter saturation voltage	$V_{CEsat}$	max. 1.5	1.5 V
Collector current			
saturation	$I_{Csat}$	max. 6.0	5.0 A
DC	$I_C$	max. 8	A
peak value	$I_{CM}$	max. 20	A
Total power dissipation			
up to $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max. 125	W
Fall time	$t_f$	max. 0.8	$\mu\text{s}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO220AB.



Collector connected to mounting base.

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## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		BUT12		BUT12A	
Collector-emitter voltage peak value; $V_{BE} = 0$ open base	$V_{CESM}$	max.	850	1000 V	
	$V_{CEO}$	max.	400	450 V	
Collector current saturation DC peak value	$I_{Csat}$		6.0	5.0 A	
	$I_C$	max.		8	A
	$I_{CM}$	max.		20	A
Base current DC peak value	$I_B$	max.	4.0	A	
	$I_{BM}$	max.	6.0	A	
Total power dissipation up to $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125	W	
Storage temperature range	$T_{stg}$		-65 to +150 $^\circ\text{C}$		
Junction temperature	$T_j$	max.	150	$^\circ\text{C}$	
<b>THERMAL RESISTANCE</b>					
From junction to mounting base	$R_{th\ j-mb}$	=	1.0	K/W	

## CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Collector cut-off currents\*

 $V_{CE} = V_{CESmax}; V_{BE} = 0$  $V_{CE} = V_{CESmax}; V_{BE} = 0; T_j = 125\text{ }^\circ\text{C}$ 

Emitter cut-off current

 $V_{EB} = 9\text{ V}; I_C = 0$ 

$I_{CES}$	max.	1.0	mA	
$I_{CES}$	max.	3.0	mA	
$I_{EBO}$	max.	10	mA	

\* Measured with a half-sinewave voltage (curve tracer).

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<b>Saturation voltages</b>				
$I_C = 6 \text{ A}; I_B = 1.2 \text{ A}$	$V_{CEsat}$	max.	1.5	— V
	$V_{BEsat}$	max.	1.5	— V
$I_C = 5 \text{ A}; I_B = 1.0 \text{ A}$	$V_{CEsat}$	max.	—	1.5 V
	$V_{BEsat}$	max.	—	1.5 V
<b>DC current gain</b>				
$I_C = 10 \text{ mA}; V_{CE} = 5 \text{ V}$	$h_{FE}$	min.	10	
	$h_{FE}$	typ.	18	
	$h_{FE}$	max.	35	
$I_C = 1 \text{ A}; V_{CE} = 5 \text{ V}$	$h_{FE}$	min.	10	
	$h_{FE}$	typ.	20	
	$h_{FE}$	max.	35	
<b>Collector-emitter sustaining voltage</b> (Figs 2 and 3)				
$I_C = 100 \text{ mA}; I_{B \text{ off}} = 0; L = 25 \text{ mH}$	$V_{CEOsust}$	min.	400	450 V
<b>Switching times resistive load</b> (Figs 4 and 5)				
$I_{C \text{ on}} = 6 \text{ A}; I_{B \text{ on}} = -I_{B \text{ off}} = 1.2 \text{ A}$				
<b>Turn-on time</b>	$t_{on}$	max.	1.0	— $\mu\text{s}$
<b>Turn-off;</b>				
<b>storage time</b>	$t_s$	max.	4.0	— $\mu\text{s}$
<b>fall time</b>	$t_f$	max.	0.8	— $\mu\text{s}$
$I_{C \text{ on}} = 5 \text{ A}; I_{B \text{ on}} = -I_{B \text{ off}} = 1.0 \text{ A}$				
<b>Turn-on time</b>	$t_{on}$	max.	—	1.0 $\mu\text{s}$
<b>Turn-off;</b>				
<b>storage time</b>	$t_s$	max.	—	4.0 $\mu\text{s}$
<b>fall time</b>	$t_f$	max.	—	0.8 $\mu\text{s}$
<b>Switching times inductive load</b> (Figs 5 and 6)				
$I_{C \text{ on}} = 6 \text{ A}; I_{B \text{ on}} = 1.2 \text{ A}$				
$V_{CL} = 250 \text{ V}; T_c = 100 \text{ }^\circ\text{C}$				
<b>Turn-off;</b>				
<b>storage time</b>	$t_s$	typ.	1.9	— $\mu\text{s}$
	$t_s$	max.	2.5	— $\mu\text{s}$
<b>fall time</b>	$t_f$	typ.	200	— ns
	$t_f$	max.	300	— ns
$I_{C \text{ on}} = 5 \text{ A}; I_{B \text{ on}} = 1.0 \text{ A}$				
$V_{CL} = 300 \text{ V}; T_c = 100 \text{ }^\circ\text{C}$				
<b>Turn-off;</b>				
<b>storage time</b>	$t_s$	typ.	—	1.9 $\mu\text{s}$
	$t_s$	max.	—	2.5 $\mu\text{s}$
<b>fall time</b>	$t_f$	typ.	—	200 ns
	$t_f$	max.	—	300 ns

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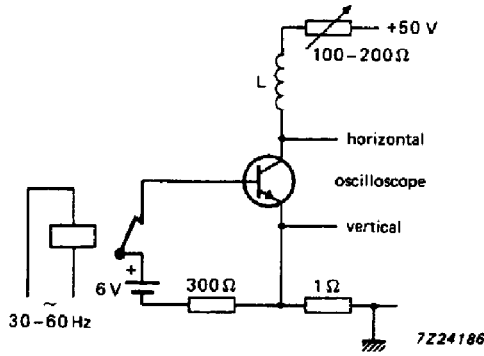


Fig. 2 Test circuit for  $V_{CEOsust}$ .

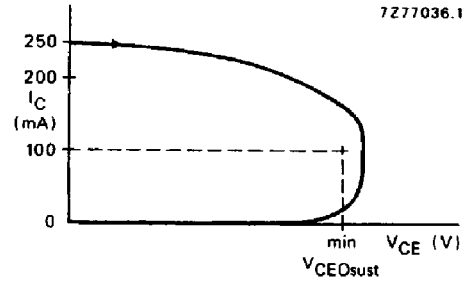
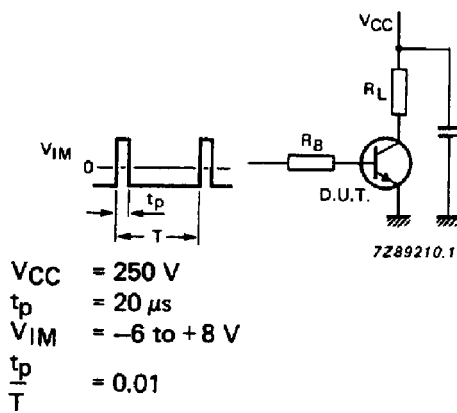


Fig. 3 Oscilloscope display for sustaining voltage.



The values of  $R_B$  and  $R_L$  are selected in accordance with  $I_{C\ on}$  and  $I_B$  requirements.

Fig. 4 Test circuit resistive load.

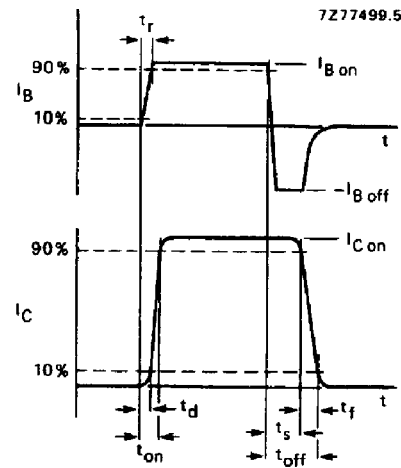


Fig. 5 Switching times waveforms with resistive load;  $t_r \leq 20\text{ ns}$ .

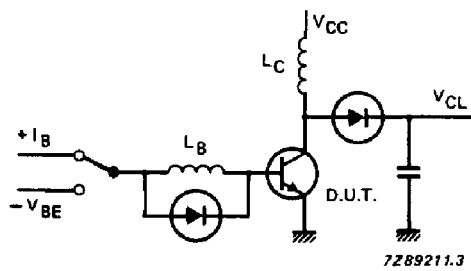


Fig. 6 Test circuit inductive load and reverse bias SOAR.

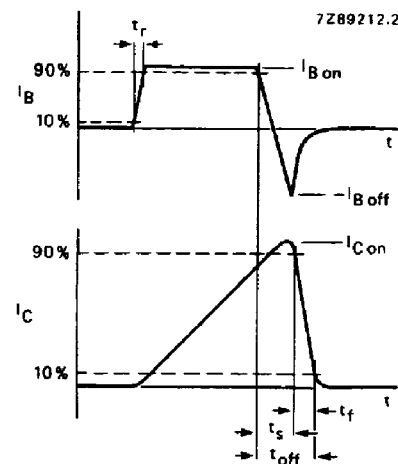


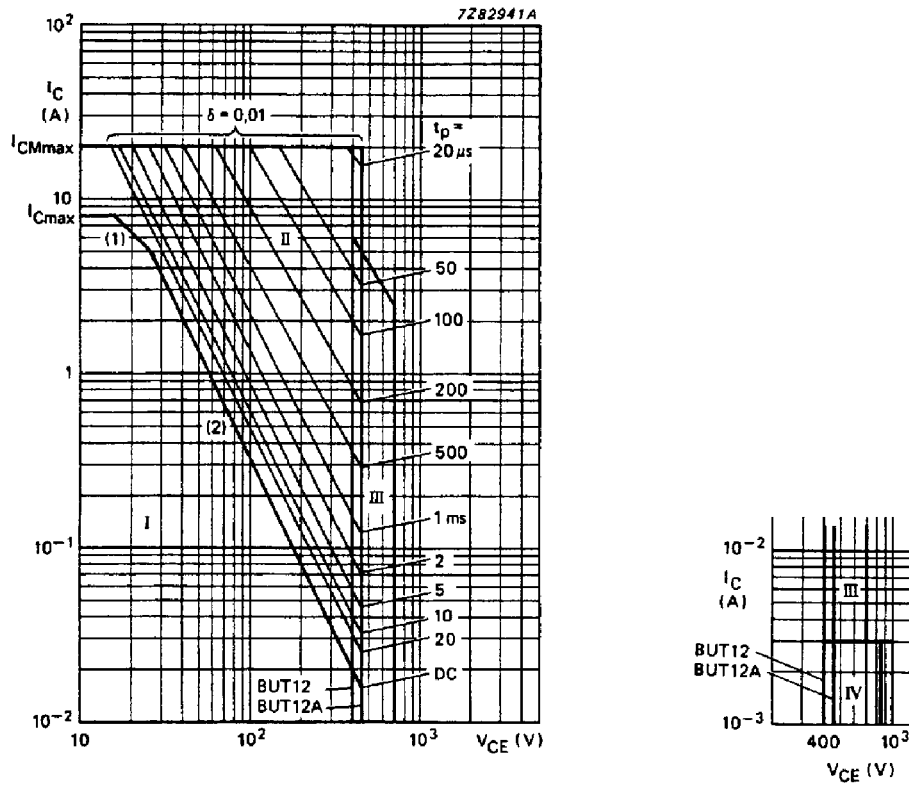
Fig. 7 Switching times waveforms with inductive load.

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- (1)  $P_{tot}$  max and  $P_{tot}$  peak max lines.
- (2) Second-breakdown limits.
- I Region of permissible DC operation
- II Permissible extension for repetitive pulse operation

Fig. 8 Safe operating area at  $T_{mb} < 25^\circ C$ .

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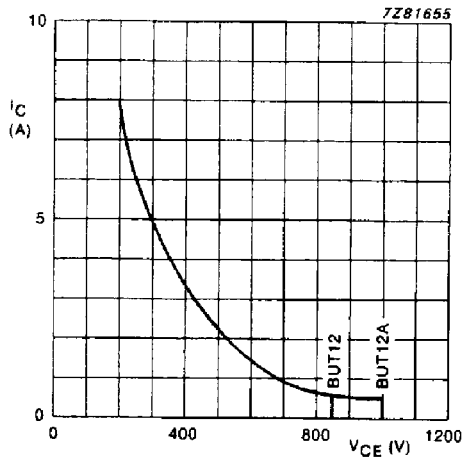


Fig. 9 Reverse bias SOAR;  $T_C = 100\text{ }^\circ\text{C}$ ;  $V_{BE} = -1\text{ V to } -5\text{ V}$ .

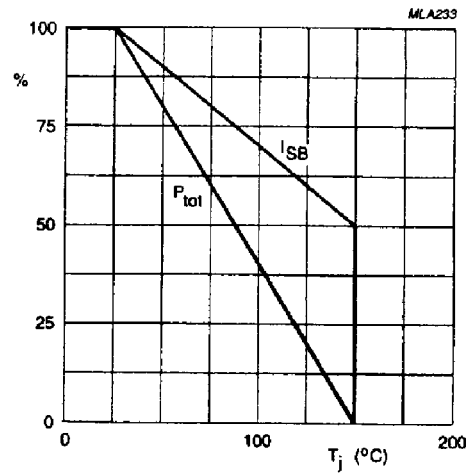


Fig. 10 Total power dissipation and second breakdown current derating curve.

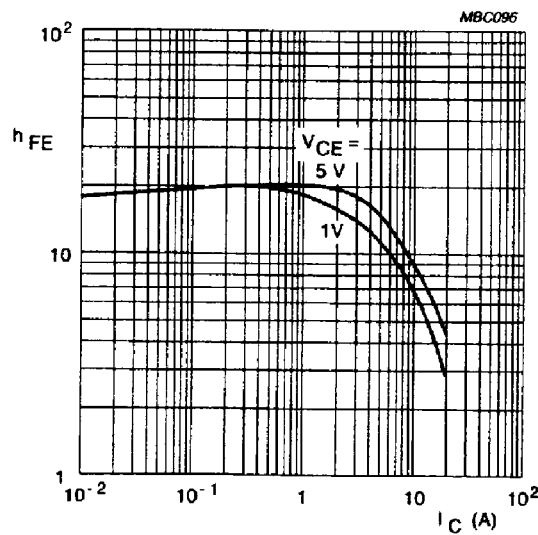


Fig. 11 Typical values DC current gain.

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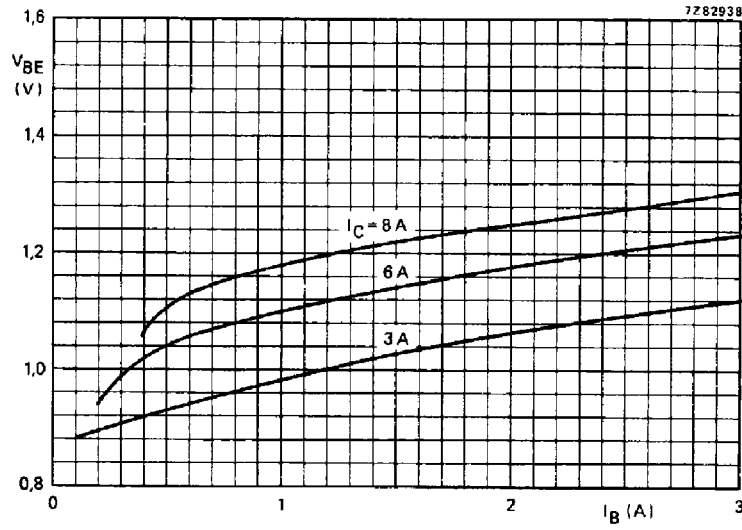


Fig. 12 Base-emitter voltage as a function of base current at  $T_j = 25^\circ C$ .

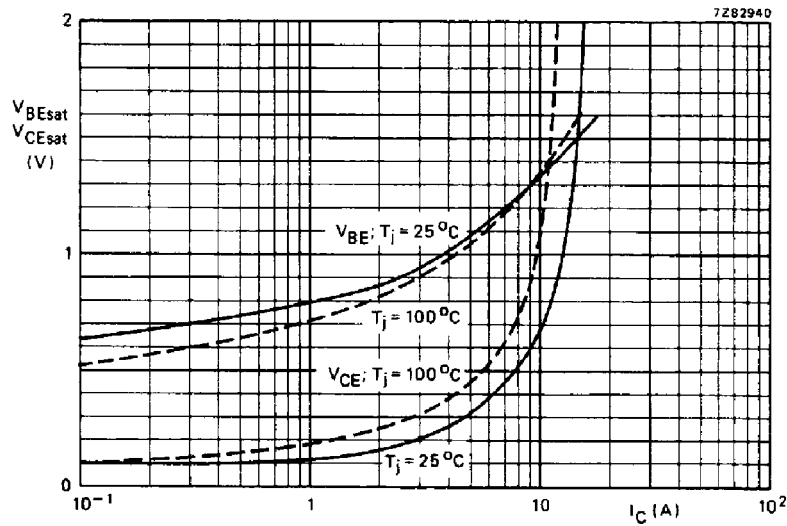


Fig. 13 Typical values base and collector voltage at  $I_C/I_B = 5$ .

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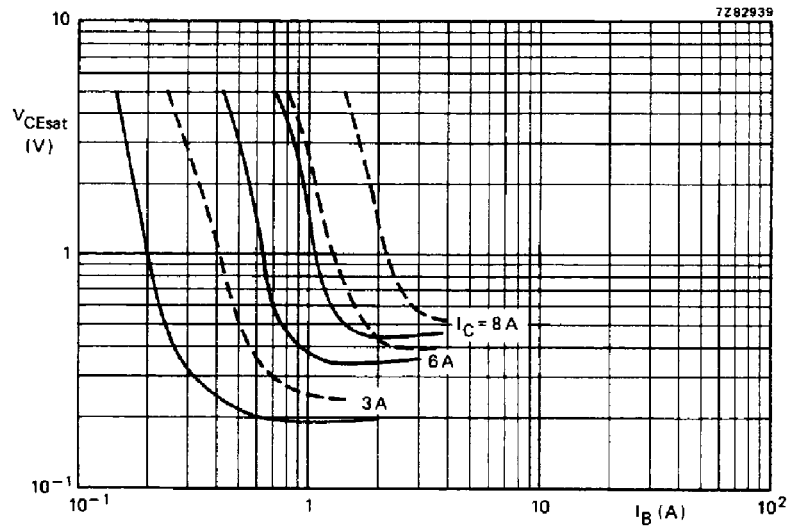


Fig. 14 Typical (—) and max. (---) values collector emitter saturation voltage at  $T_j = 25\text{ }^\circ\text{C}$ .

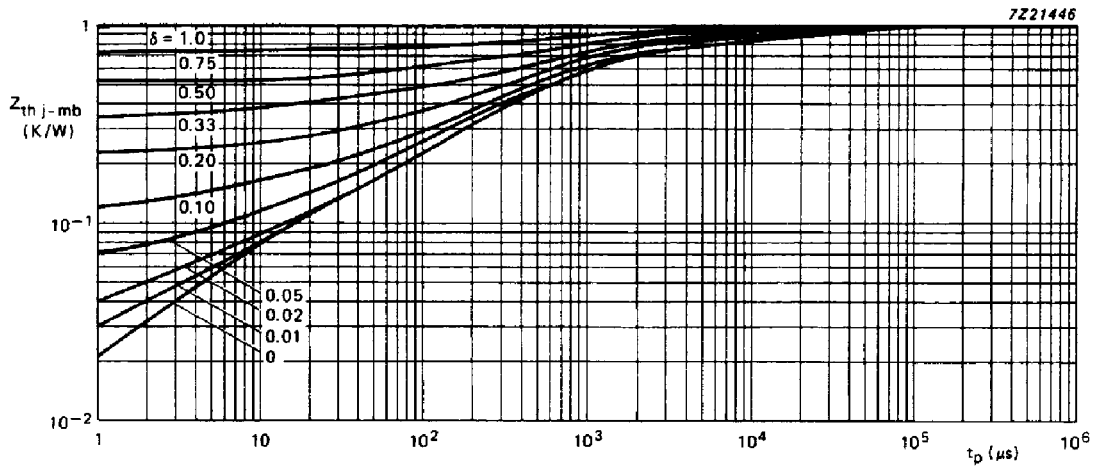


Fig. 15 Thermal response at pulse power conditions.

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