

**SINGLE-CHANNEL**  
**6N138**  
**6N139**

**DUAL-CHANNEL**  
**HCPL-2730**  
**HCPL-2731**

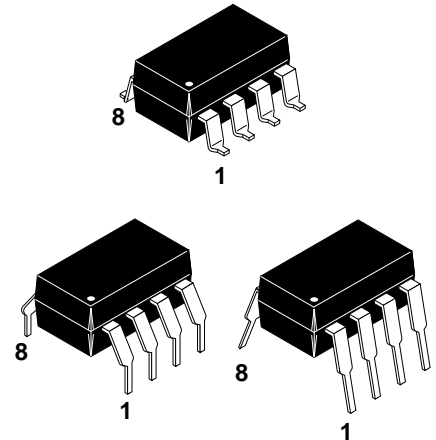
## DESCRIPTION

The 6N138/9 and HCPL-2730/HCPL-2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL-2730/HCPL2731, an integrated emitter - base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

An internal noise shield provides exceptional common mode rejection of 10 kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard 220 V.

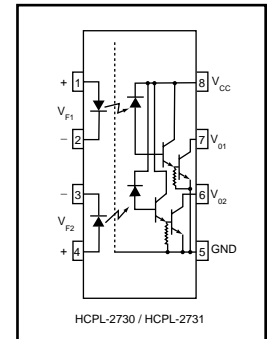
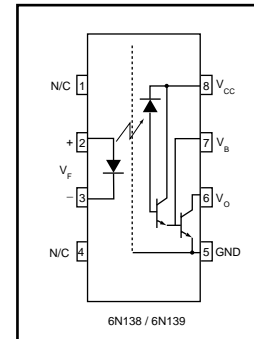


## FEATURES

- Low current - 0.5 mA
- Superior CTR-2000%
- Superior CMR-10 kV/μs
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)
- Dual Channel - HCPL-2730  
HCPL-2731

## APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver



## ABSOLUTE MAXIMUM RATINGS (No derating required up to 85°C)

Parameter	Symbol	Value	Units
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C
Operating Temperature	T <sub>OPR</sub>	-40 to +85	°C
Lead Solder Temperature	T <sub>SOL</sub>	260 for 10 sec	°C
<b>EMITTER</b>			
DC/Average Forward Input Current	I <sub>F</sub> (avg)	20	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	I <sub>F</sub> (pk)	40	mA
Peak Transient Input Current - (≤ 1 μs P.W., 300 pps)	I <sub>F</sub> (trans)	1.0	A
Reverse Input Voltage	V <sub>R</sub>	5	V
Input Power Dissipation	P <sub>D</sub>	35	mW
<b>DETECTOR</b>			
Average Output Current	I <sub>O</sub> (avg)	60	mA
Emitter-Base Reverse Voltage	V <sub>EB</sub>	0.5	V
Supply Voltage, Output Voltage	V <sub>CC</sub> , V <sub>O</sub>	-0.5 to 7 -0.5 to 18	V
Output power dissipation	P <sub>D</sub>	100	mW

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<b>ELECTRICAL CHARACTERISTICS</b> ( $T_A = 0$ to $70^\circ\text{C}$ unless otherwise specified.)							
<b>INDIVIDUAL COMPONENT CHARACTERISTICS</b>							
Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
<b>EMITTER</b> Input Forward Voltage	$T_A = 25^\circ\text{C}$ Each Channel ( $I_F = 1.6$ mA)	$V_F$	All		1.30	1.7	V
					1.75		
	Input Reverse Breakdown Voltage	$(T_A = 25^\circ\text{C}, I_R = 10$ $\mu\text{A}$ ) Each Channel	$BV_R$	All	5.0	20	
Temperature coefficient of forward voltage	( $I_F = 1.6$ mA)	$(\Delta V_F / \Delta T_A)$	All		-1.8		mV/ $^\circ\text{C}$
<b>DETECTOR</b> Logic high output current	$(I_F = 0$ mA, $V_O = V_{CC} = 18$ V) Each Channel	$I_{OH}$	6N139		0.01	100	$\mu\text{A}$
			HCPL-2731				
	$(I_F = 0$ mA, $V_O = V_{CC} = 7$ V) Each Channel	6N138		0.01	250		
		HCPL-2730					
Logic low supply	$(I_F = 1.6$ mA, $V_O = \text{Open}$ ) ( $V_{CC} = 18$ V)	$I_{CCL}$	6N138		0.4	1.5	mA
			6N139				
	$(I_{F1} = I_{F2} = 1.6$ mA, $V_{CC} = 18$ V) ( $V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 7$ V)	HCPL-2731 HCPL-2730		1.3	3		
Logic high supply	$(I_F = 0$ mA, $V_O = \text{Open}$ ) ( $V_{CC} = 18$ V)	$I_{CCH}$	6N138		0.05	10	$\mu\text{A}$
			6N139				
	$(I_{F1} = I_{F2} = 0$ mA, $V_{CC} = 18$ V) ( $V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 7$ V)	HCPL-2731		0.1	20		
		HCPL-2730					

\*\* All typicals at  $T_A = 25^\circ\text{C}$

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<b>TRANSFER CHARACTERISTICS</b> (T <sub>A</sub> = 0 to 70°C Unless otherwise specified)							
Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
<b>COUPLED</b>  Current transfer ratio (Notes 1,2)	(I <sub>F</sub> = 0.5 mA, V <sub>O</sub> = 0.4 V, V <sub>CC</sub> = 4.5 V) Each Channel	CTR	6N139	400	1100		%
			HCPL-2731		3500		
	(I <sub>F</sub> = 1.6 mA, V <sub>O</sub> = 0.4 V, V <sub>CC</sub> = 4.5 V) Each Channel		6N139	500	1300		%
			HCPL-2731		2500		
	(I <sub>F</sub> = 1.6 mA, V <sub>O</sub> = 0.4 V, V <sub>CC</sub> = 4.5 V) Each Channel		6N138	300	1300		%
			HCPL-2730		2500		
Logic low output voltage output voltage (Note 2)	(I <sub>F</sub> = 0.5 mA, I <sub>O</sub> = 2 mA, V <sub>CC</sub> = 4.5 V) Each Channel	V <sub>OL</sub>	6N139		0.08	0.4	V
	(I <sub>F</sub> = 1.6 mA, I <sub>O</sub> = 8 mA, V <sub>CC</sub> = 4.5 V) Each Channel		6N139		0.01	0.4	
	(I <sub>F</sub> = 5 mA, I <sub>O</sub> = 15 mA, V <sub>CC</sub> = 4.5 V) Each Channel		6N139		0.13	0.4	
	(I <sub>F</sub> = 12 mA, I <sub>O</sub> = 24 mA, V <sub>CC</sub> = 4.5 V) Each Channel		HCPL-2731		0.20	0.4	
	(I <sub>F</sub> = 1.6 mA, I <sub>O</sub> = 4.8 mA, V <sub>CC</sub> = 4.5 V) Each Channel		6N138		0.10	0.4	
			HCPL-2730				

\*\* All typicals at T<sub>A</sub> = 25°C

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**SWITCHING CHARACTERISTICS** ( $T_A = 0$  to  $70^\circ\text{C}$  unless otherwise specified.,  $V_{CC} = 5\text{ V}$ )

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low (Note 2) (Fig. 22)	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ Each Channel	$T_{PHL}$	6N139			30	$\mu\text{s}$
				$T_A = 25^\circ\text{C}$	4	25	
	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ Each Channel		HCPL-2731			120	
				$T_A = 25^\circ\text{C}$	3	100	
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ Each Channel		6N139			2	
				$T_A = 25^\circ\text{C}$	0.2	1	
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ Each Channel		HCPL-2730			3	
				$T_A = 25^\circ\text{C}$	0.3	2	
	$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ Each Channel		6N138			15	
				$T_A = 25^\circ\text{C}$	1.5	10	
$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ Each Channel	HCPL-2731			25			
		$T_A = 25^\circ\text{C}$	1	20			
Propagation delay time to logic high (Note 2) (Fig. 22)	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ Each Channel	$T_{PLH}$	6N139			90	$\mu\text{s}$
				$T_A = 25^\circ\text{C}$	12	60	
	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ Each Channel		HCPL-2731			22	
				$T_A = 25^\circ\text{C}$	1.3	7	
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ Each Channel		6N139			10	
				$T_A = 25^\circ\text{C}$	5	10	
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ Each Channel		HCPL-2730			15	
				$T_A = 25^\circ\text{C}$	7	35	
	$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ Each Channel		6N138			50	
				$T_A = 25^\circ\text{C}$	16		
$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ Each Channel	HCPL-2730/1			35			
		$T_A = 25^\circ\text{C}$					
Common mode transient immunity at logic high	$(I_F = 0\text{ mA},  V_{CM}  = 10\text{ V}_{P-P})$ $T_A = 25^\circ\text{C}, (R_L = 2.2\text{ k}\Omega)$ (Note 3) (Fig. 23) Each Channel	$ CM_H $	6N138	1,000	10,000		$\text{V}/\mu\text{s}$
			6N139				
			HCPL-2730 HCPL-2731				
Common mode transient immunity at logic low	$(I_F = 1.6\text{ mA},  V_{CM}  = 10\text{ V}_{P-P}, R_L = 2.2\text{ k}\Omega)$ $T_A = 25^\circ\text{C}$ (Note 3) (Fig. 23) Each Channel	$ CM_L $	6N138	1,000	10,000		$\text{V}/\mu\text{s}$
			6N139				
			HCPL-2730 HCPL-2731				

\*\* All typicals at  $T_A = 25^\circ\text{C}$

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<b>ISOLATION CHARACTERISTICS</b> ( $T_A = 0$ to $70^\circ\text{C}$ Unless otherwise specified)						
Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) ( $T_A = 25^\circ\text{C}$ , $t = 5$ s) ( $V_{I-O} = 3000$ VDC) (Note 8)	$I_{I-O}$			1.0	$\mu\text{A}$
Withstand insulation test voltage	( $\text{RH} \leq 50\%$ , $T_A = 25^\circ\text{C}$ ) (Note 4) ( $t = 1$ min.)	$V_{\text{ISO}}$	2500			$V_{\text{RMS}}$
Resistance (input to output)	(Note 4) ( $V_{I-O} = 500$ VDC)	$R_{I-O}$		$10^{12}$		$\Omega$
Capacitance (input to output)	(Note 4,5) ( $f = 1$ MHz)	$C_{I-O}$		0.6		pF
Input-Input Insulation leakage current	( $\text{RH} \leq 45\%$ , $V_{I-I} = 500$ VDC) (Note 6) $t = 5$ s, (HCPL-2730/2731 only)	$I_{I-I}$		0.005		$\mu\text{A}$
Input-Input Resistance	( $V_{I-I} = 500$ VDC) (Note 6) (HCPL-2730/2731 only)	$R_{I-I}$		$10^{11}$		$\Omega$
Input-Input Capacitance	( $f = 1$ MHz) (Note 6) (HCPL-2730/2731 only)	$C_{I-I}$		0.03		pF

\*\* All typicals at  $T_A = 25^\circ\text{C}$

## NOTES

- Current Transfer Ratio is defined as a ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.
- Pin 7 open. (6N138 and 6N139 only)
- Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{\text{cm}}/dt$  on the leading edge of the common mode pulse signal,  $V_{\text{CM}}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0$  V). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{\text{cm}}/dt$  on the trailing edge of the common mode pulse signal,  $V_{\text{CM}}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8$  V).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- For dual channel devices,  $C_{I-O}$  is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

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Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

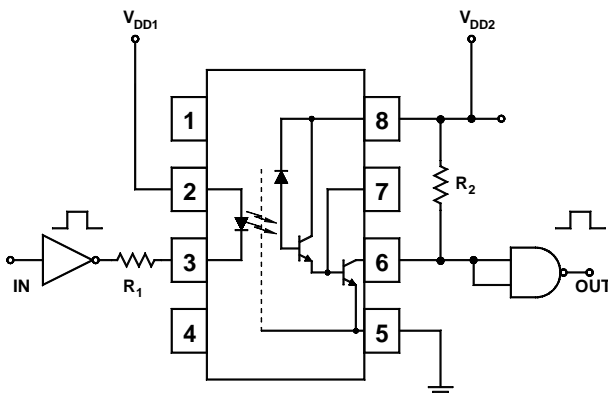
$$R_2 = \frac{V_{DD2} - V_{OLX} (@ I_L - I_2)}{I_L}$$

Where:

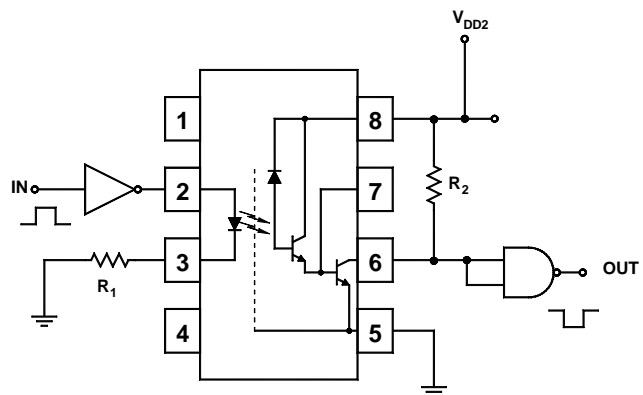
- $V_{DD1}$  - Input Supply Voltage
- $V_{DD2}$  - Output Supply Voltage
- $V_{DF}$  - Diode Forward Voltage
- $V_{OL1}$  - Logic "0" Voltage of Driver
- $V_{OH1}$  - Logic "1" Voltage of Driver
- $I_F$  - Diode Forward Current
- $V_{OLX}$  - Saturation Voltage of Output Transistor
- $I_L$  - Load Current Through Resistor R2
- $I_2$  - Input Current of Output Gate

INPUT			OUTPUT						
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX	74HXX
		R1 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )	R2 ( $\Omega$ )
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

**Fig. 1 Resistor Values for Logic Interface**



**Fig. 2 Non-Inverting Logic Interface**

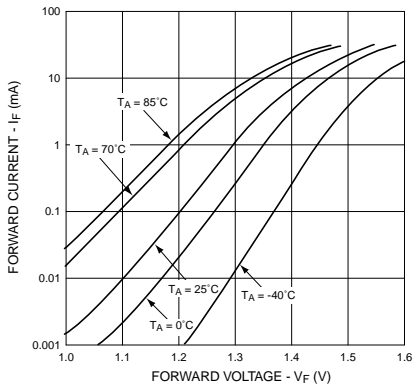


**Fig. 3 Inverting Logic Interface**

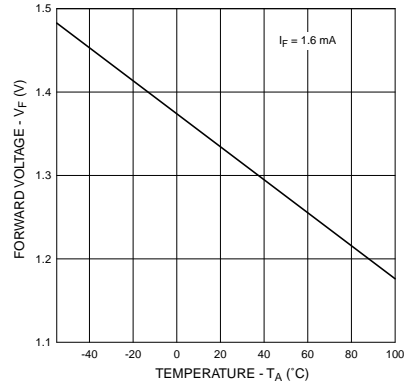
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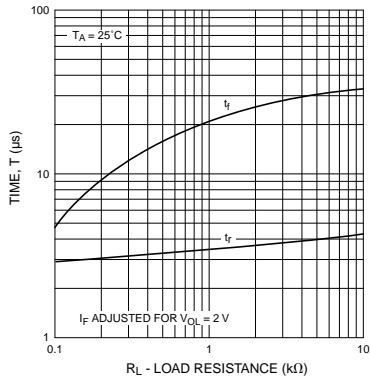
**Fig. 4 LED Forward Current vs. Forward Voltage**



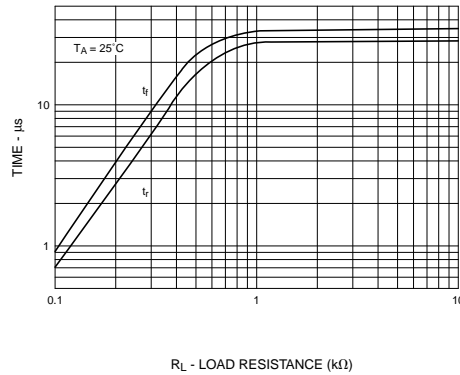
**Fig. 5 LED Forward Voltage vs. Temperature**



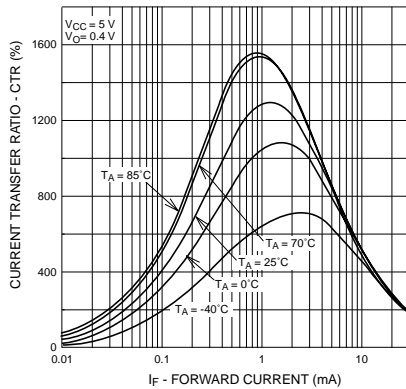
**Fig. 6 Non-saturated Rise and Fall Times vs. Load Resistance (6N138 / 6N139 Only)**



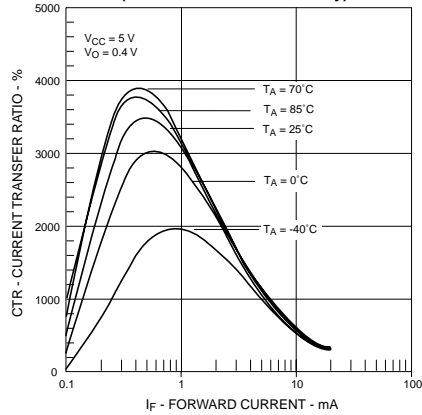
**Fig. 7 Non-saturated Rise and Fall Times vs. Load Resistance (HCPL-2730 / HCPL-2731 Only)**



**Fig. 8 Current Transfer Ratio vs. Forward Current (6N138 / 6N139 Only)**



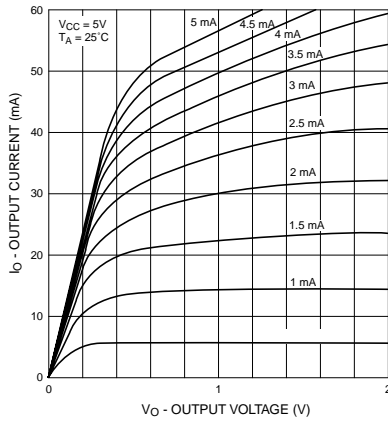
**Fig. 9 Current Transfer Ratio vs. Forward Current (HCPL-2730 / HCPL-2731 Only)**



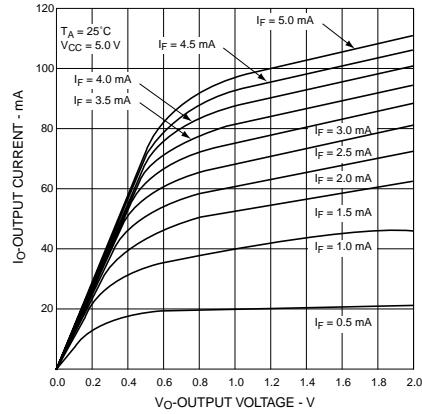
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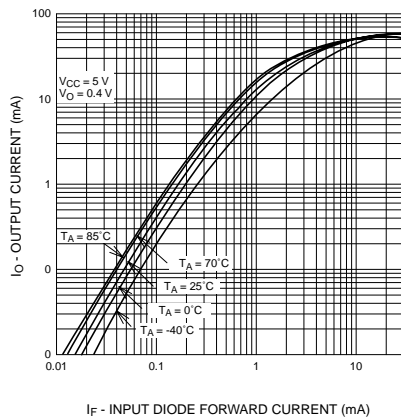
**Fig. 10 Output Current vs Output Voltage**  
(6N138 / 6N139 Only)



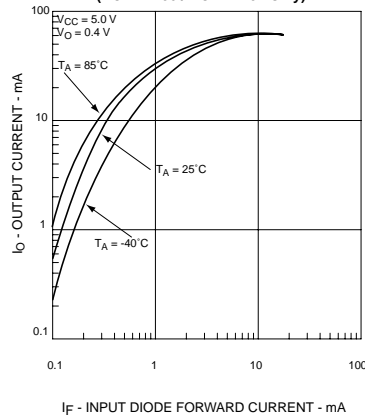
**Fig. 11 Output Current vs Output Voltage**  
(HCPL-2730 / HCPL-2731 Only)



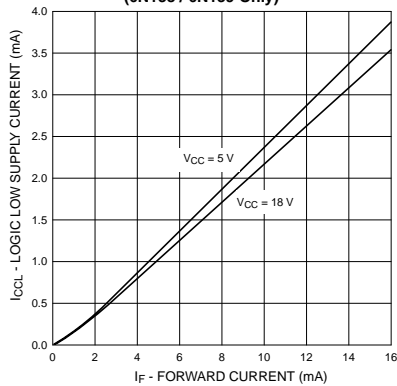
**Fig. 12 Output Current vs. Input Diode Forward Current**  
(6N138 / 6N139 Only)



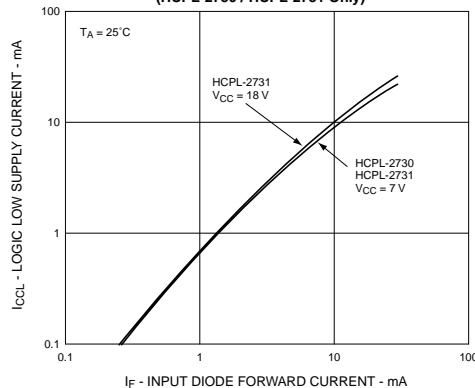
**Fig. 13 Output Current vs Input Diode Forward Current**  
(HCPL-2730 / HCPL-2731 Only)



**Fig. 14 Logic Low Supply Current vs. Input Diode Forward Current**  
(6N138 / 6N139 Only)



**Fig. 15 Logic Low Supply Current vs. Input Diode Forward Current**  
(HCPL-2730 / HCPL-2731 Only)

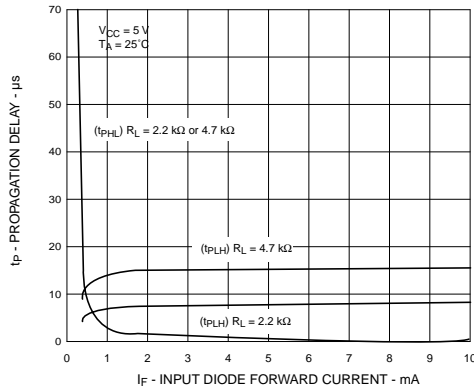




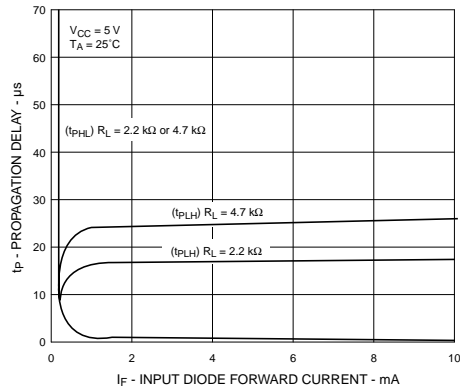
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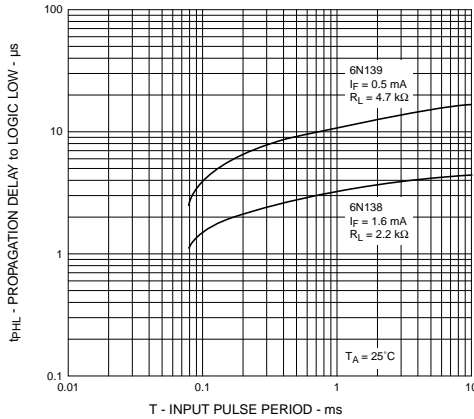
**Fig. 16 Propagation Delay vs. Input Diode Forward Current (6N138 / 6N139 Only)**



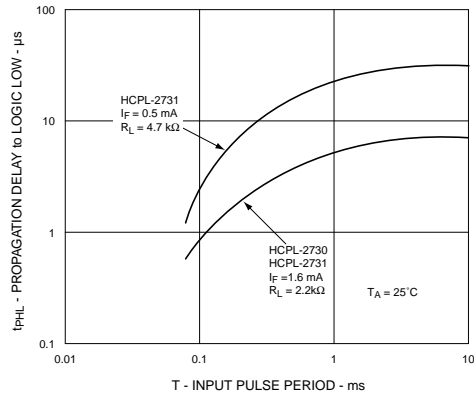
**Fig. 17 Propagation Delay vs. Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)**



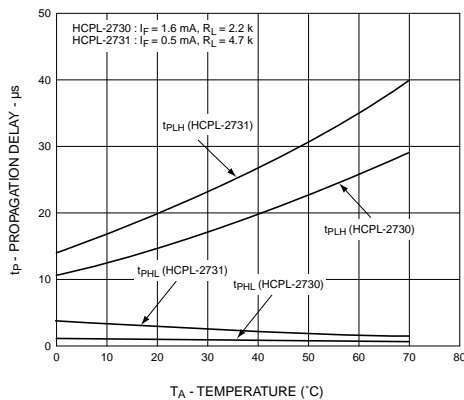
**Fig. 18 Propagation Delay to Logic Low vs. Pulse Period (6N138 / 6N139 Only)**



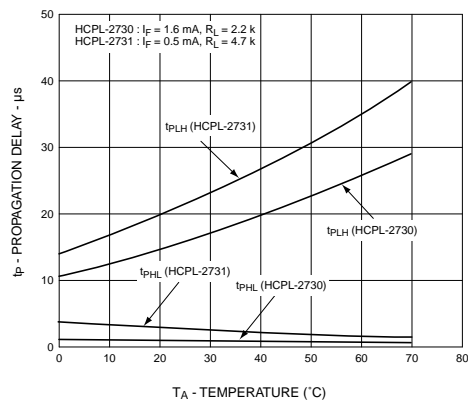
**Fig. 19 Propagation Delay to Logic Low vs. Pulse Period (HCPL-2730 / HCPL-2731 Only)**



**Fig. 20 Propagation Delay vs. Temperature (6N138 / 6N139 Only)**

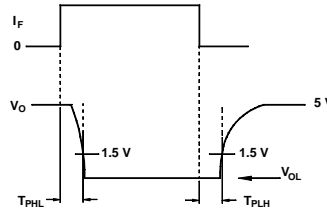
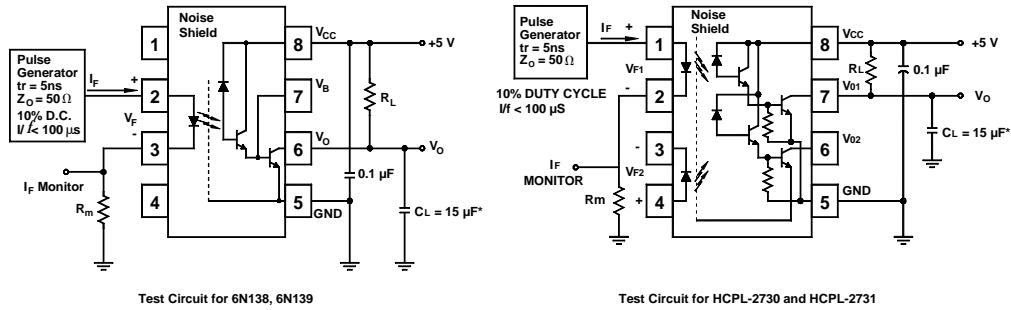


**Fig. 21 Propagation Delay vs. Temperature (HCPL-2730 / HCPL-2731 Only)**



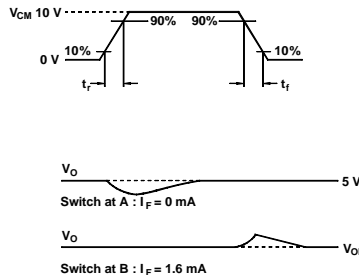
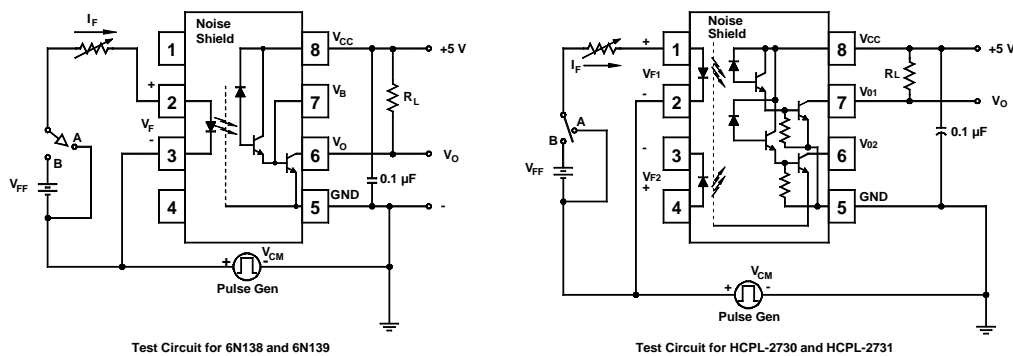
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**Fig. 22 Switching Time Test Circuit**

\*Includes Probe and Fixture Capacitance

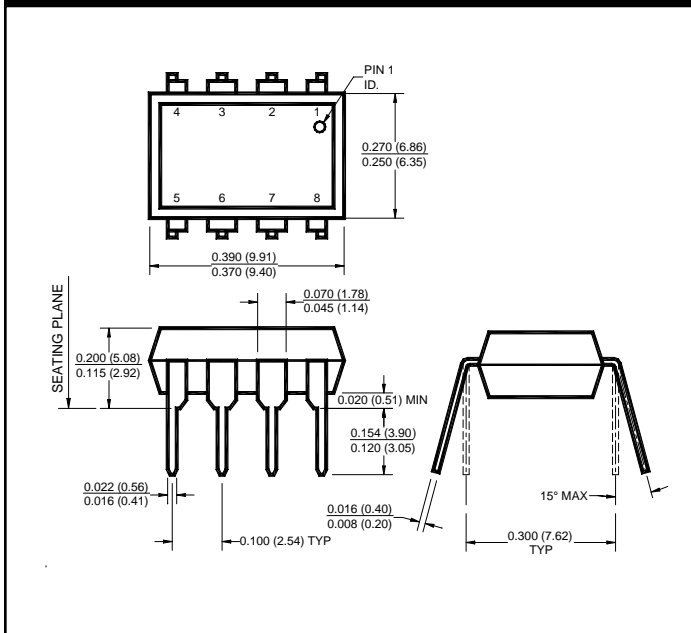


**Fig. 23 Common Mode Immunity Test Circuit**

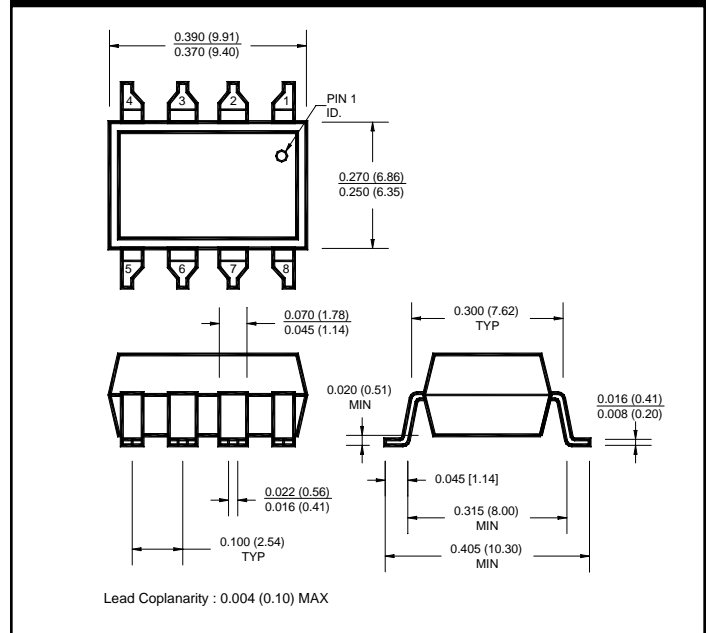
**SINGLE-CHANNEL**  
**6N138**  
**6N139**

**DUAL-CHANNEL**  
**HCPL-2730**  
**HCPL-2731**

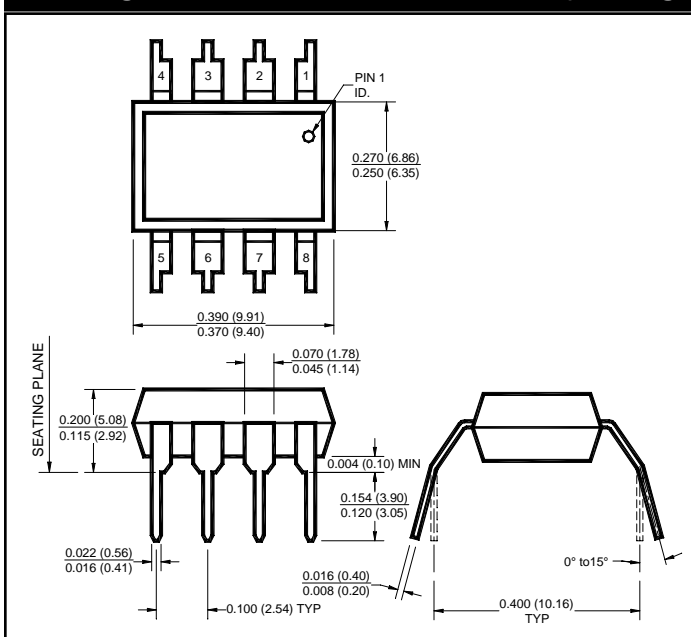
## Package Dimensions (Through Hole)



## Package Dimensions (Surface Mount)



## Package Dimensions (0.4" Lead Spacing)



**NOTE**

All dimensions are in inches (millimeters)

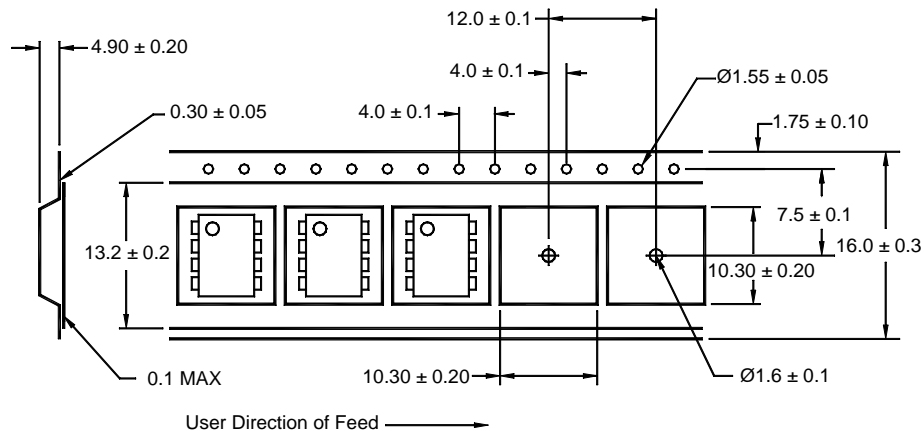
**SINGLE-CHANNEL**  
**6N138**  
**6N139**

**DUAL-CHANNEL**  
**HCPL-2730**  
**HCPL-2731**

## ORDERING INFORMATION

Option	Order Entry Identifier	Description
R2	.R2	Opto Plus Reliability Conditioning
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing

## QT Carrier Tape Specifications ("D" Taping Orientation)



### Corporate Headquarters

QT Optoelectronics  
610 North Mary Avenue  
Sunnyvale, CA 94086  
(408) 720-1440 Phone  
(408) 720-0848 Fax

### European Sales

QT Optoelectronics  
"Le Levant"  
2, rue du Nouveau Bercy  
F-94277-CHARENTON-LE PONT Cedex  
FRANCE  
33 [0] 1.45.18.78.78 Phone  
33 [0] 1.43.75.77.57 Fax

### North American Sales

QT Optoelectronics  
16775 Addison Rd., Suite 200  
Addison, TX 75001  
(972) 447-1300 Phone  
(972) 447-0784 Fax

### Asia/Pacific Sales

QT Optoelectronics  
B613, 6th Floor  
East Wing, Wisma Tractors  
Jalan SS16/1, Subang Jaya  
47500 Petaling Jaya  
Selangor Darul Eshan, Malaysia  
603/735-2417 Phone  
603/736-3382 Fax

### European Sales

Quality Technologies Deutschland GmbH  
Max-Huber-Strasse 8  
D-85737 Ismaning, Germany  
49 [0] 89/96.30.51 Phone  
49 [0] 89/96.54.74 Fax

### European Sales

Quality Technologies (U.K) Ltd.  
10, Prebendal Court, Oxford Road  
Aylesbury, Buckinghamshire  
HP19-3EY United Kingdom  
44 [0] 1296/30.44.99 Phone  
44 [0] 1296/39.24.32 Fax

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.