402-990

ANALOG DEVICES
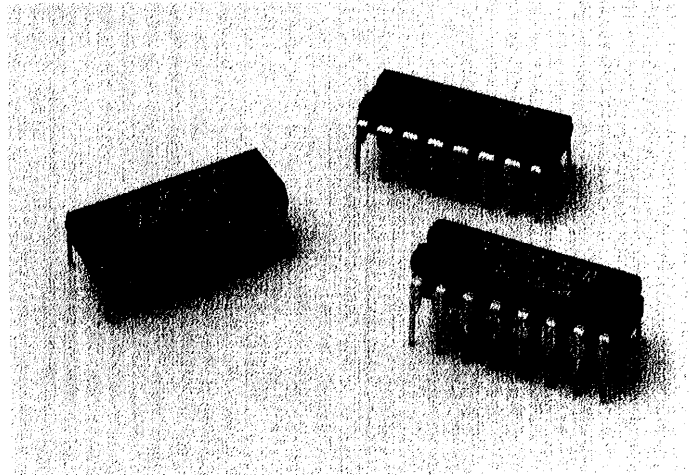
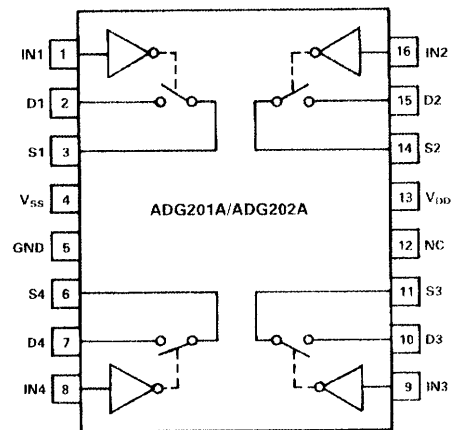# CMOS Quad SPST Switches

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Low Power Dissipation (33mW)
TTL/CMOS Compatible
Superior Second Source:
  ADG201A Replaces DG201A, HI-201
  ADG202A Replaces DG202

GENERAL DESCRIPTION
The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC^2MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS
1. Extended Signal Range:
   These switches are fabricated on an enhanced LC^2MOS process, resulting in high breakdown and an increased analog signal range of ±15V.

2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.

3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

PIN CONFIGURATION
(TOP VIEW)

IN1	1		16	IN2
D1	2		15	D2
S1	3		14	S2
V_{SS}	4	ADG201A/ADG202A	13	V_{DD}
GND	5		12	NC
S4	6		11	S3
D4	7		10	D3
IN4	8		9	IN3

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

SPECIFICATIONS $(V_{DD} = +15V, V_{SS} = -15V,$ unless otherwise noted)

Parameter	ADG201AKN ADG202AKN 25°C	ADG201AKN ADG202AKN 0 to +70°C	ADG201ABQ ADG202ABQ 25°C	ADG201ABQ ADG202ABQ -25°C to +85°C	ADG201ATQ ADG202ATQ 25°C	ADG201ATQ ADG202ATQ -55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V < V_S < +10V$
	90	145	90	145	90	145	Ω max	$I_{DS} = 1.0mA$ Test Circuit 1
R_{ON} vs. $V_D(V_S)$	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	$V_S = 0V, I_{DS} = 1mA$
I_S (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm14V; V_S = \mp14V$; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm14V; V_S = \mp14V$; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	$V_D = \pm14V$; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH} High Threshold		2.4		2.4		2.4	V min	
V_{INL} Low Threshold		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	
OFF Isolation	80		80		80		dB typ	$V_S = 10V(p\text{-}p); f = 100kHz$ $R_L = 75Ω$; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_{DS} (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	$R_S = 0Ω; C_L = 1000pF; V_S = 0V$ Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

-2-

ABSOLUTE MAXIMUM RATINGS*
($T_A = 25°C$ unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . $-25V$
Analog Inputs[1]
 Voltage at S, D . . . . V_{SS} to V_{DD}
 Continuous Current, S or D 30mA
 Pulsed Current S or D
  1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
 Voltage at IN . . . . $V_{SS} - 2V$ to
  $V_{DD} + 2V$ or
  20mA, Whichever Occurs First

Power Dissipation (Package)
 Plastic DIP
  Up to $+75°C$ 470mW
 Cerdip
  Up to $+75°C$ . . . . 900mW/°C
  Derates above $+75°C$ by . . . . 12mW/°C
Operating Temperature
 Plastic (KN Version) . . . . 0 to $+70°C$
 Cerdip (BQ Version) . . . . $-25°C$ to $+85°C$
 Cerdip (TQ Version) . . . . $-55°C$ to $+125°C$
Storage Temperature Range . . . . $-65°C$ to $+150°C$
Lead Temperature (Soldering 10sec) . . . . $+300°C$
NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
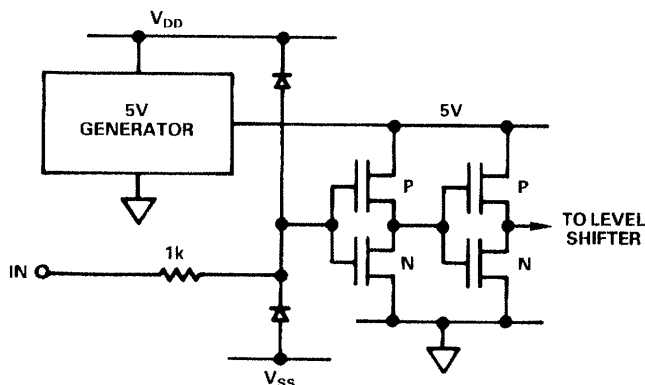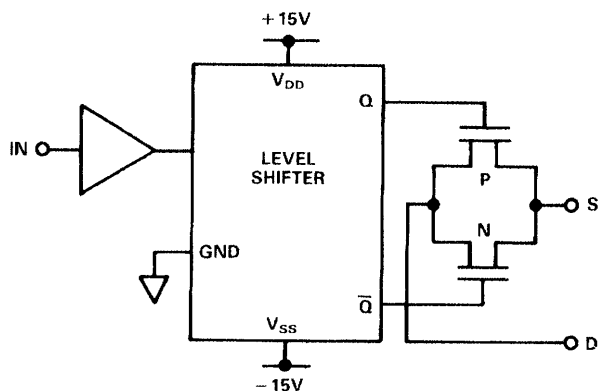
ADG201A/ADG202A FUNCTIONAL DIAGRAM

Figure 1. Typical Digital Input Cell

ORDERING INFORMATION[1,2]

Plastic 0 to +70°C	Cerdip[3] -25°C to +85°C	Cerdip[3] -55°C to +125°C
ADG201AKN	ADG201ABQ	ADG201ATQ
ADG202AKN	ADG202ABQ	ADG202ATQ

NOTES
[1]To order military standard 883B REV C processed parts, add /883B to part number. Contact your local sales office for military data sheet.
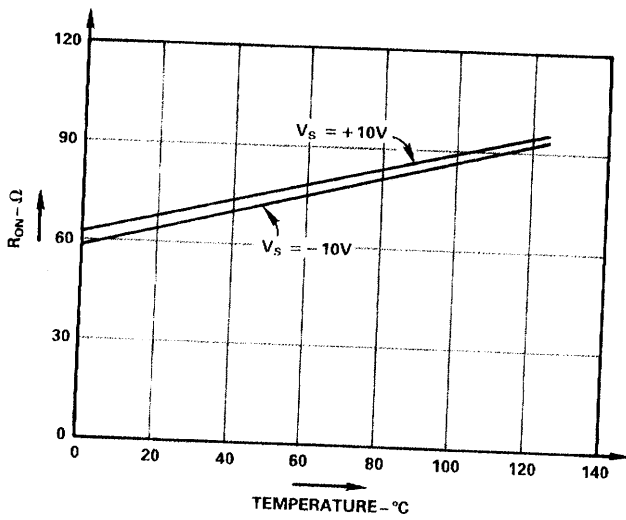[2]Leadless Ceramic Chip Carrier versions are available. To order, replace Q with E. Plastic Leaded Chip Carrier versions are also available. To order, replace N with P.
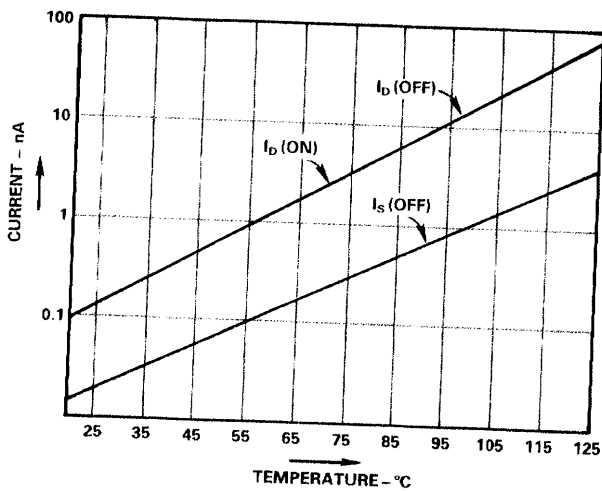[3]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.
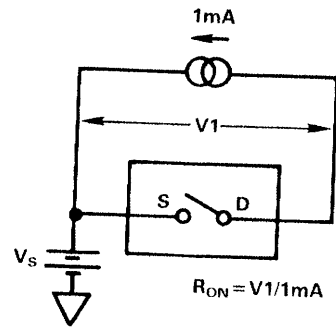
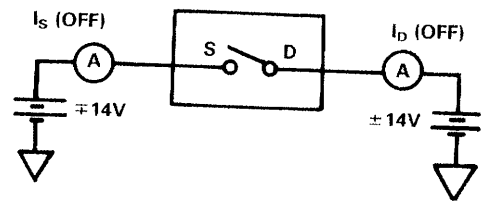# Typical Performance Characteristics
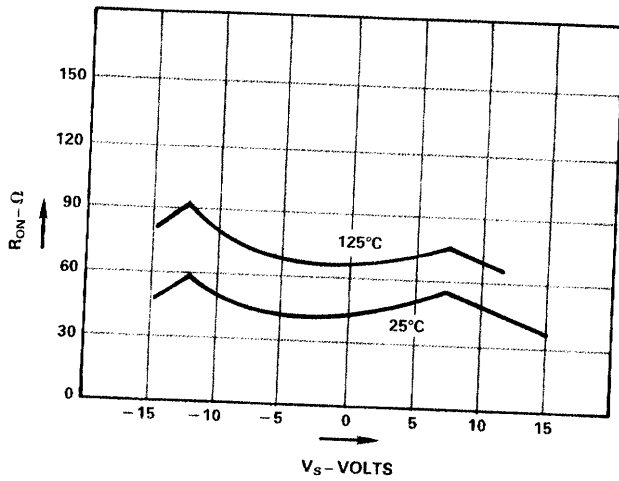
R_{ON} as a Function of V_D (V_S)

Test Circuit 1

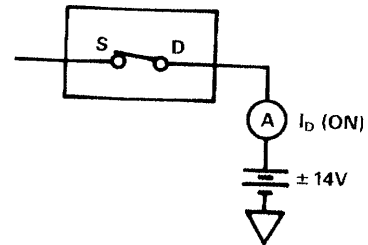R_{ON} as a Function of Temperature

Test Circuit 2

Leakage Current as a Function of Temperature

Test Circuit 3

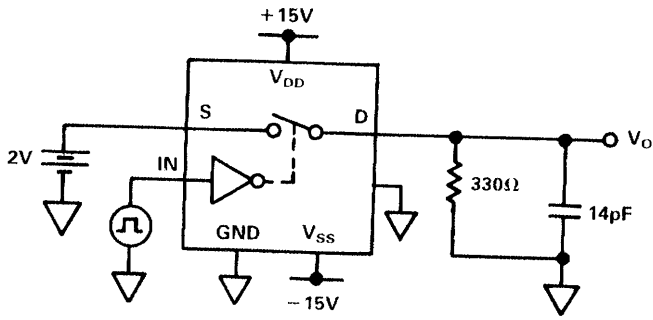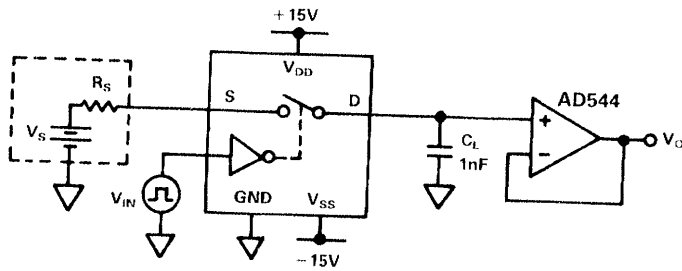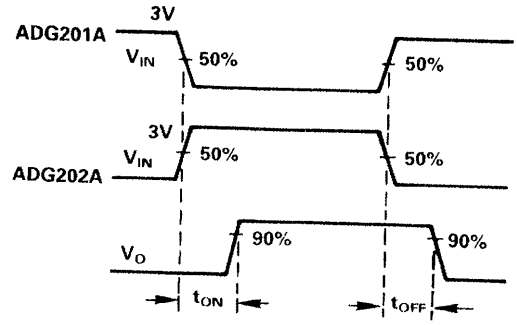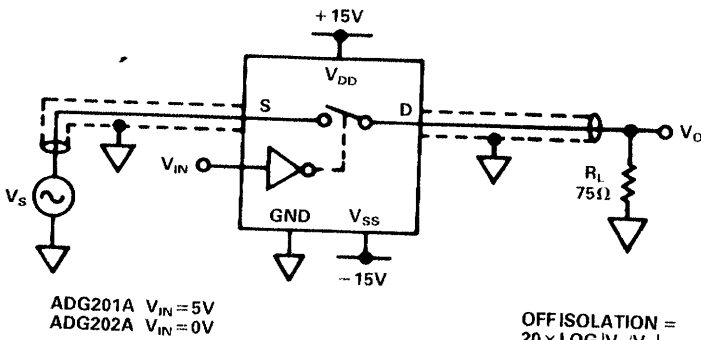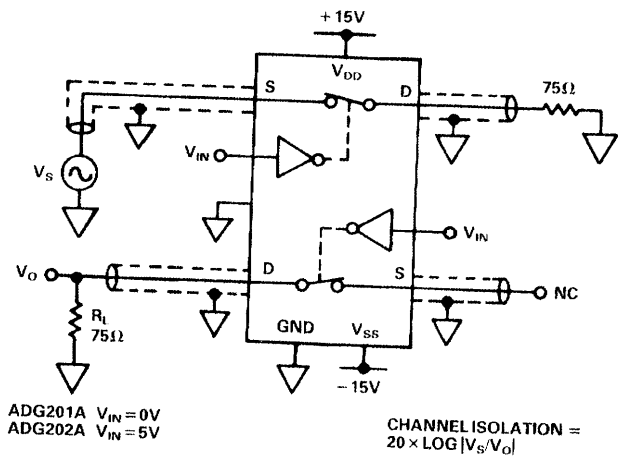Test Circuit 4

Test Circuit 5. Charge Injection

$$QINJ = C_L \times \Delta V_O$$

ADG201A $V_{IN} = 5V$
ADG202A $V_{IN} = 0V$

OFF ISOLATION = $20 \times LOG |V_S/V_O|$
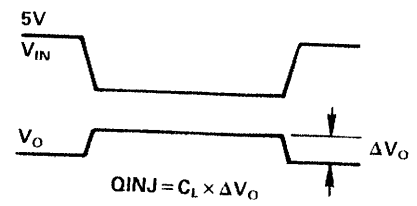
Test Circuit 6. Off Isolation

ADG201A $V_{IN} = 0V$
ADG202A $V_{IN} = 5V$

CHANNEL ISOLATION = $20 \times LOG |V_S/V_O|$

Test Circuit 7. Channel to Channel Isolation

TERMINOLOGY

|	
R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	OUT terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_{DS} (ON)	Input to output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Threshold voltage for low state
V_{INH}	Threshold voltage for high state
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

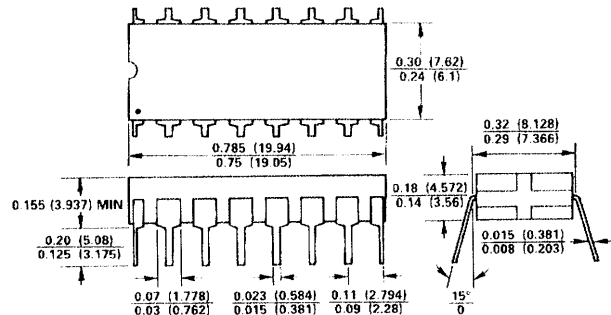# MECHANICAL INFORMATION

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).
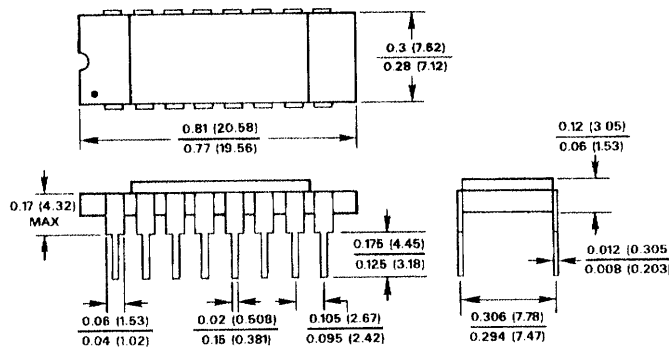
16-PIN PLASTIC (SUFFIX N)
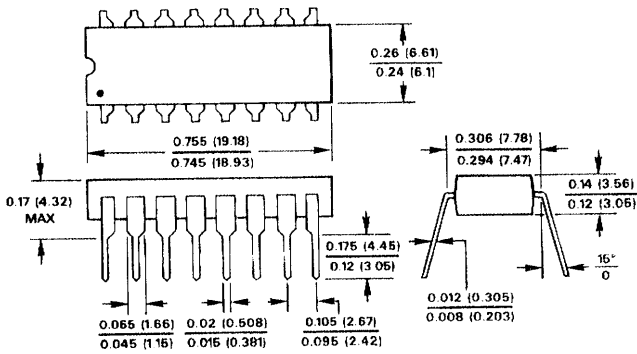
LEAD NO 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERDIP (SUFFIX Q)

16-PIN CERAMIC DIP[1]

LEAD NO 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

NOTE
[1]ANALOG DEVICES RESERVES THE RIGHT TO
SHIP CERAMIC PACKAGES IN LIEU OF CERDIP
PACKAGES.