



## ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 500-mA LOW-DROPOUT LINEAR REGULATORS

### FEATURES

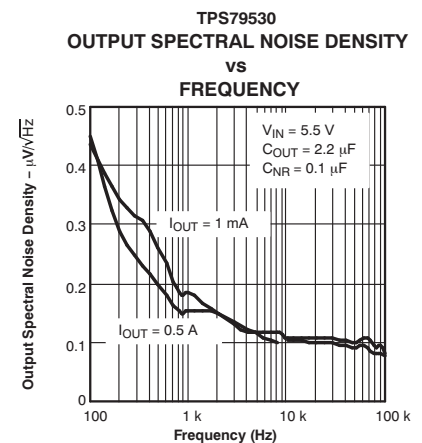
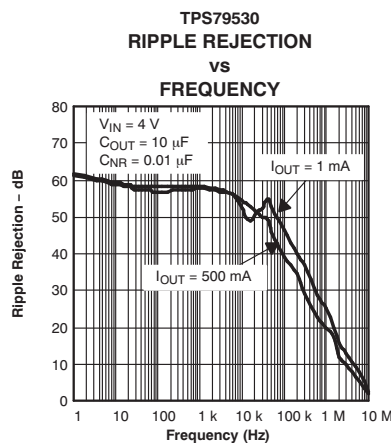
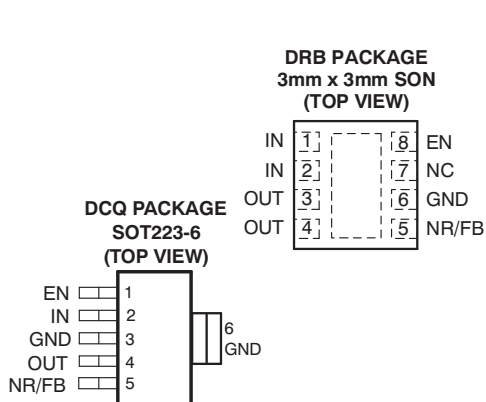
- 500-mA Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2-V to 5.5-V) Versions
- High PSRR (50 dB at 10 kHz)
- Ultralow Noise (33  $\mu\text{V}_{\text{RMS}}$ , TPS79530)
- Fast Start-Up Time (50  $\mu\text{s}$ )
- Stable With a 1- $\mu\text{F}$  Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (110 mV at Full Load, TPS79530)
- 6-Pin SOT223 and 3  $\times$  3 SON Packages

### APPLICATIONS

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth<sup>®</sup>, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

### DESCRIPTION

The TPS795xx family of low-dropout (LDO), low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, SOT223-6 and 3  $\times$  3 SON packages. Each device in the family is stable with a small 1- $\mu\text{F}$  ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 110 mV at 500 mA). Each device achieves fast start-up times (approximately 50  $\mu\text{s}$  with a 0.001- $\mu\text{F}$  bypass capacitor) while consuming very low quiescent current (265  $\mu\text{A}$ , typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1  $\mu\text{A}$ . The TPS79530 exhibits approximately 33  $\mu\text{V}_{\text{RMS}}$  of output voltage noise at 3.0 V output with a 0.1- $\mu\text{F}$  bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.  
All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TPS795xxyyyz	<b>XX</b> is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). <b>YYY</b> is package designator. <b>Z</b> is package quantity.

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Output voltages from 1.3 V to 5.0 V in 100 mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS

over operating temperature (unless otherwise noted)<sup>(1)</sup>

	VALUE
V <sub>IN</sub> range	– 0.3 V to 6 V
V <sub>EN</sub> range	–0.3 V to V <sub>IN</sub> + 0.3 V
V <sub>OUT</sub> range	6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Junction temperature range, T <sub>J</sub>	–40°C to +150°C
Storage temperature range, T <sub>stg</sub>	–65°C to +150°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

### DISSIPATION RATING TABLE

PACKAGE	BOARD	R <sub>θJC</sub>	R <sub>θJA</sub>
SOT223	Low K <sup>(1)</sup>	15°C/W	53°C/W
3 x 3 SON	High-K <sup>(2)</sup>	1.2°C/W	40°C/W

- (1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3-inch (7.5 cm × 7.5cm), two-layer board with 2-ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch × 3-inch (7,5-cm × 7,5-cm), multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{EN} = V_{IN}$ ,  $V_{IN} = V_{OUT(nom)} + 1\text{ V}^{(1)}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 0.01\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $+25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input voltage, $V_{IN}^{(1)}$			2.7		5.5	V	
Internal reference, $V_{FB}$ (TPS79501)			1.200	1.225	1.250	V	
Continuous output current, $I_{OUT}$			0		500	mA	
Output voltage	Output voltage range	TPS79501		1.225	$5.5 - V_{DO}$	V	
	Accuracy	TPS79501 <sup>(2)</sup>	$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$ , $V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	$0.98(V_{OUT})$	$V_{OUT}$	$1.02(V_{OUT})$	V
		Fixed $V_{OUT}$	$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$ , $V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	-2.0		+2.0	%
Output voltage line regulation ( $\Delta V_{OUT}/\Delta V_{IN}^{(1)}$ )		$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.05	0.12	%/V	
Load regulation ( $\Delta V_{OUT}/\Delta I_{OUT}$ )		$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$ ,		3		mV	
Dropout voltage <sup>(3)</sup> $V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$	TPS79530	$I_{OUT} = 500\text{ mA}$		110	170	mV	
	TPS79533	$I_{OUT} = 500\text{ mA}$		105	160		
Output current limit		$V_{OUT} = 0\text{ V}$	2.4	2.8	4.2	A	
Ground pin current		$0\text{ }\mu\text{A} \leq I_{OUT} \leq 500\text{ mA}$		265	385	$\mu\text{A}$	
Shutdown current <sup>(4)</sup>		$V_{EN} = 0\text{ V}$ , $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.07	1	$\mu\text{A}$	
FB pin current		$V_{FB} = 1.225\text{ V}$			1	$\mu\text{A}$	
Power-supply ripple rejection	TPS79530	$f = 100\text{ Hz}$ , $I_{OUT} = 10\text{ mA}$		59		dB	
		$f = 100\text{ Hz}$ , $I_{OUT} = 500\text{ mA}$		58			
		$f = 10\text{ kHz}$ , $I_{OUT} = 500\text{ mA}$		50			
		$f = 100\text{ kHz}$ , $I_{OUT} = 500\text{ mA}$		39			
Output noise voltage (TPS79530)		$BW = 100\text{ Hz to }100\text{ kHz}$ , $I_{OUT} = 500\text{ mA}$	$C_{NR} = 0.001\text{ }\mu\text{F}$		46	$\mu\text{V}_{RMS}$	
			$C_{NR} = 0.0047\text{ }\mu\text{F}$		41		
			$C_{NR} = 0.01\text{ }\mu\text{F}$		35		
			$C_{NR} = 0.1\text{ }\mu\text{F}$		33		
Time, start-up (TPS79530)		$R_L = 6\text{ }\Omega$ , $C_{OUT} = 1\text{ }\mu\text{F}$	$C_{NR} = 0.001\text{ }\mu\text{F}$		50	$\mu\text{s}$	
			$C_{NR} = 0.0047\text{ }\mu\text{F}$		75		
			$C_{NR} = 0.01\text{ }\mu\text{F}$		110		
High-level enable input voltage		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	1.7		$V_{IN}$	V	
Low-level enable input voltage		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$			0.7	V	
EN pin current		$V_{EN} = 0\text{ V}$	1		1	$\mu\text{A}$	
UVLO threshold		$V_{CC}$ rising	2.25		2.65	V	
UVLO hysteresis				100		mV	

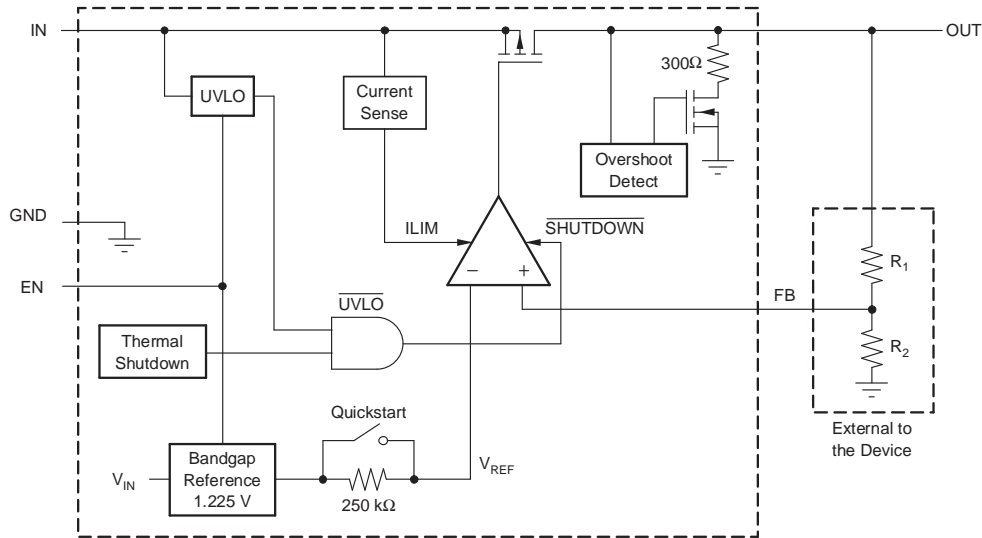
(1) Minimum  $V_{IN}$  is 2.7 V or  $V_{OUT} + V_{DO}$ , whichever is greater.

(2) Tolerance of external resistors not included in this specification.

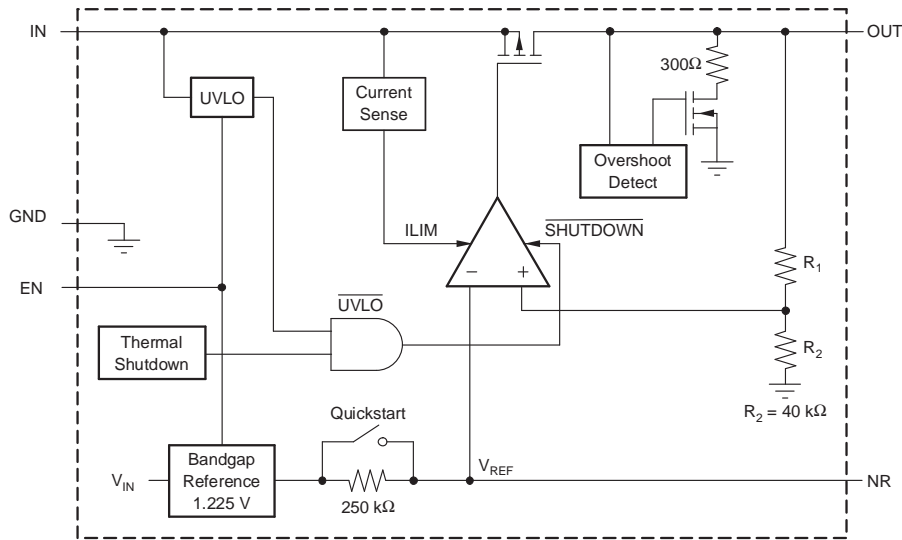
(3) Dropout is not measured for the TPS79501 and TPS79525 since minimum  $V_{IN} = 2.7\text{ V}$ .

(4) For adjustable version, this applies only after  $V_{IN}$  is applied; then  $V_{EN}$  transitions high to low.

**FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION**



**FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION**



**Table 1. Terminal Functions**

NAME	SOT223 (DCQ) PIN NO.	3x3 SON (DRB) PIN NO.	DESCRIPTION
IN	2	1, 2	Unregulated input to the device
GND	3, 6	6	Regulator ground
EN	1	8	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	5	5	Noise-reduction pin for fixed versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise. (Not available on adjustable versions.)
FB	5	5	Feedback input voltage for the adjustable device. (Not available on fixed voltage versions.)
OUT	4	3, 4	Regulator output.
NC	—	7	Not connected

TYPICAL CHARACTERISTICS

TPS79530  
OUTPUT VOLTAGE  
vs OUTPUT CURRENT

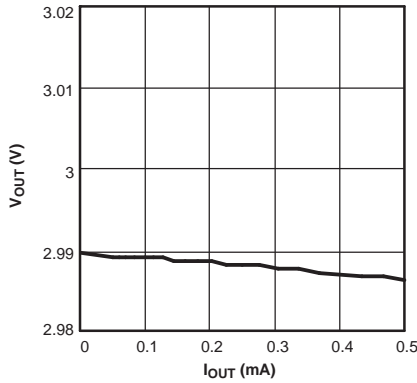


Figure 1.

TPS79530  
OUTPUT VOLTAGE  
vs JUNCTION TEMPERATURE

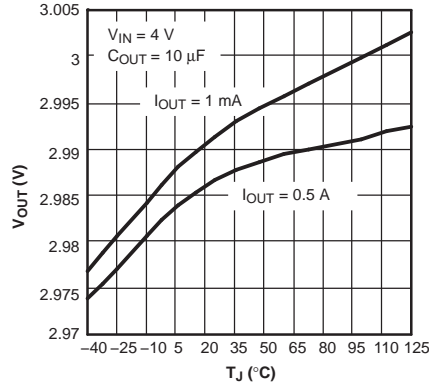


Figure 2.

TPS79530  
GROUND CURRENT  
vs JUNCTION TEMPERATURE

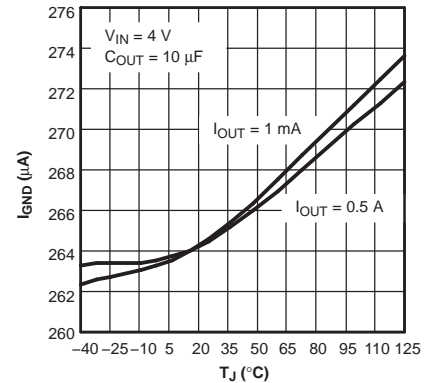


Figure 3.

TPS79530  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

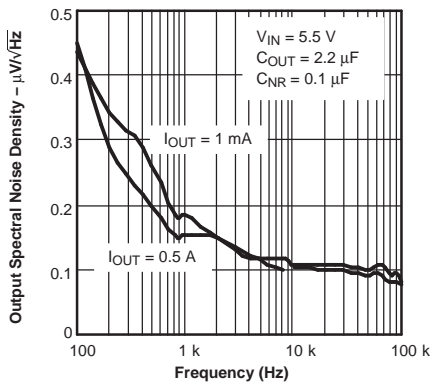


Figure 4.

TPS79530  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

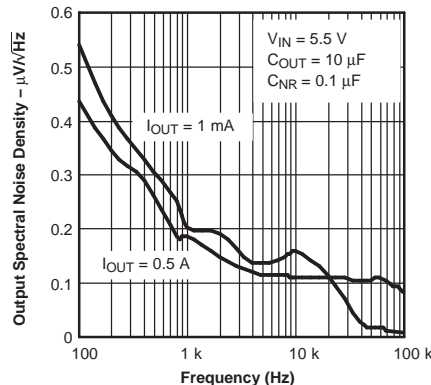


Figure 5.

TPS79530  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

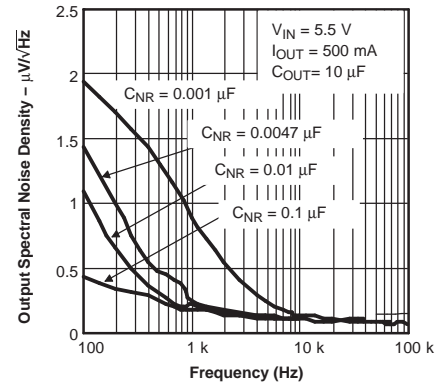


Figure 6.

TPS79530  
ROOT MEAN SQUARED  
OUTPUT NOISE vs CNR

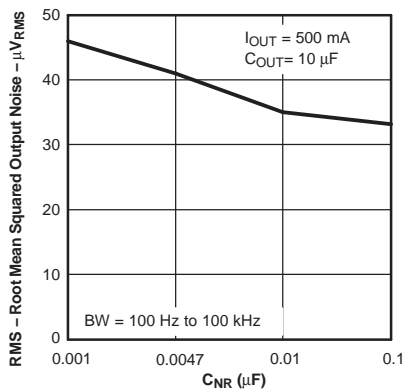


Figure 7.

TPS79530  
DROPOUT VOLTAGE  
vs JUNCTION TEMPERATURE

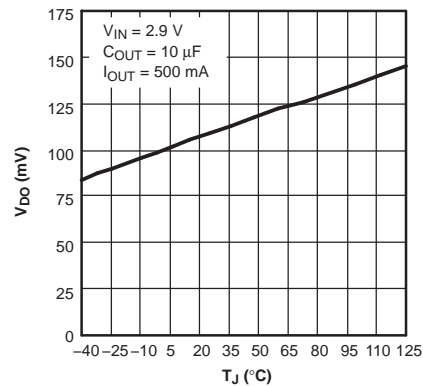


Figure 8.

TPS79530  
RIPPLE REJECTION  
vs FREQUENCY

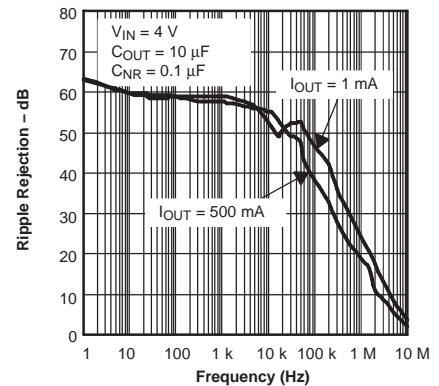


Figure 9.

TYPICAL CHARACTERISTICS (continued)

**TPS79530  
RIPPLE REJECTION  
vs FREQUENCY**

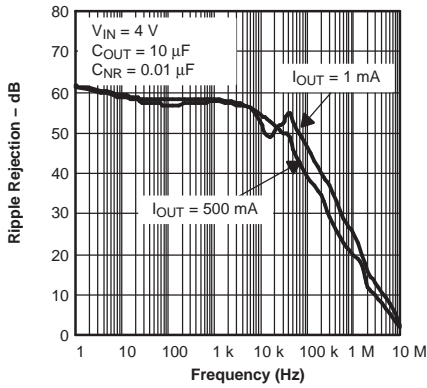


Figure 10.

**TPS79530  
RIPPLE REJECTION  
vs FREQUENCY**

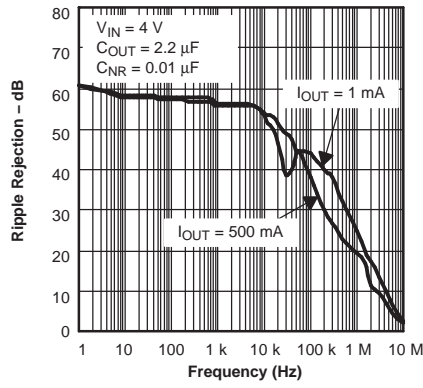


Figure 11.

**TPS79530  
RIPPLE REJECTION  
vs FREQUENCY**

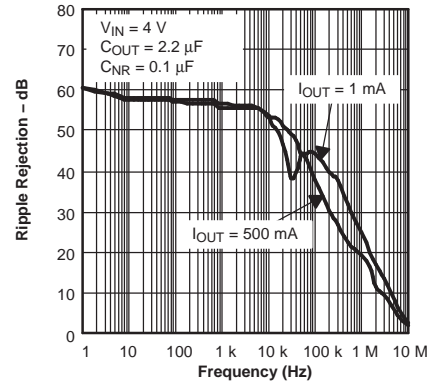


Figure 12.

**TPS79530  
START-UP TIME**

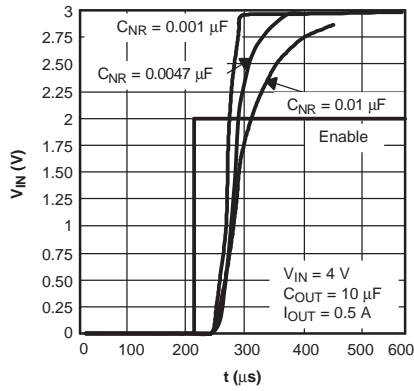


Figure 13.

**TPS79518  
LINE TRANSIENT RESPONSE**

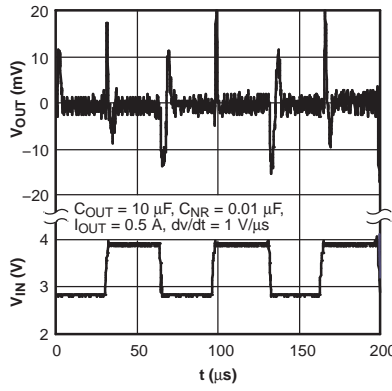


Figure 14.

**TPS79530  
LINE TRANSIENT RESPONSE**

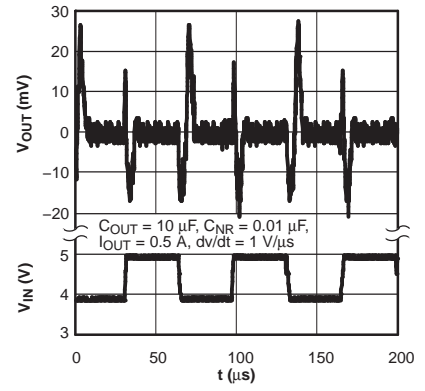


Figure 15.

**TPS79530  
LOAD TRANSIENT RESPONSE**

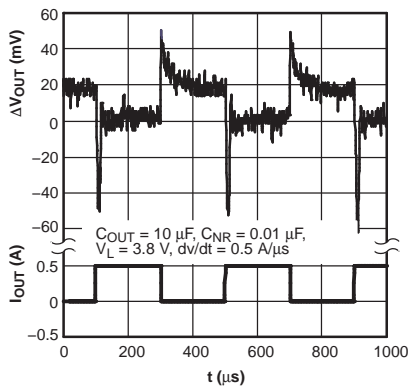


Figure 16.

**TPS79525  
POWER UP/POWER DOWN**

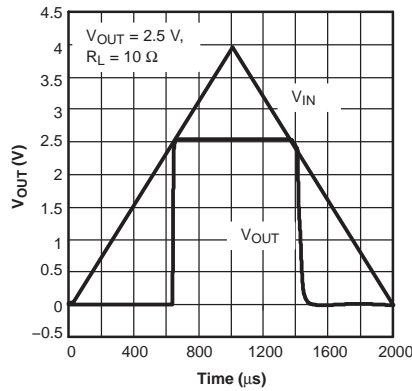


Figure 17.

**TPS79530  
DROPOUT VOLTAGE  
vs OUTPUT CURRENT**

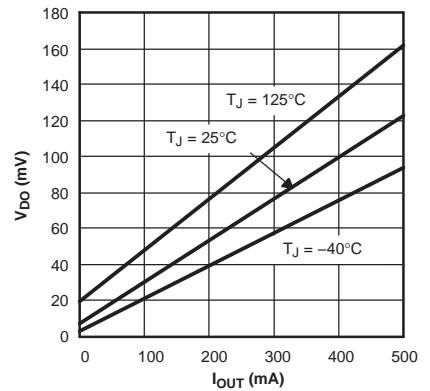


Figure 18.

TYPICAL CHARACTERISTICS (continued)

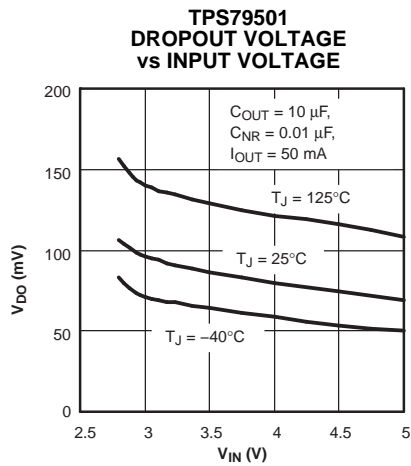


Figure 19.

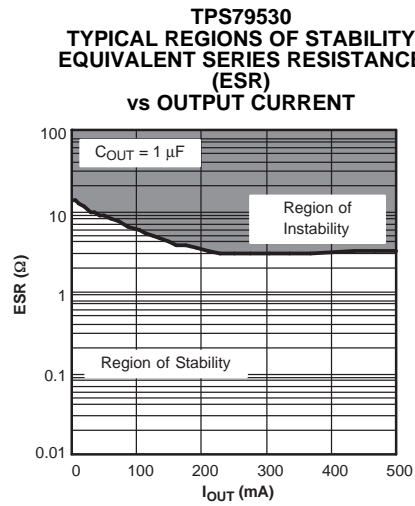


Figure 20.

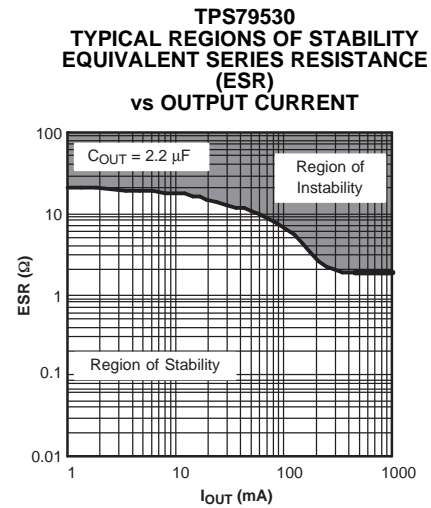


Figure 21.

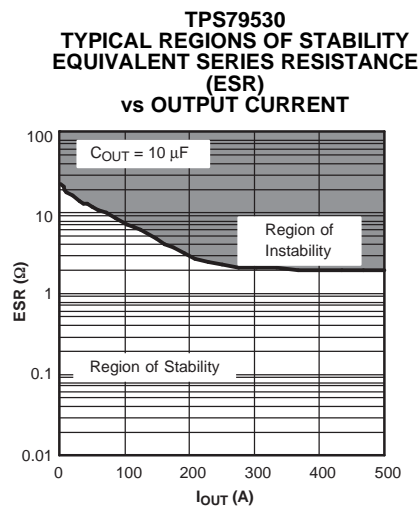
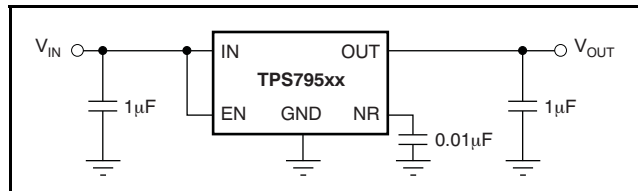


Figure 22.

## APPLICATION INFORMATION

The TPS795xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265  $\mu\text{A}$  typically), and an enable input to reduce supply currents to less than 1  $\mu\text{A}$  when the regulator is turned off.

A typical application circuit is shown in [Figure 23](#).



**Figure 23. Typical Application Circuit**

### EXTERNAL CAPACITOR REQUIREMENTS

Although not required, it is good analog design practice to place a 0.1  $\mu\text{F}$  — 2.2  $\mu\text{F}$  capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS795xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1  $\mu\text{F}$ . Any 1  $\mu\text{F}$  or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS795xx has an NR pin which is connected to the voltage reference through a 250-k $\Omega$  internal resistor. The 250-k $\Omega$  internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum,

because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1- $\mu\text{F}$  in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the [Functional Block Diagram](#).

For example, the TPS79530 exhibits only 33  $\mu\text{V}_{\text{RMS}}$  of output voltage noise using a 0.1- $\mu\text{F}$  ceramic bypass capacitor and a 10- $\mu\text{F}$  ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-k $\Omega$  resistor and external capacitor.

### BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ , with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

### REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report [SBFA015](#), *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site ([www.ti.com](http://www.ti.com)).



## PROGRAMMING THE TPS79501 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79501 adjustable regulator is programmed using an external resistor divider as shown in [Figure 24](#). The output voltage is calculated using [Equation 1](#):

$$V_{\text{OUT}} = V_{\text{REF}} \times \left( 1 + \frac{R_1}{R_2} \right) \quad (1)$$

where:

- $V_{\text{REF}} = 1.2246 \text{ V}$  typ (the internal reference voltage)

Resistors  $R_1$  and  $R_2$  should be chosen for approximately 40- $\mu\text{A}$  divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose  $R_2 = 30.1 \text{ k}\Omega$  to set the divider current at 40  $\mu\text{A}$ ,  $C_1 = 15 \text{ pF}$  for stability, and then calculate  $R_1$  using [Equation 2](#):

$$R_1 = \left( \frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right) \times R_2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated as [Equation 3](#):

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within [Figure 24](#). If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2  $\mu\text{F}$  instead of 1  $\mu\text{F}$ .

## REGULATOR PROTECTION

The TPS795xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS795xx features internal current limiting and thermal protection. During normal operation, the TPS795xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

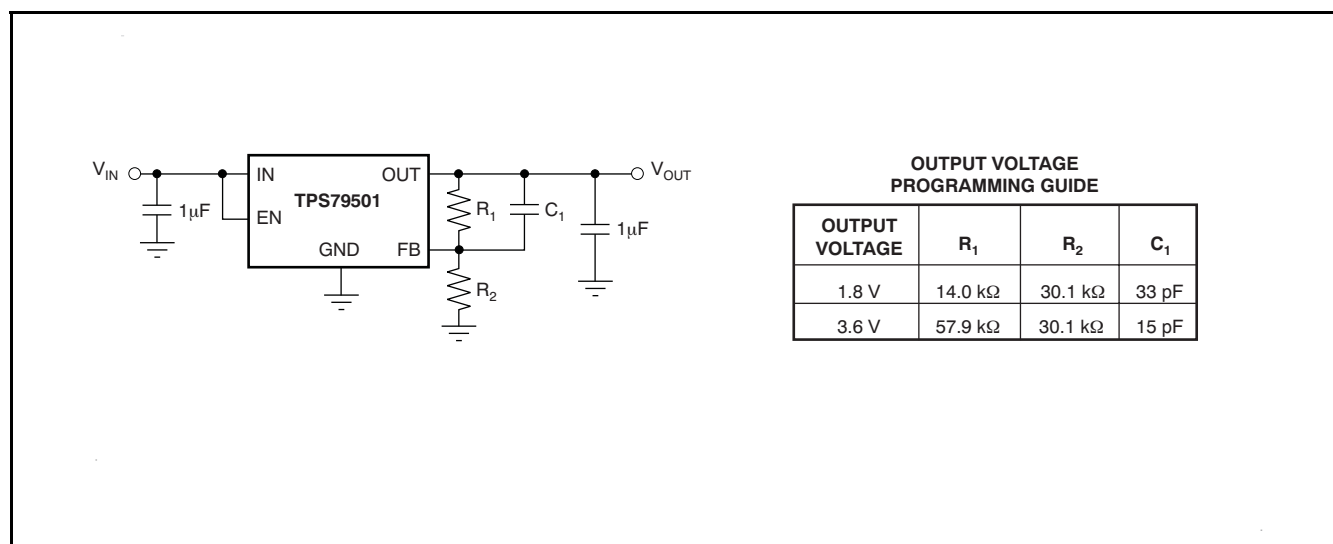


Figure 24. TPS79501 Adjustable LDO Regulator Programming

## THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ( $T_{Jmax}$ ) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature ( $T_J$ ) does not exceed the maximum junction temperature ( $T_{Jmax}$ ). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ( $P_{Dmax}$ ) consumed by a linear regulator is computed as shown in [Equation 4](#):

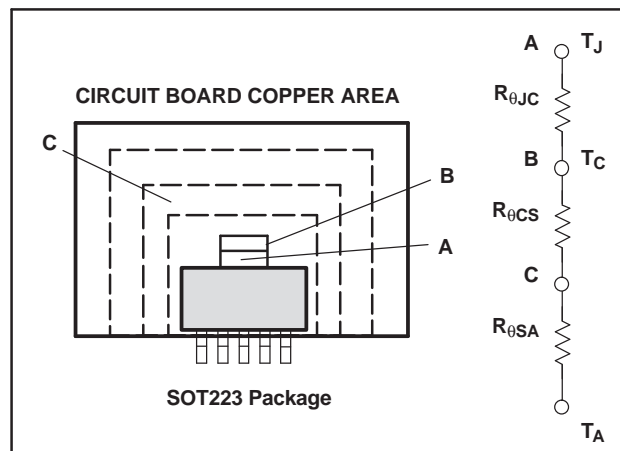
$$P_{Dmax} = (V_{IN(av)} - V_{OUT(av)}) \times I_{OUT(av)} + V_{I(av)} \times I_Q \quad (4)$$

where:

- $V_{IN(av)}$  is the average input voltage
- $V_{OUT(av)}$  is the average output voltage
- $I_{OUT(av)}$  is the average output current
- $I_Q$  is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term  $V_{IN(av)} \times I_Q$  can be neglected. The operating junction temperature is computed by adding the ambient temperature ( $T_A$ ) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ( $R_{\theta JC}$ ), the case to heatsink ( $R_{\theta CS}$ ), and the heatsink to ambient ( $R_{\theta SA}$ ). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

[Figure 25](#) illustrates these thermal resistances for a SOT223 package mounted in a JEDEC low-K board.



**Figure 25. Thermal Resistances**

[Equation 5](#) summarizes the computation:

$$T_J = T_A + P_{Dmax} \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (5)$$

The  $R_{\theta JC}$  is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The  $R_{\theta SA}$  is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have  $R_{\theta CS}$  values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The  $R_{\theta CS}$  is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package,  $R_{\theta CS}$  of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ( $R_{\theta JA}$ ). This  $R_{\theta JA}$  is valid only for the specific operating environment used in the computer model.

Equation 5 simplifies into Equation 6:

$$T_J = T_A + P_{D \max} \times R_{\theta JA} \quad (6)$$

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{D \max}} \quad (7)$$

Using Equation 6 and the computer model generated curves shown in Figure 26, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

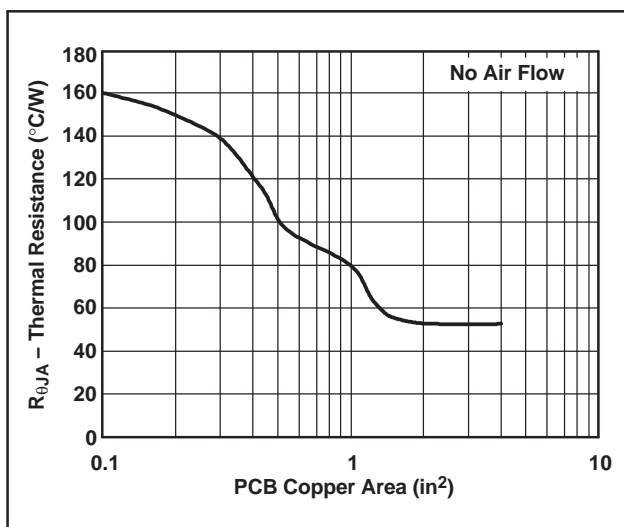


Figure 26. SOT223 Thermal Resistance vs PCB Copper Area

### SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface-mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS79525 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is Equation 8:

$$P_{D \max} = (3.3 - 2.5)V \times 1A = 800\text{mW} \quad (8)$$

Substituting  $T_{J \max}$  for  $T_J$  into Equation 4 gives Equation 9:

$$R_{\theta JA \max} = (125 - 55)^\circ\text{C}/800\text{mW} = 87.5^\circ\text{C}/\text{W} \quad (9)$$

From Figure 26,  $R_{\theta JA}$  vs PCB Copper Area, the ground plane needs to be 0.55 in<sup>2</sup> for the part to dissipate 800 mW. The operating environment used to construct Figure 26 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

From the data in Figure 26 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed, as shown in Figure 27.

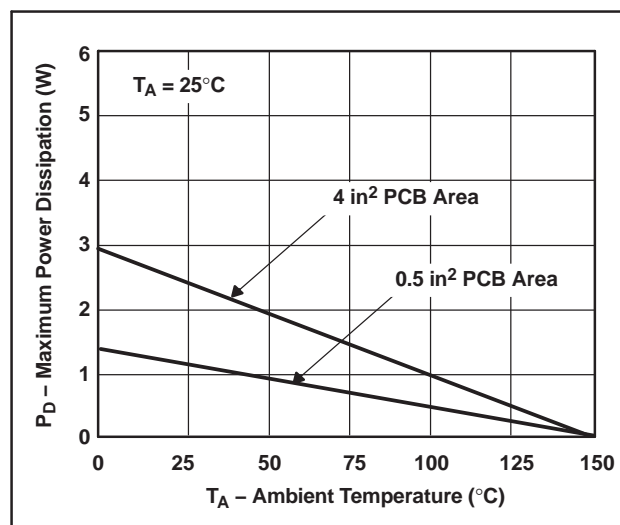


Figure 27. SOT223 Maximum Power Dissipation vs Ambient Temperature

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS79501DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79501DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79501DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79501DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79501DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79501DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79501DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79501DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79516DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
TPS79516DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
TPS79516DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79516DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79518DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79518DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79518DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79518DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79525DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS79525DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79525DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
TPS79525DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Purchase Samples</a>
TPS79530DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79530DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79530DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79530DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79533DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79533DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Contact TI Distributor or Sales Office
TPS79533DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>
TPS79533DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	<a href="#">Request Free Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

---

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79501DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79501DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79516DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79518DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79525DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79530DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79533DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3

**TAPE AND REEL BOX DIMENSIONS**

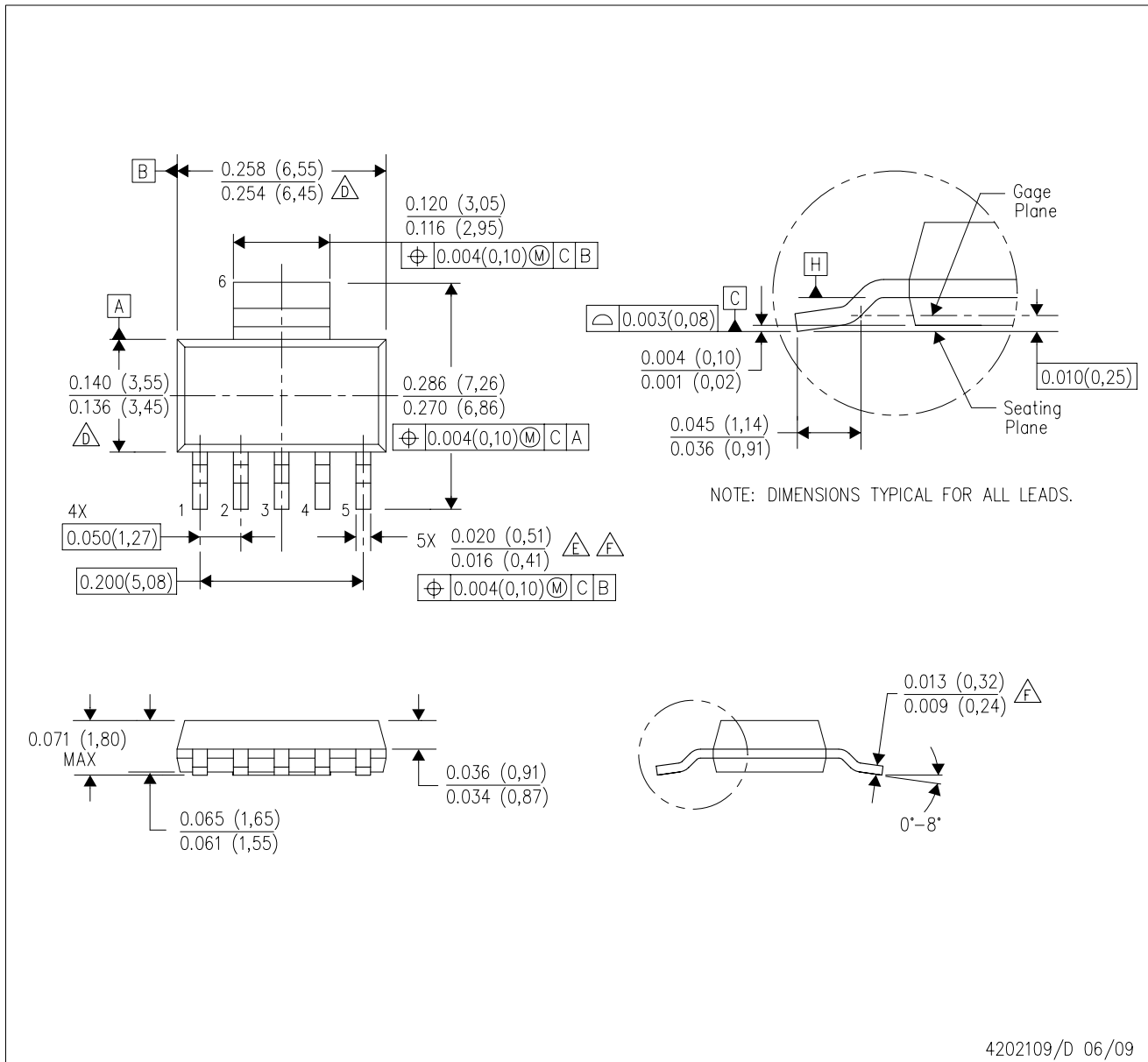

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79501DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79501DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS79501DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS79516DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79518DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79525DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79530DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79533DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0



DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE

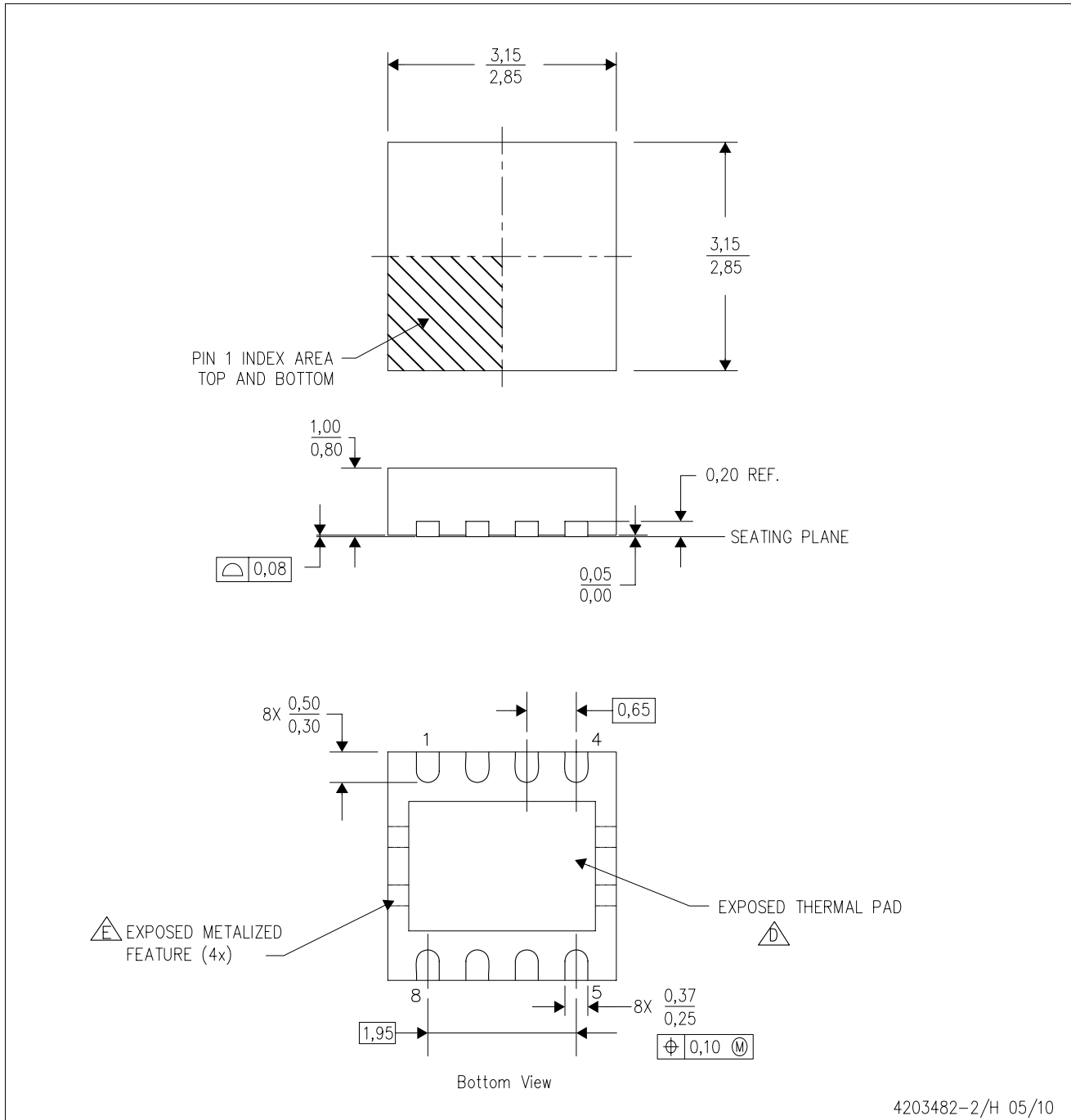


4202109/D 06/09

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Controlling dimension in inches.
  - $\triangle D$  Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
  - $\triangle E$  Lead width dimension does not include dambar protrusion.
  - $\triangle F$  Lead width and thickness dimensions apply to solder plated leads.
  - G. Interlead flash allow 0.008 inch max.
  - H. Gate burr/protrusion max. 0.006 inch.
  - I. Datums A and B are to be determined at Datum H.

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Metalized features are supplier options and may not be on the package.

## THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

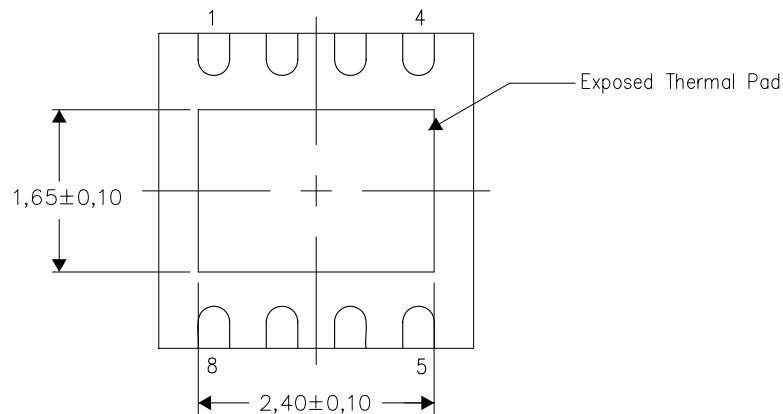
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

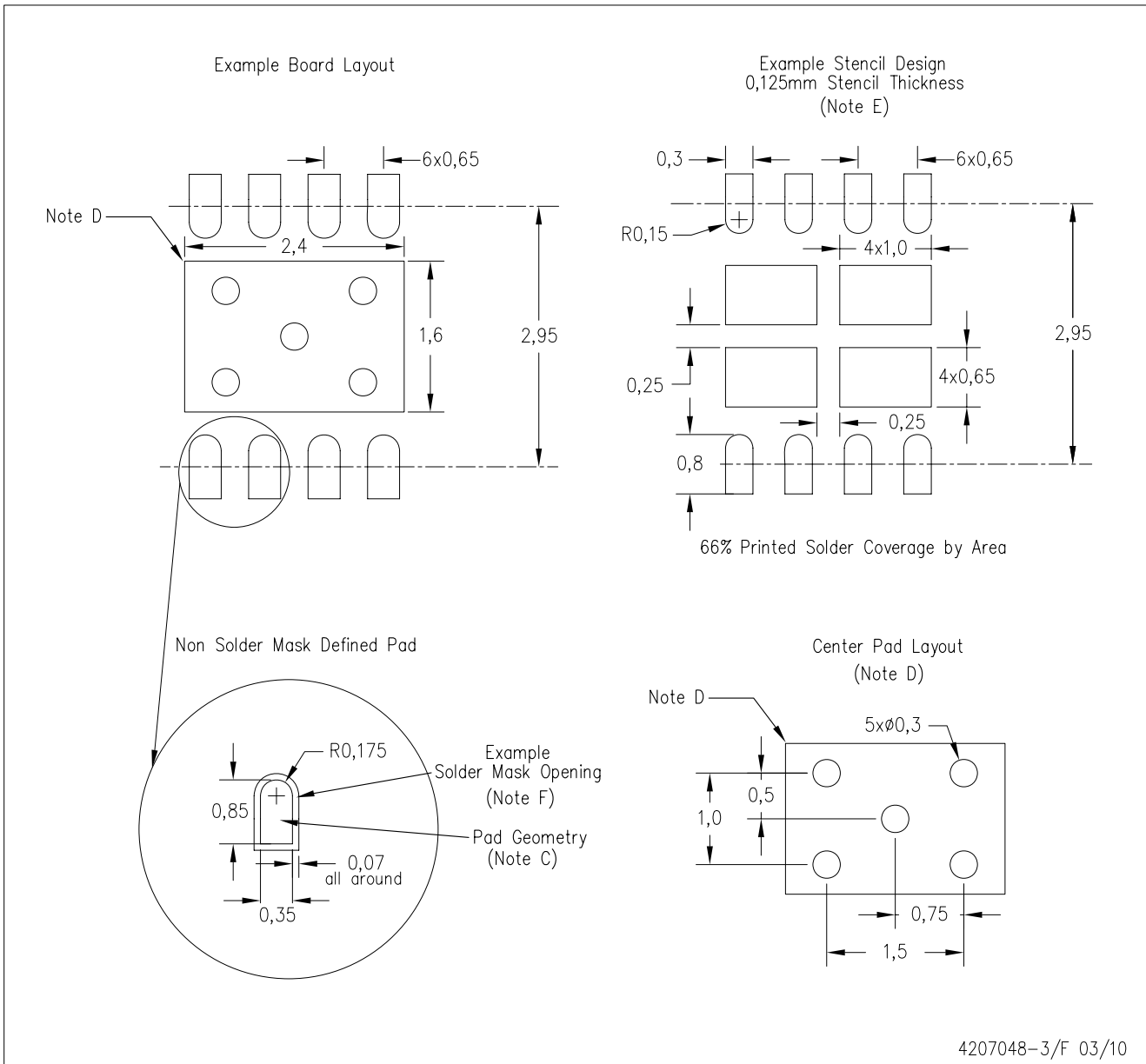
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206340-3/J 07/10

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2010, Texas Instruments Incorporated