Atmel AVR Microcontroller Family - Product Selection Guide

DEVICE	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103		
ON-CHIP MEMORY											
FLASH (Bytes)	1K	2K	2K	4K	8K	2K	8K	64K	128K		
EEPROM (Bytes)	64	128	128	256	512	128	512	2K	4K		
SRAM (Bytes)	0	128	128	256	512	128	512	4K	4K		
In-System Programmable (ISP)	YES	YES	YES	YES	YES	YES	YES	YES	YES		
HARDWARE FEATURES											
I/O Pins	15	15	5	32	32	20	32	32I/O, 8O, 8I	32I/O, 8O, 8I		
On-chip RC Oscillator	YES	NO	YES	NO	NO	NO	NO	NO	NO		
Real Time Clock (RTC)	NO	NO	NO	NO	NO	NO	NO	YES	YES		
SPI Port	NO	NO	NO	YES	YES	YES	YES	YES	YES		
Full Duplex Serial UART	NO	YES	NO	YES	YES	YES	YES	1	1		
Watchdog Timer	YES	YES	YES	YES	YES	YES	YES	YES	YES		
Timer/Counters	1	2	2	2	2	2	2	3	3		
PWM Channels (10-bit)	-	1	-	2	2	1	TBA	2	2		
Analogue Comparator	YES	YES	NO	NO	NO	NO	NO	NO	NO		
ADC	NO	NO	NO	NO	NO	6CH/10BIT	8CH/10BIT	8CH/10BIT	8CH/10BIT		
IDLE and Power Down modes	YES	YES	YES	YES	YES	YES	YES	YES	YES		
Interrupts	4	11	3	13	13	14	17	24	24		
MISCELLANEOUS											
AVR Instructions	89	118	118	118	118	118	120	121	121		
Max External Clock Frequency	12MHz	10MHz	10MHz	8MHz	8MHz	8MHz	8MHz	6MHz	6MHz		
Vcc Voltage Range (V)	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V		
EQUINOX SUPPORT TOOLS										**Farnell Order Code**	**Equinox Order Code**
AVR Starter System	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP only	ACT-UPG1	ACT-UPG1	111-806	EQ-8051-ST1 (UK)
AVR Development System	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	UISP-UPG1	UISP-UPG1	302-2249	AVR-DV1 (UK)
Micro-ISP Series IV Programmer	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	302-2286	UISP-S4
Micro-ISP Series IV LV Prog.	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	302-2298	UISP-LV4
Micro-Pro Device Programmer	PAR only	PAR only	-	ZIF-ISP	ZIF-ISP	-	-	-	-	111-715	MPW-PLUS (UK)
AllWriter Universal Programmer	PAR	PAR	-	PAR	PAR	-	-	-	-	302-2225	SG-ALLWRITER
AVR BASIC LITE	YES (1K)	-	-	-	-	-	-	-	-	111-788	AVR-BAS-LIT
AVR BASIC FULL	YES	YES	YES	YES	YES	YES	YES	YES	YES	302-2330	AVR-BAS-FULL
AT90S8515 Socket Stealer (DIL-40)	NO	NO	NO	YES	YES	NO	NO	NO	NO	302-2365	SS-90S8515-P

** Max speed depends on Vcc voltage. Frequencies and Currents listed are for Vcc = 5.0V & T = 25ºC*

Please verify correct part codes for low voltage parts before ordering.

Key

- **SRAM** - Static RAM
- **ISP** - In-System Programmable
- **I/O** - Input/Output
- **ADC** - Analogue to Digital Convertor
- **SPI** - Serial Peripheral Interface
- **PWM** - Pulse Width Modulation
- **PAR** - Parallel programming mode
- **FLASH** - Reprogrammable Code Memory
- **EEPROM** - Parallel programming mode

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***Disclaimer*:** Whilst information is supplied in good faith, we are not liable for any errors or omissions. Please consult the relevant Atmel datasheet. E&OE

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The Embedded Solutions Company

Atmel AVR Microcontroller Family - Product Selection Guide

Continued....

Device	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103	Farnell Order Code	Equinox Order Code
EQUINOX SUPPORT TOOLS											
AT90S8515 Socket Stealer (PLCC)	NO	NO	NO	YES	YES	NO	NO	NO	NO	303-1068	SS-90S8515-J
DOBOX-MOD1	YES	YES	YES	YES	YES	NO	YES	NO	NO	121-022	UC-PM1
PACKAGE TYPES (Farnell Codes)											
6AC	-	-	-	-	-	-	-	120-984	120-972		
8JC	-	-	-	111-480	111-508	-	120-959	-	-		
8PC	-	-	-	111-478	111-491	-	120-960	-	-		
10PC	-	111-454	111-430	-	-	-	-	-	-		
10SC	-	111-466	111-442	-	-	-	-	-	-		
12PC	690-752	-	-	-	-	-	-	-	-		
12SC	690-934	-	-	-	-	-	-	-	-		

Errata

- **Reset During EEPROM Write**
- **Verifying EEPROM in System**
- **Serial Programming at Voltages below 3.0 Volts**

3. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

2. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.

1. Serial Programming at Voltages below 3.0 Volts

At voltages below 3.0 Volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 3.0 Volts or higher during In-System Programming.

8-Bit AVR® Microcontroller with 1K bytes In-System Programmable Flash

AT90S1200/A Rev. F Errata Sheet

Rev. 1190B–01/99

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1190B–01/99/xM

8-bit AVR® Microcontroller with 1K bytes In-System Programmable Flash

AT90S1200

Features

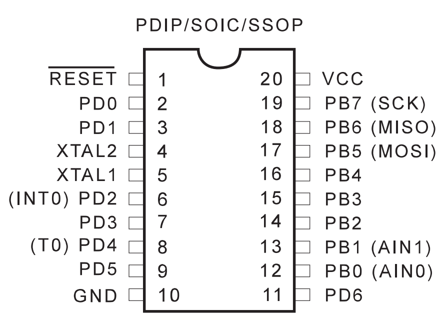
- Utilizes the AVR® RISC Architecture
- AVR - High-performance and Low-power RISC Architecture
  - 89 Powerful Instructions - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Up to 12 MIPS Throughput at 12 MHz
- Data and Nonvolatile Program Memory
  - 1K Bytes of In-System Programmable Flash
    Endurance: 1,000 Write/Erase Cycles
  - 64 Bytes of In-System Programmable EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with On-chip Oscillator
  - SPI Serial Interface for In System Programming
- Special Microcontroller Features
  - Low-power Idle and Power Down Modes
  - External and Internal Interrupt Sources
  - Selectable On-chip RC Oscillator for Zero External Components
- Specifications
  - Low-power, High-speed CMOS Process Technology
  - Fully Static Operation
- Power Consumption at 4 MHz, 3V, 25°C
  - Active: 2.0 mA
  - Idle Mode: 0.4 mA
  - Power Down Mode: <1 µA
- I/O and Packages
  - 15 Programmable I/O Lines
  - 20-pin PDIP and SOIC
- Operating Voltages
  - 2.7 - 6.0V (AT90S1200-4)
  - 4.0 - 6.0V (AT90S1200-12)
- Speed Grades
  - 0 - 4 MHz, (AT90S1200-4)
  - 0 - 12 MHz, (AT90S1200-12)

Description

The AT90S1200 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the

(continued)

Pin Configuration



Rev. 0838ES–04/99

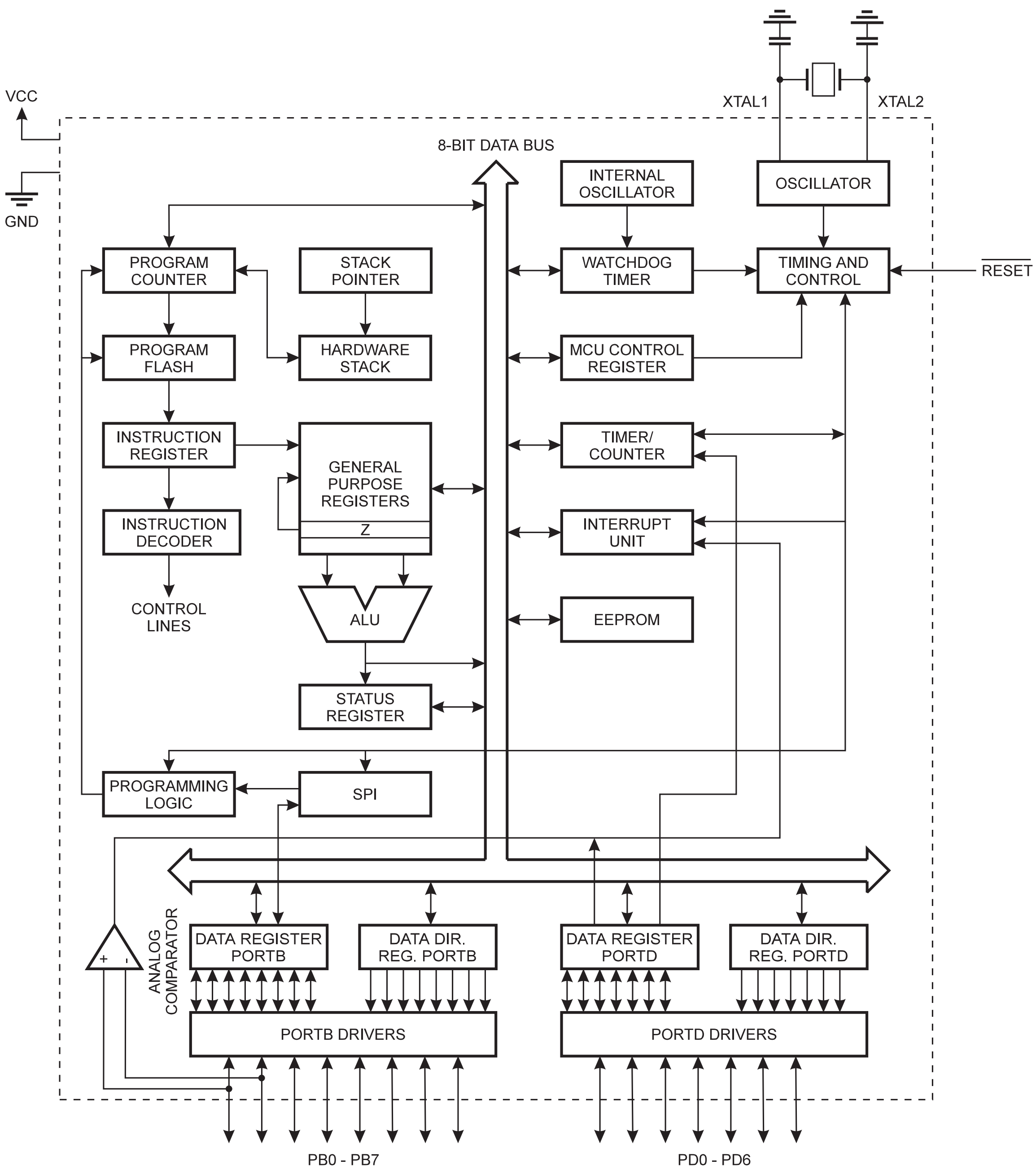
Note: This is a summary document. For the complete 65 page document, please visit our web site at *www.atmel.com* or e-mail at *literature@atmel.com* and request literature #0838E.

AT90S1200 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with the 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Block Diagram

Figure 1. The AT90S1200 Block Diagram



The architecture supports high level languages efficiently as well as extremely dense assembler code programs. The AT90S1200 provides the following features: 1K bytes of In-System Programmable Flash, 64 bytes EEPROM, 15 general purpose I/O lines, 32 general purpose working registers, internal and external interrupts, programmable Watchdog Timer with internal oscillator, an SPI serial port for program downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the registers, timer/counter, watchdog and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The device is manufactured using Atmel’s high density non-volatile memory technology. The on-chip In-System Programmable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S1200 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S1200 AVR is supported with a full suite of program and system development tools including: macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). PB0 and PB1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip analog comparator. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Port D (PD6..PD0)

Port D has seven bi-directional I/O pins with internal pull-up resistors, PD6..PD0. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

$\overline{\text{RESET}}$

Reset input. A low level on this pin for more than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

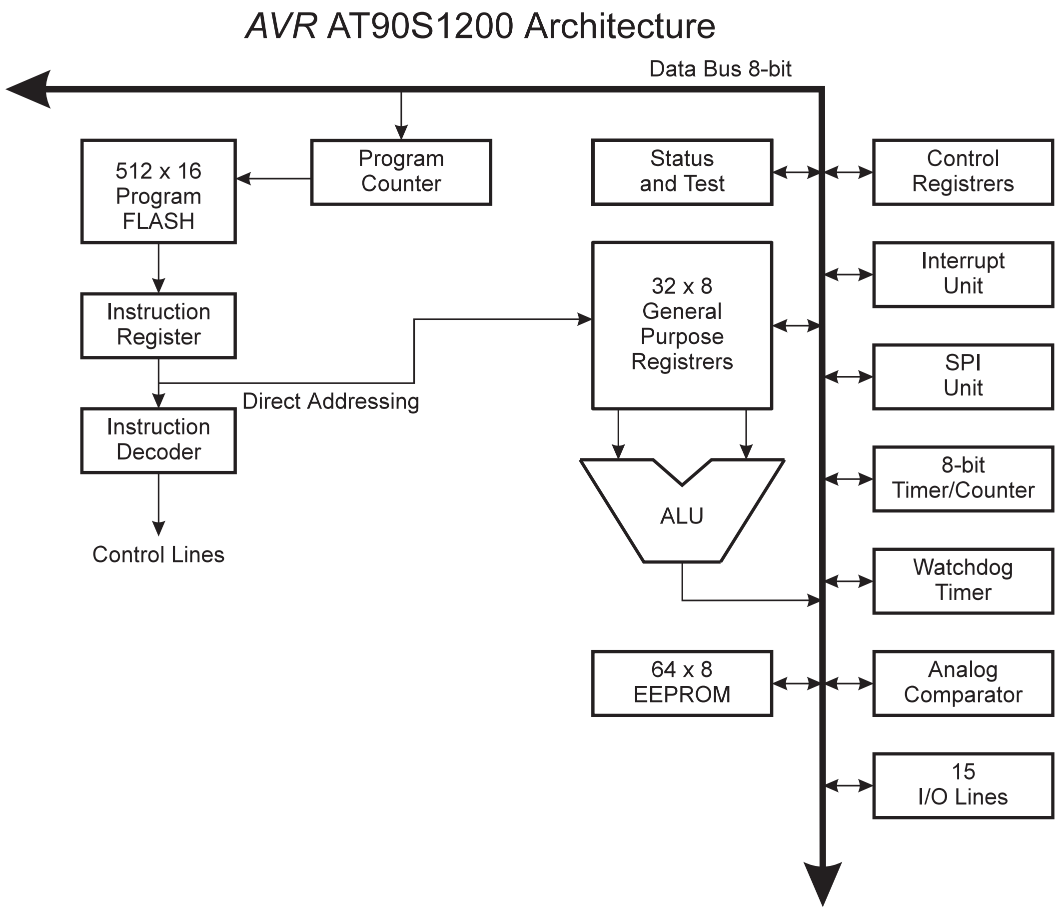
XTAL2

Output from the inverting oscillator amplifier.

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file - in one clock cycle.

Figure 2. The AT90S1200 AVR Enhanced RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 2 shows the AT90S1200 AVR Enhanced RISC microcontroller architecture. The AVR uses a Harvard architecture concept - with separate memories and buses for program and data memories. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and relative call instructions, the whole 512 address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is a 3 level deep hardware stack dedicated for subroutines and interrupts.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

AT90S1200 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$3F	SREG	I	T	H	S	V	N	Z	C
$3E	Reserved								
$3D	Reserved								
$3C	Reserved								
$3B	GIMSK	-	INT0	-	-	-	-	-	-
$3A	Reserved								
$39	TIMSK	-	-	-	-	-	-	TOIE0	-
$38	TIFR	-	-	-	-	-	-	TOV0	-
$37	Reserved								
$36	Reserved								
$35	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00
$34	Reserved								
$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00
$32	TCNT0	Timer/Counter0 (8 Bit)							
$31	Reserved								
$30	Reserved								
$2F	Reserved								
$2E	Reserved								
$2D	Reserved								
$2C	Reserved								
$2B	Reserved								
$2A	Reserved								
$29	Reserved								
$28	Reserved								
$27	Reserved								
$26	Reserved								
$25	Reserved								
$24	Reserved								
$23	Reserved								
$22	Reserved								
$21	WDTCR	-	-	-	-	WDE	WDP2	WDP1	WDP0
$20	Reserved								
$1F	Reserved								
$1E	EEAR	-	EEPROM Address Register						
$1D	EEDR	EEPROM Data Register							
$1C	EECR	-	-	-	-	-	-	EEWE	EERE
$1B	Reserved								
$1A	Reserved								
$19	Reserved								
$18	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
$17	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
$16	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
$15	Reserved								
$14	Reserved								
$13	Reserved								
$12	PORTD	-	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0
$11	DDRD	-	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
$10	PIND	-	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
$0F	Reserved								
...	Reserved								
$09	Reserved								
$08	ACSR	ACD	-	ACO	ACI	ACIE	-	ACIS1	ACIS0
…	Reserved								
$00	Reserved								

Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd⊕Rr	Z,N,V	1
COM	Rd	One’s Complement	Rd ← $FF - Rd	Z,C,N,V	1
NEG	Rd	Two’s Complement	Rd ← $00 - Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (FFh - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd⊕Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2
CP	Rd,Rr	Compare	Rd - Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd - K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
DATA TRANSFER INSTRUCTIONS					
LD	Rd,Z	Load Register Indirect	Rd ← (Z)	None	2
ST	Z,Rr	Store Register Indirect	(Z) ← Rr	None	2
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1

Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	3
WDR		Watch Dog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information[1]

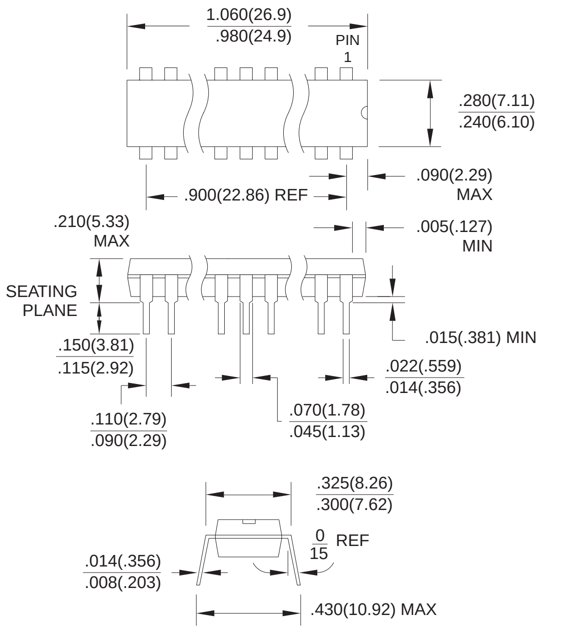
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
4	2.7 - 6.0V	AT90S1200-4PC AT90S1200-4SC AT90S1200-4YC	20P3 20S 20Y	Commercial (0°C to 70°C)
		AT90S1200-4PI AT90S1200-4SI AT90S1200-4YI	20P3 20S 20Y	Industrial (-40°C to 85°C)
12	4.0 - 6.0V	AT90S1200-12PC AT90S1200-12SC AT90S1200-12YC	20P3 20S 20Y	Commercial (0°C to 70°C)
		AT90S1200-12PI AT90S1200-12SI AT90S1200-12YI	20P3 20S 20Y	Industrial (-40°C to 85°C)

Note: 1. Order AT90S1200A-XXX for devices with the RCEN fuse programmed.

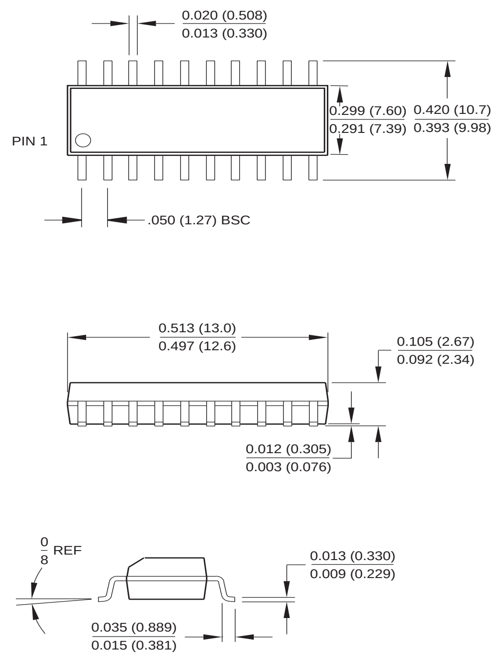
Package Type	
20P3	20-lead, 0.300" Wide Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)
20Y	20-lead, 5.3 mm Wide, Plastic Shrink Small Outline Package (SSOP)

Packaging Information

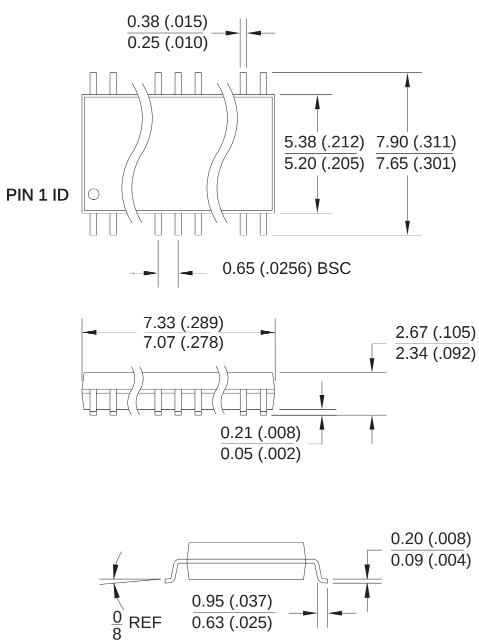
20P3, 20-lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



20S, 20-lead, 0.300" Wide,
Plastic Gull-Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



20Y, 20-lead, 5.3 mm Wide,
Plastic Shrink Small Outline Package (SSOP)
Dimensions in Millimeters and (Inches)



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