2.25 MHz Step Down Converter with Dual LDOs and SVS

FEATURES

- **Step-Down Converters:**
  - **V_{IN} Range From 2.3V to 6V**
  - **Spread Spectrum Clock (SSC) Generation for Reduced EMI**
  - **2.25MHz Fixed Frequency Operation**
  - **600mA Output Current**
- **LDOs:**
  - **V_{IN} Range From 1.6V to 6V**
  - **Adjustable Output Voltage**
  - **Up to 300mA Output Current**
  - **Separate Power Inputs and Enables**
- **Supply Voltage Supervisor (TPS65001)**
  - **Manual Reset Input for Push Button**
  - **Adjustable Reset Time**
  - **Adjustable Reset Voltage**
- **3mm × 3mm 16-Pin QFN (TPS65000)**
- **3mm x×3mm 20-Pin QFN (TPS65001)**

APPLICATIONS

- **Point of Load**
- **Embedded Processor Power**
- **Cell Phones, Smart-Phones**
- **PDAs, Pocket PCs**
- **Portable Media Players**

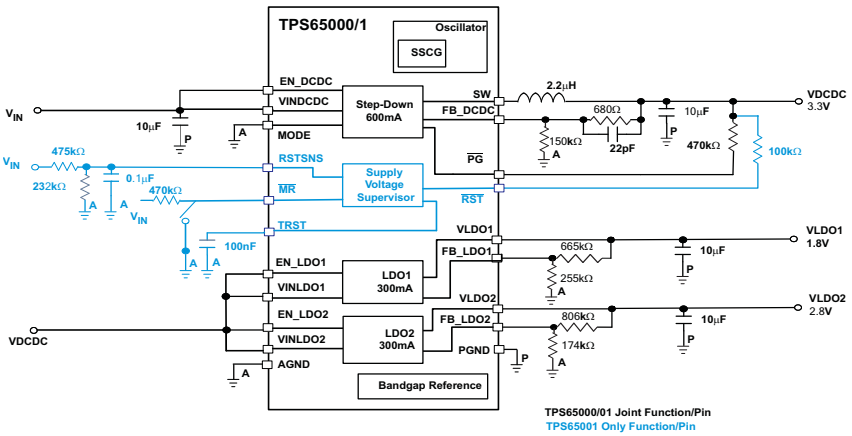
DESCRIPTION

The TPS65000 and TPS65001 are single chip Power Management ICs for portable applications. Both devices combine a single step-down converter with two low dropout regulators. The step-down converter enters a low power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications, the devices can be forced into fixed frequency PWM via a pin. The step-down converter allows the use of a small inductor and capacitors to achieve a small solution size. The step-down converter has Power Good status output that can be used for sequencing. The LDOs are capable of supplying 300mA, and can operate with an input voltage range between 1.6V and 6V, allowing them to be supplied from the step-down converter or directly from the main battery. The step-down converter and the LDOs have separate voltage inputs and enables, allowing for design and sequencing flexibility.

The TPS65000 is available in a 16-pin leadless package (3mm × 3mm QFN).

The TPS65001 extends functionality by adding a Supply Voltage Supervisor (SVS). The SVS allows maximum flexibility by having the reset voltage set with two external resistors, and the reset time set by a small external capacitor. In addition, an active low Manual Reset input allows the SVS to be connected to a push button for external control.

The TPS65001 is available in a 20-pin leadless package (3mm × 3mm QFN).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER(1)	PACKAGE	PACKAGE DESIGNATOR	OPTIONS	SVS	SSC	ORDERING(2)	PACKAGE MARKING
–40°C to 85°C	TPS65000	QFN 3×3 16	RTE	LDO voltages externally adjustable DCDC converters 600mA, V_{OUT} externally adjustable	N/A	Included	TPS65000RTE	TPS65000
	TPS65001	QFN 3×3 20	RUK		Included	Included	TPS65001RUK	TPS65001

(1) Different DCDC current limits and fixed voltage outputs of the DCDC and LDOs are available. Please contact your Texas Instruments sales representative for further information.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range	On all pins except AGND, PGND, EN_DCDC, VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC pins with respect to AGND	–0.3	7	V
	On EN_DCDC with respect to AGND	-0.3	V_{IN} + 0.3, ≤ 7	
Output voltage range	On VLDO1, VLDO2, FB_LDO1, FB_LDO2, FB_DCDC	-0.3	3.6	V
Current	VINDCDC, SW, PGND,		1800	mA
	VINLDO1/2, VLDO1/2, AGND		800	mA
	at all other pins		1	mA
Continuous total power dissipation		See dissipation rating table		
Operating free-air temperature, T_A		-40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

DEVICE	PACKAGE	$R_{\theta JA}$	$R_{\theta JB}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
TPS65000/01(1)	RTE / RUK	270°C/W	14°C/W	370 mW	204 mW	148 mW
TPS65000/01(2)		48.7°C/W	14°C/W	2.05 W	1.13 W	821 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$I_{O(DCDC)}$	DCDC converter output current			600	mA
L1	SW pin inductor	1.5	2.2	3.3	µH
$C_{I(DCDC)}$	Input capacitor at VINDCDC	10			µF
$C_{O(DCDC)}$	Output capacitor for DCDC	10		22	µF
$C_{I(LDO1/2)}$	Input capacitor at VINLDO1/2	2.2			µF
$C_{O(LDO1/2)}$	Output capacitor for LDO1/2	2.2			µF
$I_{O(LDO1)}$	LDO1 output current			300	mA
$I_{O(LDO2)}$	LDO2 output current			300	mA
T_A	Operating ambient temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the parameter measurement information).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
V_{IN}	Input voltage for VINDCDC of DCDC converter		2.3		6	V
VINLDO1	Input voltage for LDO1	See (1)	1.6		6	
VINLDO2	Input voltage for LDO2	See (1)	1.6		6	
UVLO	Internal undervoltage lockout threshold	V_{CC} falling	1.72	1.77	1.82	V
	Internal undervoltage lockout hysteresis			160		mV
SUPPLY CURRENT TPS65000						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1/2 low, I_{OUT} = 0 mA and no switching		23	32	µA
		MODE low, EN_DCDC low, EN_LDO1/2 high, I_{OUT} = 0mA		50	57	
		EN_DCDC high, MODE high, EN_LDO1/2 low, I_{OUT} = 0mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		0.16	2.2	µA
SUPPLY CURRENT TPS65001						
I_Q	Operating quiescent current	MODE low, EN_DCDC high, EN_LDO1/2 low, I_{OUT} = 0 mA and no switching		24	37	µA
		MODE low, EN_DCDC low, EN_LDO1/2 high, I_{OUT} = 0mA		55	62	µA
		EN_DCDC high, MODE high, EN_LDO1/2 low, I_{OUT} = 0mA		4		mA
I_{SD}	Shutdown Current	EN_DCDC low EN_LDO1 and EN_LDO2 low		11	17	µA
DIGITAL PINS (EN_DCDC, EN_LDO1, EN_LDO2, MODE, $\overline{PG}$, $\overline{MR}$, $\overline{RST}$						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.4	V
V_{OL}	Low level output voltage	$\overline{PG}$ and $\overline{RST}$ pins only, I_O = -100µA			0.4	V
I_{lkg}	Input leakage current	MODE, EN_DCDC, EN_LDO1, EN_LDO2 tied to GND or VINDCDC		0.01	0.1	µA

(1) The design principle allows only VINDCDC to be the highest supply in the system if different voltage input supplies separately to DCDC converter and LDOs, meaning VINDCDC ≥ VINLDO1, VINDCDC ≥ VINLDO2.

ELECTRICAL CHARACTERISTICS (continued)

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the parameter measurement information).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Oscillator frequency		1.722	2.25	2.847	MHz
STEP DOWN CONVERTER POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	VINDCDC = V_{GS} = 3.6V		240	480	mΩ
	Low side MOSFET on-resistance			185	380	
I_O	DC output current	2.3 V ≤ VINDCDC ≤ 2.5V			300	mA
		2.5 V ≤ VINDCDC ≤ 6V			600	
I_{LIMF}	Forward current limit PMOS and NMOS	2.3 V ≤ VINDCDC ≤ 6V	800	1000	1400	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		30		
STEP DOWN CONVERTER OUTPUT VOLTAGE						
VDCDC	Adjustable output voltage range, DCDC		0.6		VINDCDC	V
	FB_DCDC pin current				0.1	µA
V_{ref}	Internal reference voltage		0.594	0.6	0.606	V
VDCDC	Output Voltage Accuracy (PWM Mode)(2)	MODE = high, 2.3 ≤ VINDCDC ≤ 6V	–1.5%	0%	1.5%	
	Output Voltage Accuracy (PFM mode) (3)	MODE low +1% voltage positioning active		1%		
	Load regulation (PWM mode)	MODE high		0.5		%/A
t_{Start}	Start-up time	EN_DCDC to start of switching (10%)		250		µs
t_{Ramp}	VDCDC ramp up time	VDCDC ramp from 10% to 90%		250		µs
R_{DIS}	Internal discharge resistance at SW	EN_DCDC low		450		Ω
LOW DROP OUT REGULATORS						
VINLDOx	Input voltage for LDOx		1.6		6	V
VLDOx	Adjustable output voltage, LDOx (4)		0.73		VINLDOx - V_{DO}	V
I_O	Continuous Pass FET Current				300	mA
I_{SC}	Short circuit current limit	2.3V ≤ VINLDOx	340		700	mA
		VINLDOx < 2.3V	210		700	
	FB_LDOx pin current				0.1	µA
	FB_LDOx voltage	Adjustable V_{OUT} mode only		0.5		V
V_{DO}	Dropout Voltage (5)	VINLDOx ≥ 2.3V, I_{OUT} = 250mA			370	mV
		VINLDOx < 2.3V I_{OUT} = 175mA			370	mV
	Output Voltage Accuracy (6)	I_O = 1mA to 300mA, VINLDOx = 2.3 - 6V, VLDOx = 1.2V	-3.5%		3.5%	
		I_O = 1mA to 175mA VINLDOx = 1.6V - 6V, VLDOx = 1.2V	-3.5%		3.5%	
	Load regulation	I_O = 1mA to 300mA VINLDOx = 3.6V VLDOx = 1.2V	-1.5%		1.5%	
	Line regulation	VINLDOx = 1.6V - 6V VLDOx = 1.2V at I_O = 1mA	-0.5%		0.5%	

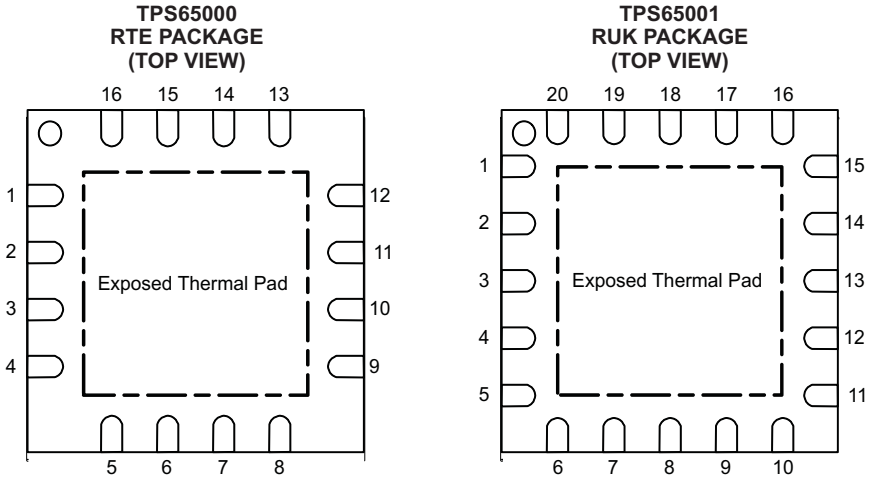
(2) For VINDCDC = VDCDC + 1V
(3) In PFM Mode, the internal reference voltage is typ 1.01 × V_{REF}.
(4) Max output voltage VLDOx = 3.6V.
(5) V_{DO} = VINLDOx - VLDOx where VINLDOx = VLDOx(nom) - 100mV
(6) Output voltage specification does not include tolerance of external programming resistors.

ELECTRICAL CHARACTERISTICS (continued)

Over full operating ambient temperature range, typical values are at T_A = 25° C. Unless otherwise noted, specifications apply for condition V_{IN} = EN_LDOx = EN_DCDC = 3.6 V. External components L = 2.2 µH, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, (see the parameter measurement information).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSSR	Power Supply Rejection Ratio	f_{NOISE} ≤ 10kHz, C_{OUT} ≥ 2.2µF, V_{IN} = 2.3V, V_{OUT} = 1.3V I_{OUT} = 10mA		40		dB
t_{RAMP}	VLDOx Ramp Time	VLDOx ramp from 10% to 90%		200		µs
R_{DIS}	Internal discharge resistance at VLDOx	EN_LDOx low		450		Ω
T_{SD}	Thermal shutdown	Increasing temperature		150		°C
	Thermal shutdown hysteresis	Decreasing temperature		30		°C
SUPPLY VOLTAGE SUPERVISOR						
V_{IN}	Input voltage for RSTSNS pin		0		6	V
$t_{\overline{MR}DEGLITCH}$	$\overline{MR}$ Deglitch time			1		ms
V_{IH}	Input high voltage	$\overline{MR}$ pin only	1.2		6	V
V_{IL}	Input low voltage	$\overline{MR}$ pin only	0		0.4	V
I_{lkg}	High input leakage current	$\overline{RST}$ pin		0.01	0.1	µA
V_{OL}	Output low voltage	$\overline{RST}$ pin only, I_O = -100µA			0.4	V
I_{TRST}	Reset timer capacitor current		1.6	2	2.2	µA
	Reset voltage trip voltage	Voltage rising (Reset time begins)	0.54	0.6	0.66	V
	Reset voltage trip hysteresis	Voltage falling ($\overline{RST}$ pulled low)		-5%		

PIN ASSIGNMENTS

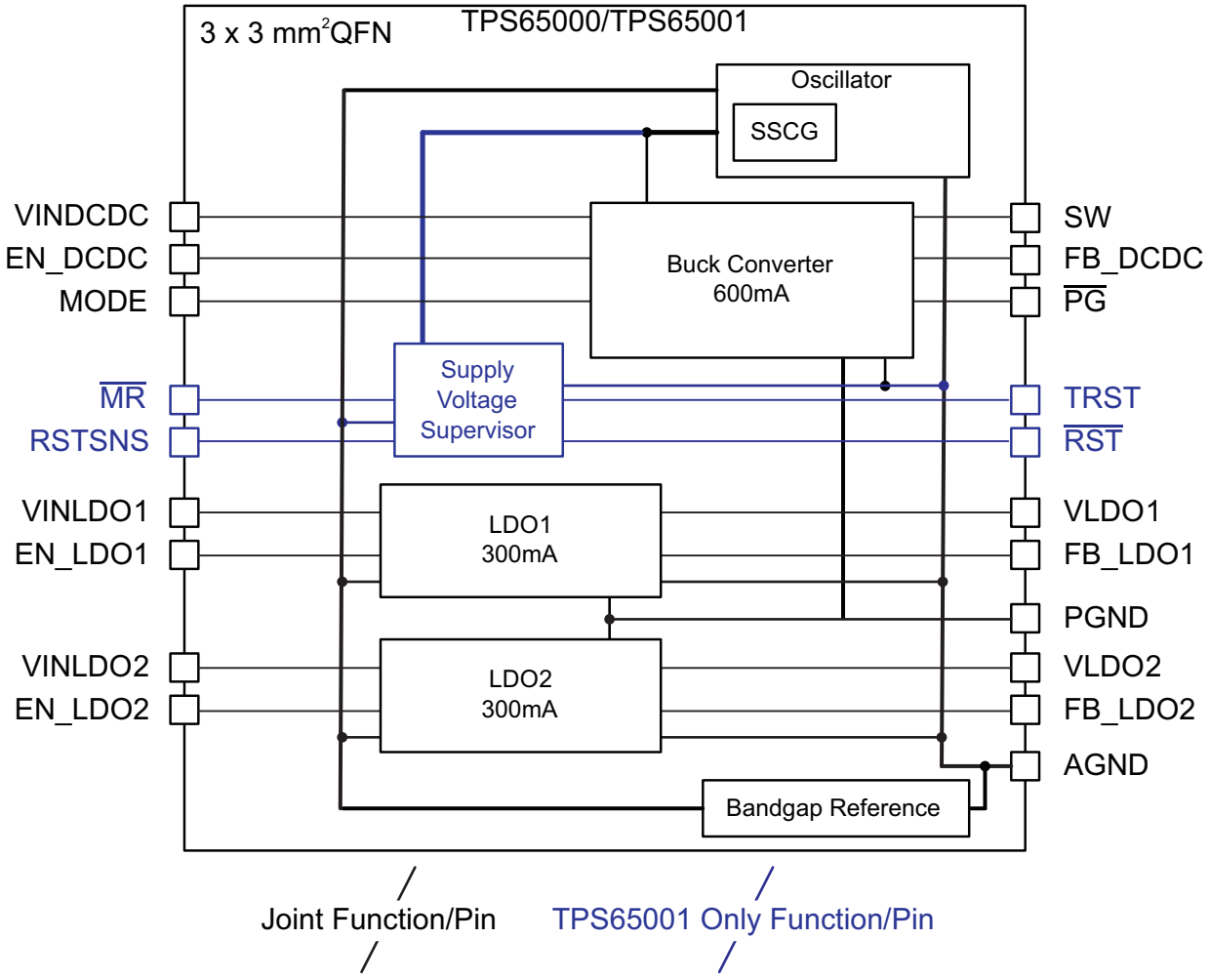


PIN FUNCTIONS

PIN			I/O	DESCRIPTION
NAME	TPS65000	TPS65001		
VINDCDC	6	8	I	Input voltage to DCDC converter and all other control blocks.
EN_DCDC	8	10	I	Enable DCDC converter
MODE	7	9	I	Selects force PWM or PWM/PFM automatic transition mode
VINLDO1	13	15	I	Input voltage to LDO1
EN_LDO1	1	3	I	Enable LDO1
VINLDO2	16	18	I	Input voltage to LDO2
EN_LDO2	2	4	I	Enable LDO2
PGND	4	6		Power ground – Connected to the PowerPAD™
AGND	10	12		Analog ground - Star back to PGND as close to the IC as possible.
$\overline{PG}$	3	5	O	Open drain active low power good output.
SW	5	7	O	Switch pin – connect inductor here
FB_DCDC	9	11	I	Voltage to DCDC error amplifier
VLDO1	12	14	O	LDO1 output voltage
VLDO2	15	17	O	LDO2 output voltage
FB_LDO1	11	13	I	Voltage to LDO1 error amplifier
FB_LDO2	14	16	I	Voltage to LDO2 error amplifier
RSTSNS	–	19	I	Voltage for $\overline{RST}$ generation
$\overline{RST}$	–	20	O	Open drain active low reset output.
$\overline{MR}$	–	1	I	Active low input to force a reset. (1)
TRST	–	2	I/O	Capacitor connection for setting reset time.

(1) External pull up on $\overline{MR}$ is required.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

EFFICIENCY (DCDC PFM Mode) vs OUTPUT CURRENT

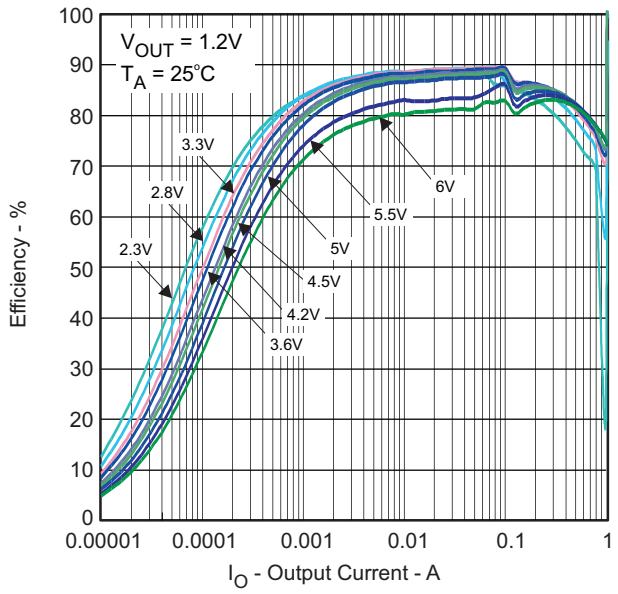


Figure 1.

EFFICIENCY (DCDC PWM Mode) vs OUTPUT CURRENT

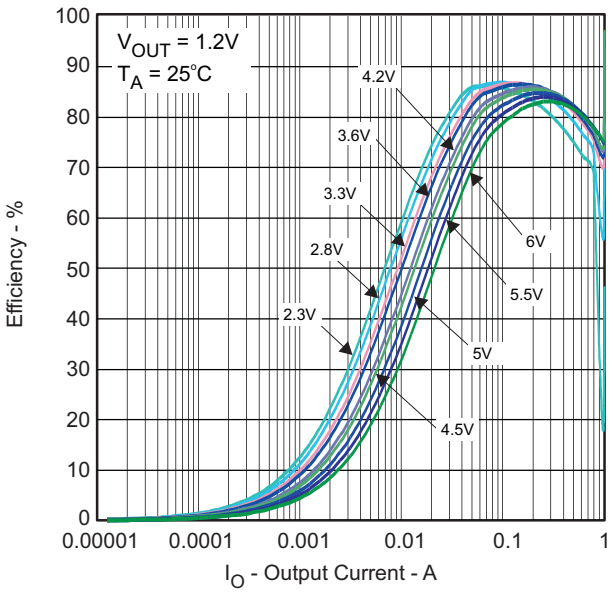


Figure 2.

OUTPUT VOLTAGE RIPPLE (DCDC PFM Mode)

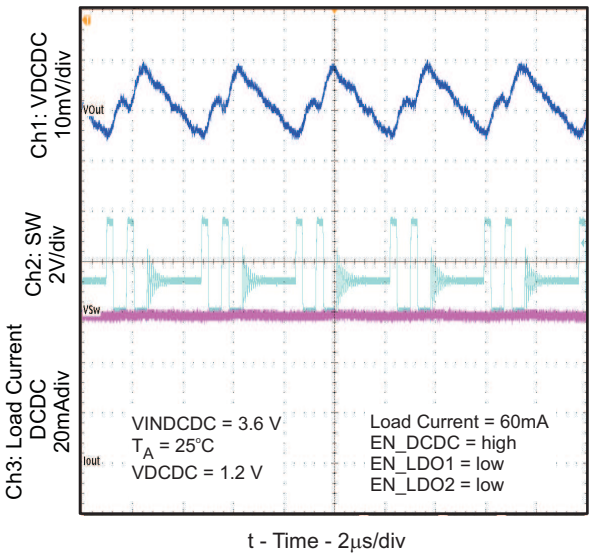


Figure 3.

OUTPUT VOLTAGE RIPPLE (DCDC PWM Mode)

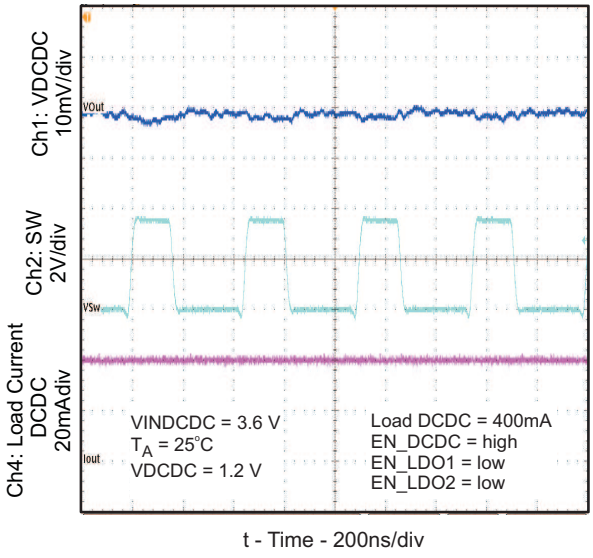


Figure 4.

TYPICAL CHARACTERISTICS (continued)

STARTUP TIMING (DCDC)

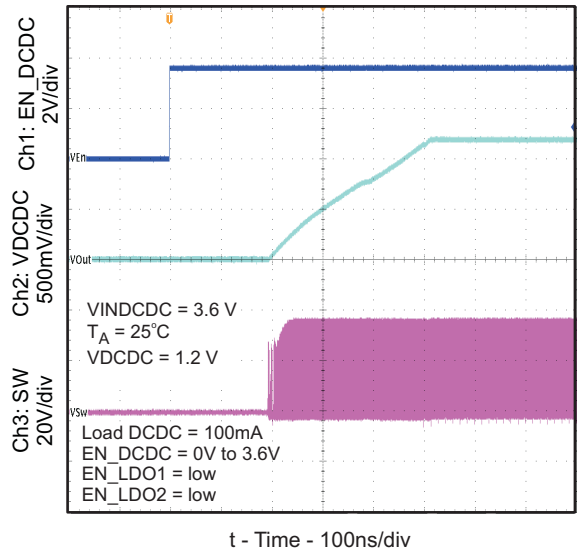


Figure 5.

START-UP TIMING (LDOx)

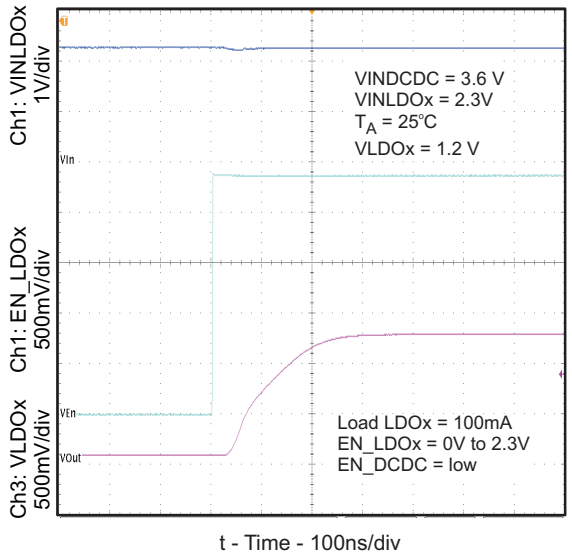


Figure 6.

TPS65001
QUIESCENT CURRENT (DCDC PFM Mode)
vs
INPUT VOLTAGE

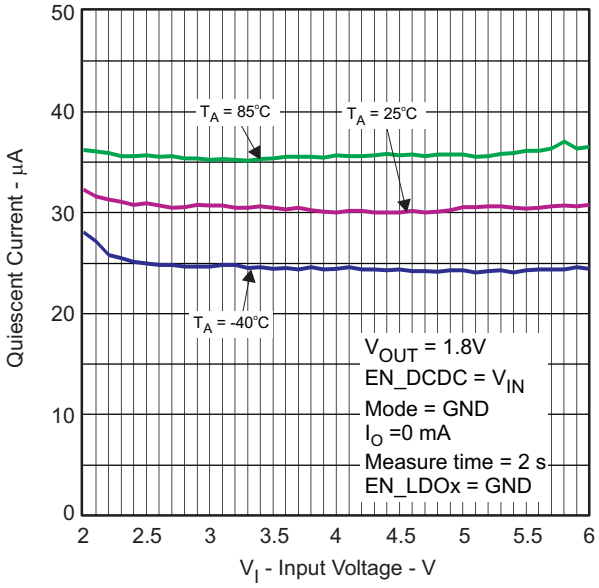


Figure 7.

TPS65001
QUIESCENT CURRENT (LDOx)
vs
INPUT VOLTAGE

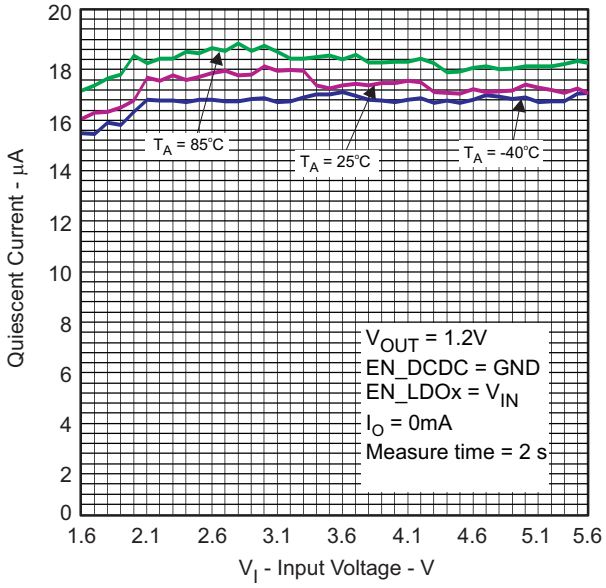


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TPS65001 SHUTDOWN CURRENT vs INPUT VOLTAGE

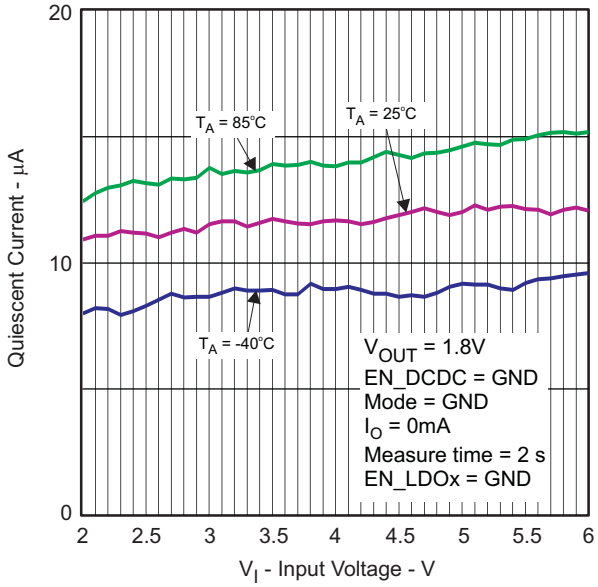


Figure 9.

LINE TRANSIENT RESPONSE (DCDC PFM Mode)

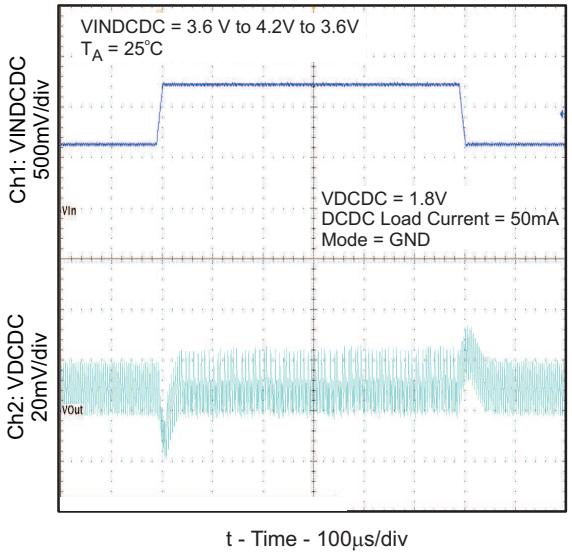


Figure 10.

LINE TRANSIENT RESPONSE (DCDC PWM Mode)

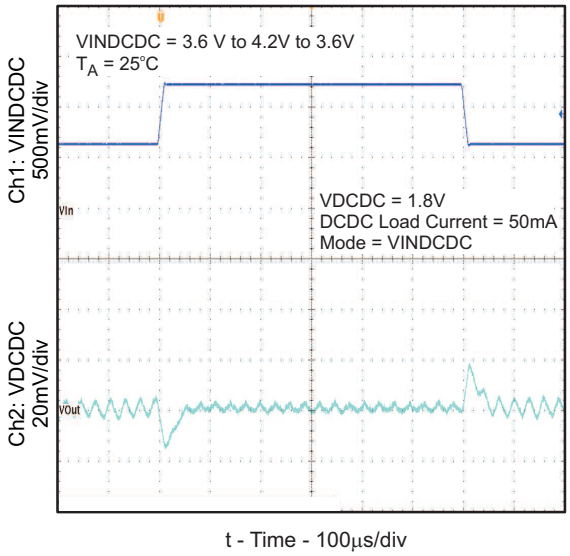


Figure 11.

LINE TRANSIENT RESPONSE (LDOx)

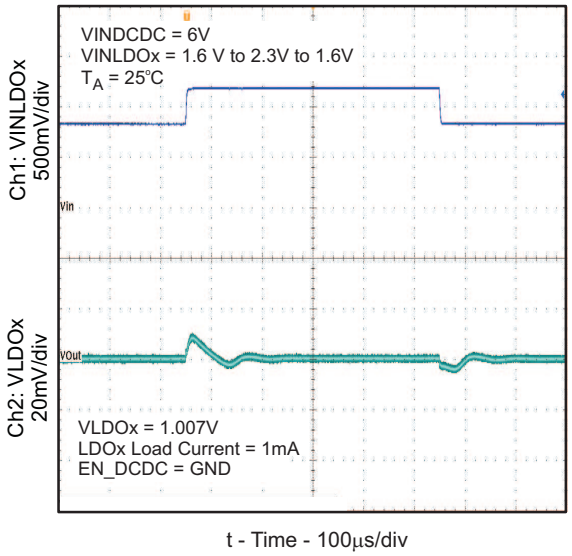


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE (DCDC PFM Mode)

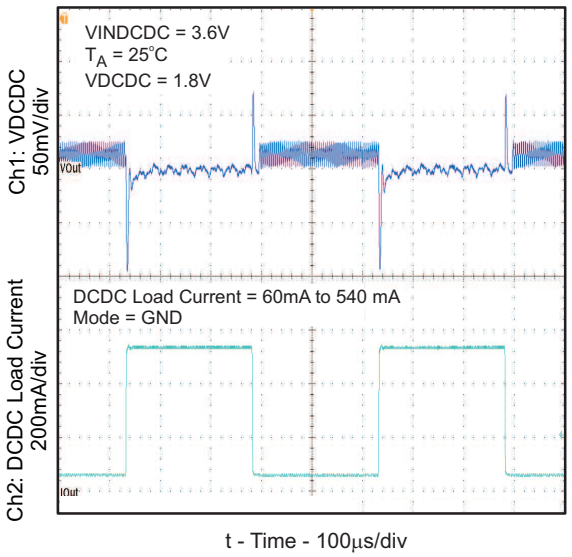


Figure 13.

LOAD TRANSIENT RESPONSE (DCDC PWM Mode)

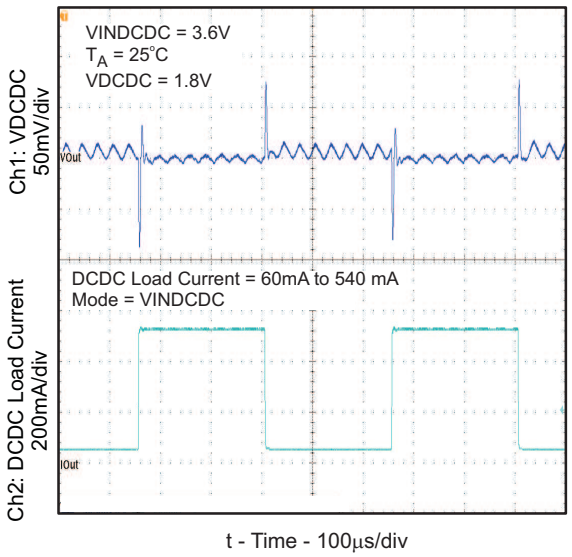


Figure 14.

LOAD TRANSIENT RESPONSE (LDOx)

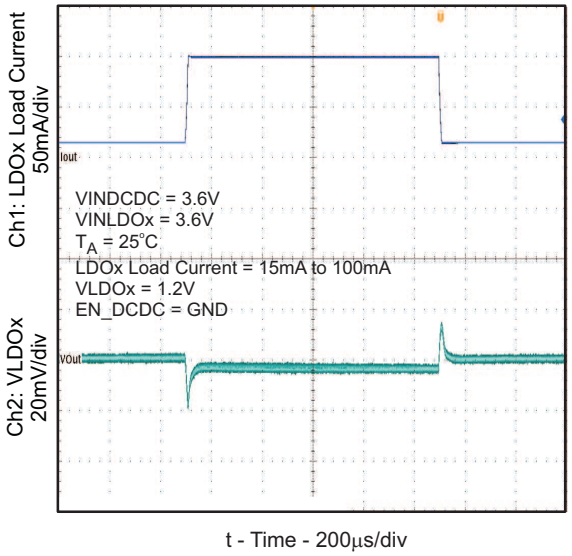


Figure 15.

PFM to PWM TRANSITION (DCDC)

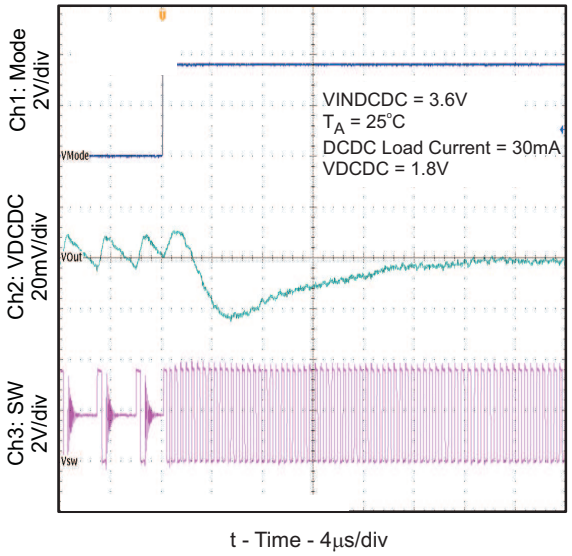


Figure 16.

TYPICAL CHARACTERISTICS (continued)

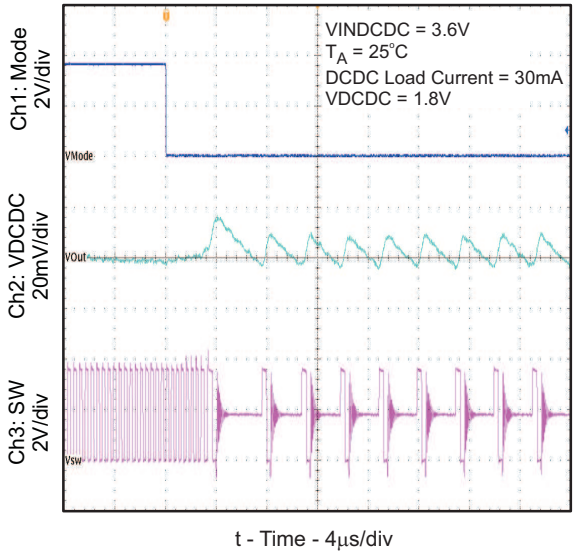


Figure 17.

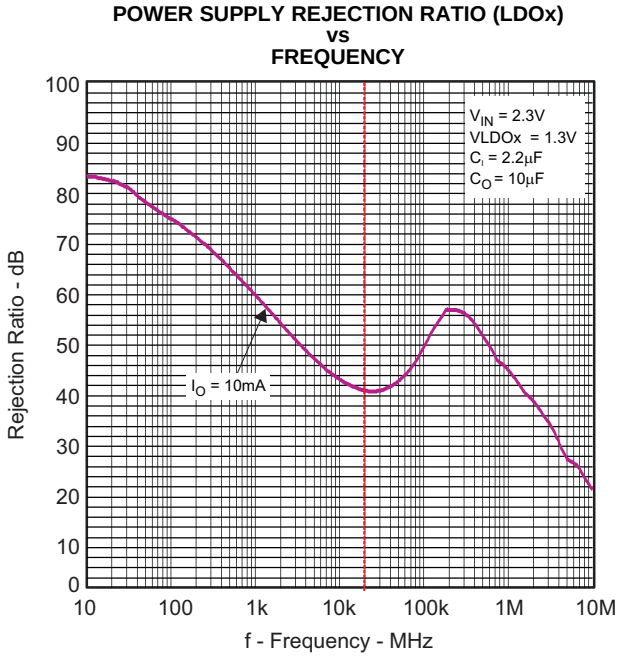


Figure 18.

DETAILED DESCRIPTION

Step-Down Converter

The step down converter is intended to allow maximum flexibility in the end equipment. The output voltage is user selectable with a resistor network on the output. Figure 19 illustrates the necessary connections.

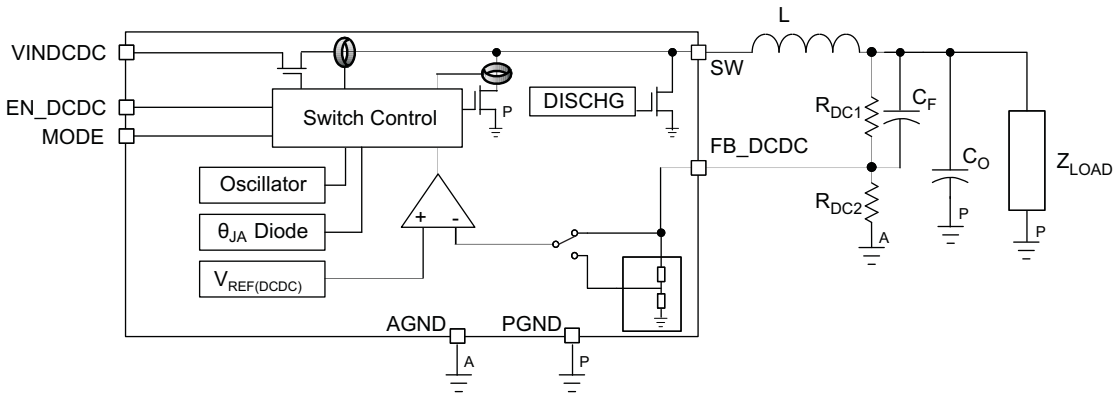


Figure 19. DCDC Block Diagram and Output Voltage Setting

The output voltage of the DCDC converter is set by Equation 1:

$$V_{DCDC} = V_{FB\_DCDC} \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}}$$

$$V_{DCDC} = 0.6V \times \frac{(R_{DC1} + R_{DC2})}{R_{DC2}} \quad (1)$$

The combined resistance of R_{DC1} and R_{DC2} should be less than 1 MΩ.

Fixed output voltages and additional current limit options are also possible. Please contact Texas Instruments for further information.

The step-down converter has two modes of operation to maximize efficiency at different load conditions. At moderate to heavy load currents, the device operates in a fixed frequency pulse width modulation (PWM) mode that results in small output ripple and high efficiency. Pulling the MODE pin to a DC high level will result in PWM mode over the entire load range.

At light load currents, the device operates in a pulsed frequency modulation (PFM) mode to improve efficiency. The transition to this mode occurs when the inductor current through the low-side FET becomes zero, indicating discontinuous conduction. PFM mode also results in the output voltage increasing by 1% from its nominally set value. This voltage positioning is intended to minimize the voltage undershoot of a load step from light to heavy loads, as when a processor moves from sleep to active modes, and the voltage overshoot at load throw-off. Figure 20 shows the voltage positioning behavior for a light to heavy load step.

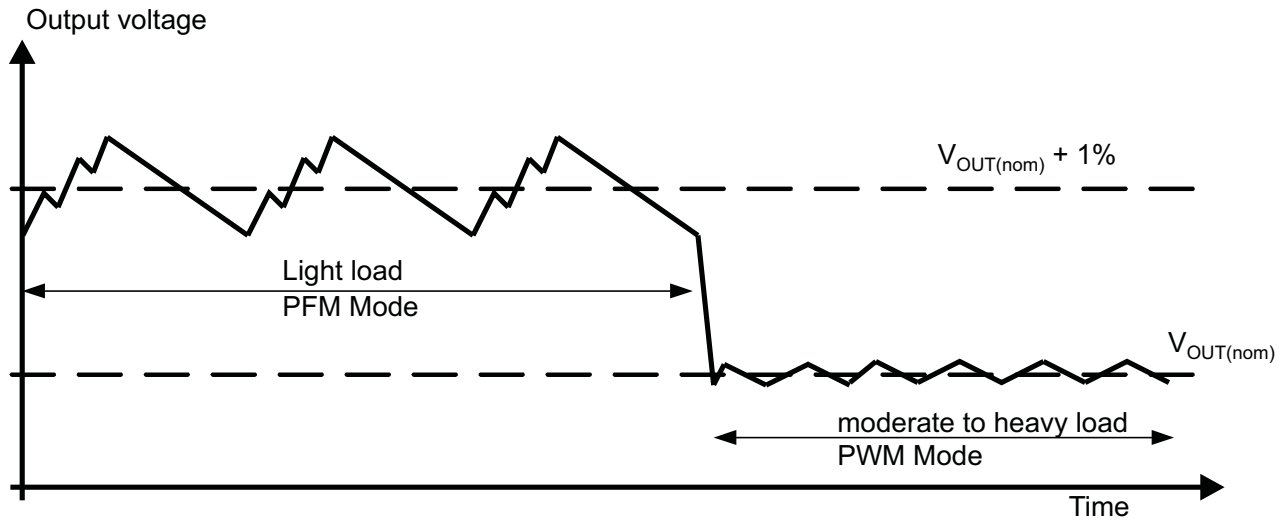


Figure 20. PFM Voltage Positioning

Pulling the MODE pin to DC ground will result in automatic transition between PFM and PWM modes to maximize efficiency.

The DCDC converter output automatically discharges to ground through an internal 450Ω load when EN_DCDC goes low or when the UVLO condition is met.

SOFT START

The step-down converter has an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 21.

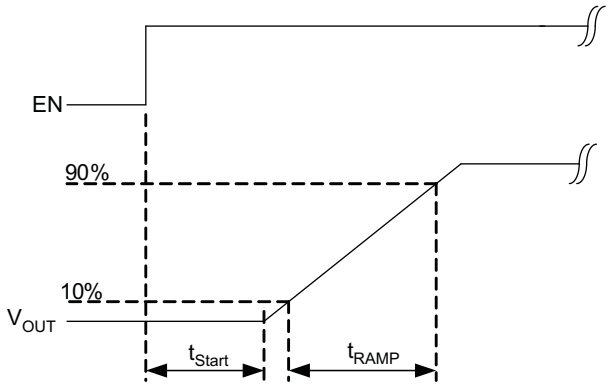


Figure 21. Soft Start

LINEAR REGULATORS

The two linear dropout regulators (LDOs) in the TPS65000 and TPS65001 are designed to provide flexibility in system design. Each LDO has a separate voltage input and enable signal. The input can be tied to the output of the step-down converter or the output of another voltage source. Each LDO output discharge to ground automatically when EN_LDOx goes low.

A resistor network is needed to set the output voltage of the LDOs. Fixed voltage output versions are also available; contact Texas Instruments sales representative for more information.

The LDOs are general-purpose devices that can handle inputs from 6V down to 1.6V, making them suitable for direct connection to the battery. Figure 22 illustrates the necessary connections for LDO1. The same architecture applies to LDO2.

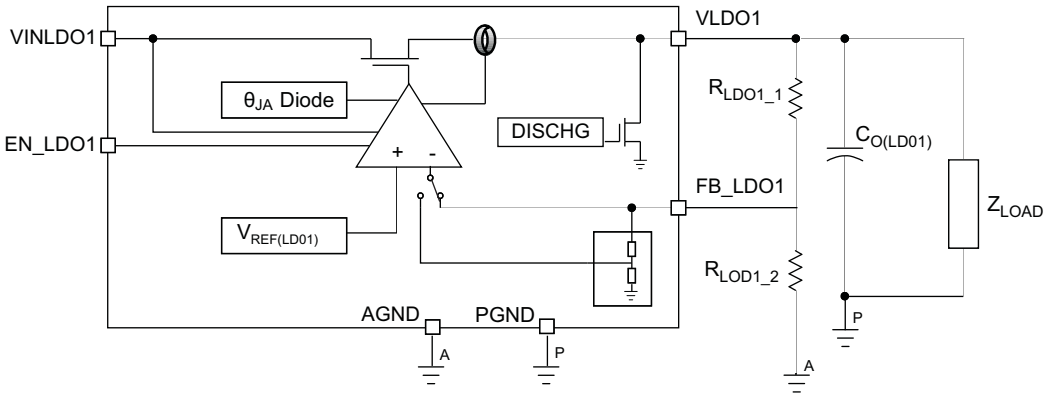


Figure 22. LDO Block Diagram and Output Voltage Setting

The output voltages of the LDOs are set by Equation 2:

$$V_{LDO1} = V_{FB\_LDO1} \times \frac{\left(R_{LDO1\_1} + R_{LDO1\_2}\right)}{R_{LDO1\_2}}$$

$$V_{LDO1} = 0.5V \times \frac{\left(R_{LDO1\_1} + R_{LDO1\_2}\right)}{R_{LDO1\_2}} \quad (2)$$

The combined resistance of R_{LDO1_1} and R_{LDO1_2} should be less than 1MΩ.

Oscillator and Spread Spectrum Clock Generation

The TPS6500x contains an internal oscillator running at a typical frequency of 2.25MHz. This frequency is the fundamental switching frequency of the step-down converter when it is running in PWM mode. An additional circuit in the oscillator block implements spread spectrum clocking, which modulates the main switching frequency when the device is in PWM mode. This spread spectrum oscillation reduces the power that may cause EMI. When viewed in the frequency domain, the SSC spreads out the frequency that may introduce interference while simultaneously reducing the power. Since the frequency is continually shifting, the amount of time the switcher spends at any single frequency is reduced. This reduction in time means that the receiver that may see the interference has less time to integrate the interference.

Different spin versions of SSC settings are also feasible; contact a Texas Instruments sales representative for more information.

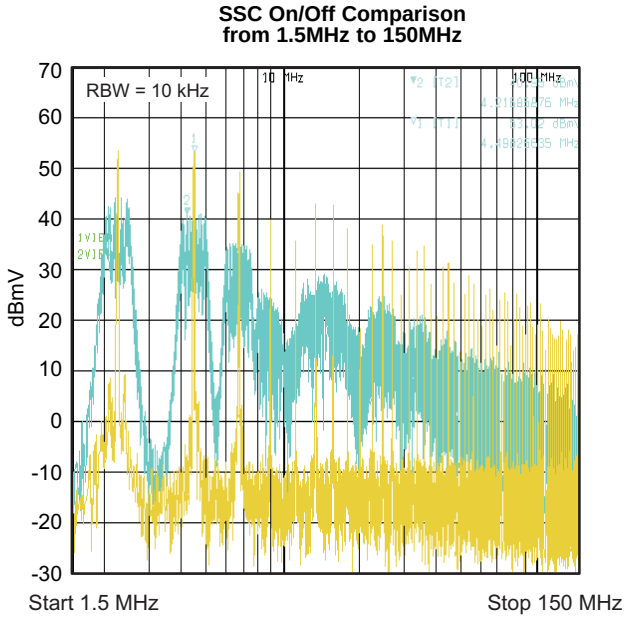


Figure 23.

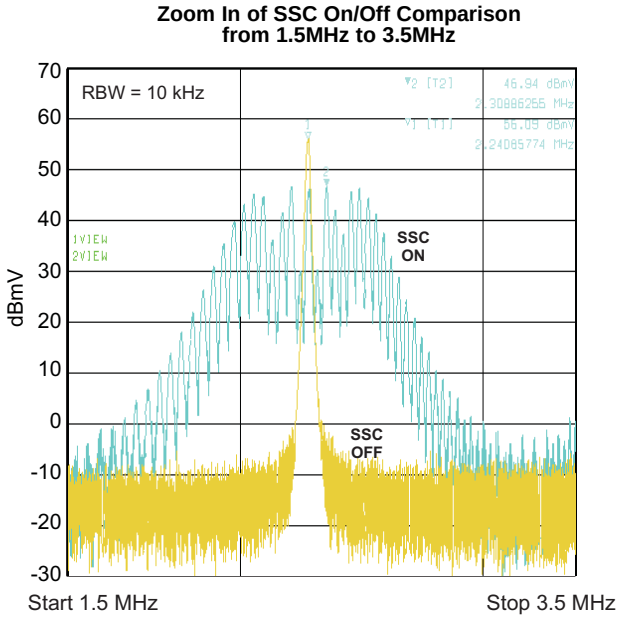


Figure 24.

Figure 23 to Figure 24 shows the advantage of SSC with the frequency spectrum centering on the nominal frequency 2.25MHz. The blue spectrum is the result of the spread change. As depicted in the figures the harmonic spectrum is attenuated 10dB comparing to the same device without SSC.

POWER GOOD

The open drain $\overline{PG}$ output is used to indicate the condition of the step down converter and each LDO. This is a combined output, with the outputs being compared when the appropriate enable signal is high. The pin will be pulled low when all enabled outputs are greater than 90% of the target voltage and High-Z when an enabled output is less than 90% of its intended value or when all the enable signals are pulled low.

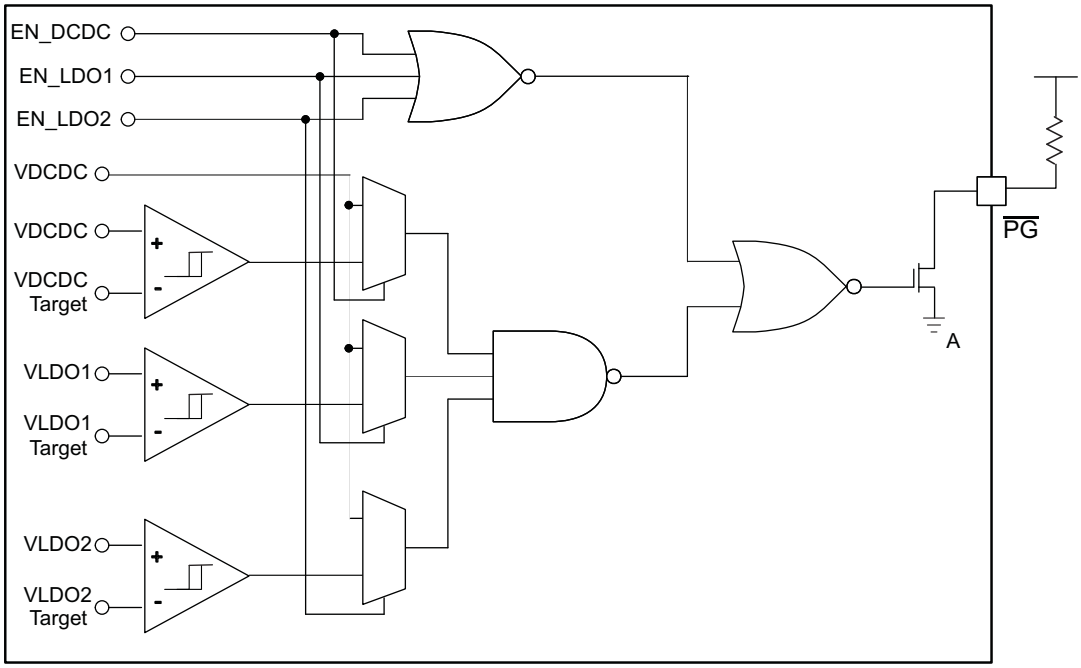


Figure 25. Power Good Functionality

Supply Voltage Supervisor (SVS) [TPS65001 Only]

The SVS is made up of 4 inputs and one output. The $\overline{RST}$ pin is an active low high impedance output. The $\overline{MR}$ pin is an active low input, suitable for connecting to a push button circuit to allow manual reset generation. The RSTSNS pin is an analog input pin used for voltage comparison. The TRST pin is connected to an external capacitor, allowing the reset timing to be set in the application. The VINDCDC pin is the main supply input for the control circuits and the switch mode converter.

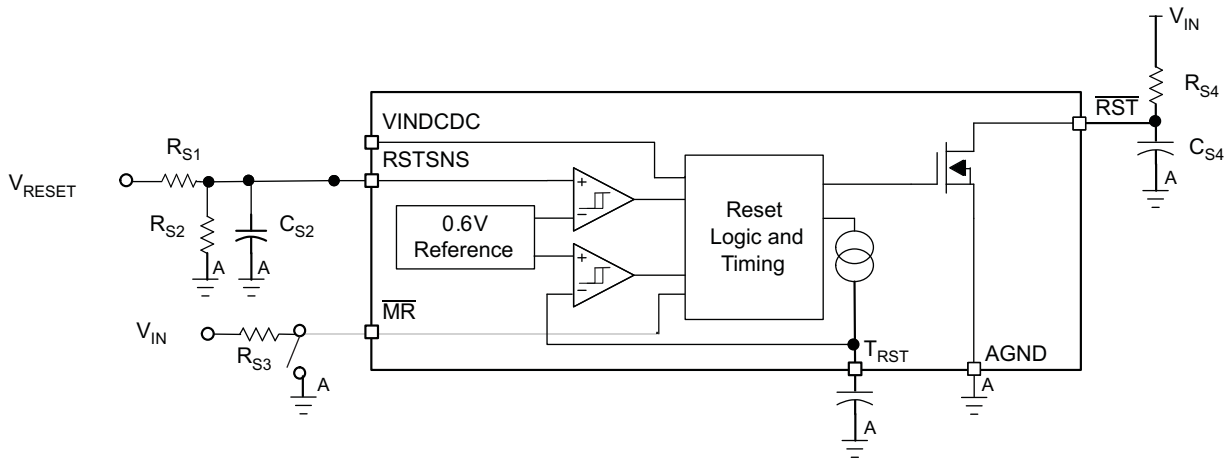


Figure 26. SVS Block Diagram

Each input can individually trigger $\overline{RST}$ to go active. Table 1 outlines the paths to activate the reset.

Table 1. $\overline{RST}$ Generation Table

INPUTS			OUTPUTS
VINDCDC	**$\overline{MR}$**	**V_{RSTSNS}**	**$\overline{RST}$**
0.4 < V < UVLO	X	X	Low
> UVLO	≥ $V_{IH(\overline{MR})}$	≤ 0.6 V	Low
> UVLO	≥ $V_{IH(\overline{MR})}$	> 0.6 V	High-Z
> UVLO	< $V_{IL(\overline{MR})}$	X	Low

The RSTSNS pin should be tied to VINDCDC if the reset functionality is not needed from this pin. This will cause the reset to activate only when VINDCDC is rising from 0V or when VINDCDC has dropped below UVLO. The RSTSNS pin should be connected to an external RC network to set the deglitch timing for triggering a reset when VINDCDC is below the UVLO threshold. The reset threshold voltage is given by Equation 3:

$$V_{RST} = 0.6V \times \frac{(R_{S2} + R_{S1})}{R_{S2}} \quad (3)$$

The $\overline{RST}$ recovery timing is set by the capacitor on the TRST pin. A 2µA current is enabled when the reset condition is met, charging the capacitor. The TRST voltage is monitored internally and the reset ends when the voltage reaches 0.6V. The capacitor value to reset time can be computed with Equation 4:

$$t_{RST} = 0.6V \times \frac{C}{2 \times 10^{-6} A} \quad (4)$$

The value t_{RST} is the time from the end of condition that activated $\overline{RST}$ until $\overline{RST}$ returns to its Hi-Z state. The TRST pin would be internally discharged to ground when the reset condition is true or after t_{RST}.

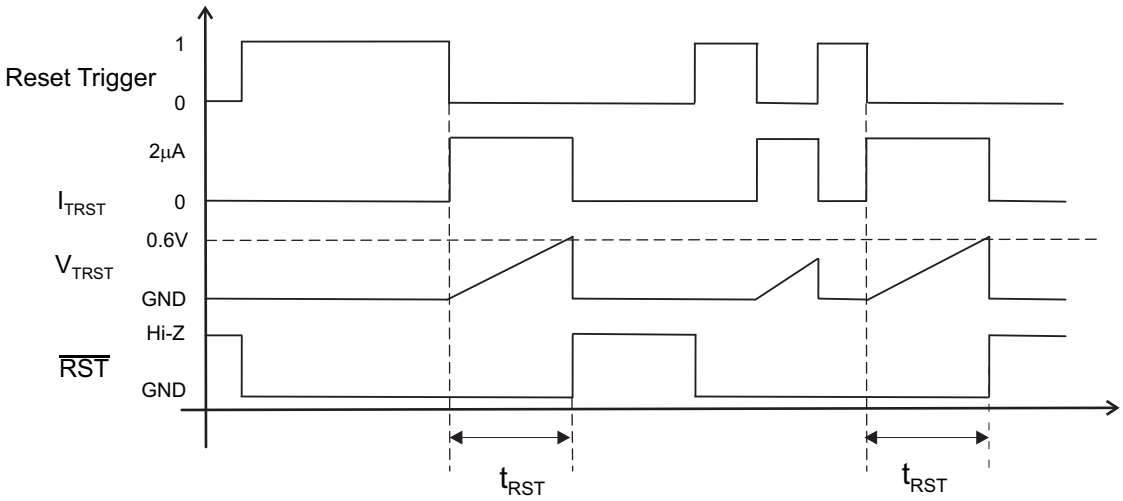


Figure 27. $\overline{RST}$ Recovery Timing

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor Selection

The typical value for the converter inductor is 2.2µH output inductor. Larger or smaller inductor values in the range of 1.5µH to 3.3µH can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance will influence directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. See SLVA157 for more information on inductor selection.

Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 6. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (5)$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \quad (6)$$

With:

f = Switching Frequency (2.25MHz typical)

L = Inductor Value

ΔI_L = Peak to Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum V_{IN}.

Open core inductors have a soft saturation characteristic, and can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Notice that the step down converter has internal loop compensation. As the internal loop compensation is designed to work with a certain output filter corner frequency calculated as follows:

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}} \text{ with } L = 2.2\mu H,\ C_{OUT} = 10\mu F \quad (7)$$

This leads to the fact the selection of external L-C filter has to be coped with the above formula. The product of L × C_{OUT} should be constant while selecting smaller inductor or increasing output capacitor value.

See Table 2 , and the typical applications for possible inductors.

Table 2. INDUCTORS

INDUCTOR TYPE	Inductance µH	SUPPLIER	Max Dimensions (mm)
MIPS2520D2R2	2.0	FDK	2.5 × 2.0 × 1.0
MIPSA2520D2R2	2.0	FDK	2.5 × 2.0 × 1.2
KSLI-252010AG2R2	2.2	Htachi Metals	2.5 × 2.0 × 1.0
LQM2HPN2R2MJ0L	2.2	Murata	2.5 × 2.0 × 1.2
LPS15222	2.2	Coilcraft	3.0 × 3.0 × 1.5

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the converter allows the use of small ceramic capacitors with a typical value of 22µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple, and therefore, are recommended. See the recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (9)$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

The adjustable output voltage of the DCDC converter is calculated by Equation 1 in the Step-Down Converter. To keep the external resistor divider network robust against noise, an external feed forward capacitor is required for optimum load transient response. The value of feed forward capacitor should be in the range between 22pF and 33pF provided the equivalent resistance of RDC1 || RDC2 in Equation 1 is approximately 300kΩ. Scale change on RDC1||RDC2 would apply a scale change to the feed forward capacitor to keep the RC product a constant.

Input Capacitor Selection

Due to the nature of the DCDC converter, having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. It is critical to put the input capacitor as close to the VINDCDC pin as close as possible with the clean GND connection provided. The same consideration is applied for the output capacitor and the inductor. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 3. Capacitors

CAPACITANCE	SUPPLIER	TYPE
22µF	TDK C2012X5R0J226MT	Ceramic
22µF	Taiyo Yuden JMK212BJ226MG	Ceramic
10µF	Taiyo Yuden JMK212BJ106M	Ceramic
10µF	TDK C2012X5R0J106M	Ceramic
10µF	Murata GRM188R60J106M69D	Ceramic

APPLICATION CIRCUITS

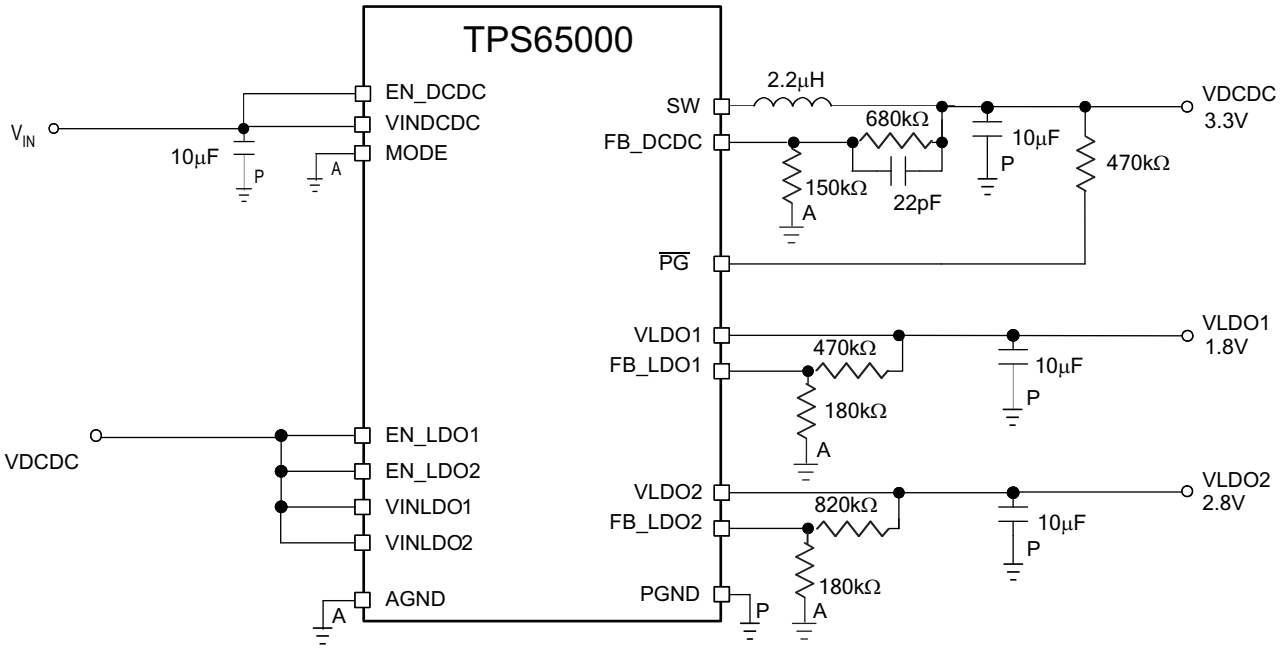


Figure 28. Typical TPS65000 Application Schematic

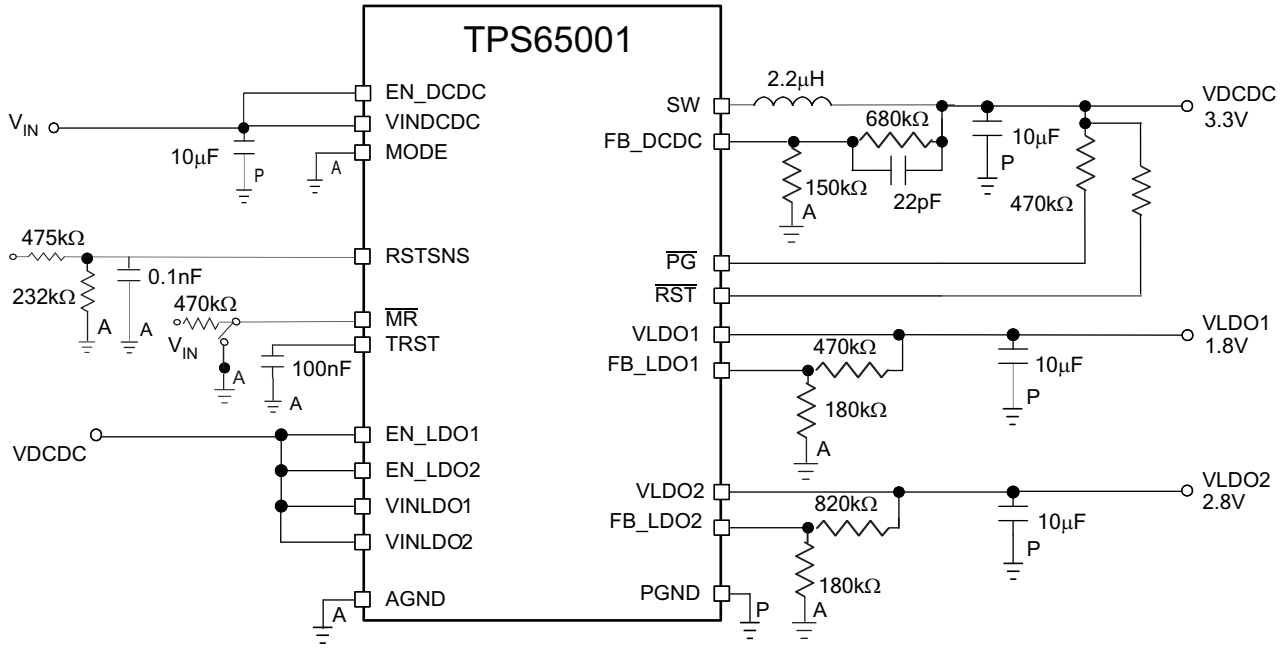


Figure 29. Typical TPS65001 Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65000RTER	ACTIVE	QFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65000RTET	ACTIVE	QFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65001RUKR	ACTIVE	QFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65001RUKT	ACTIVE	QFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

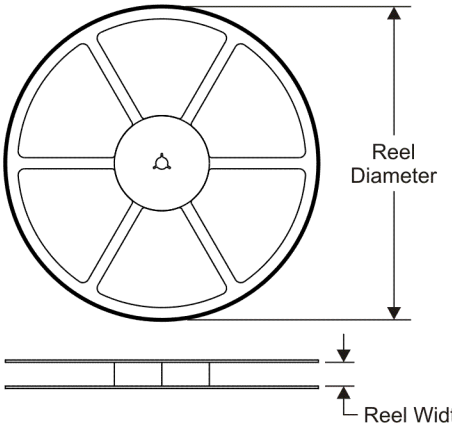
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

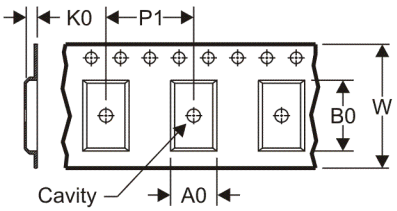
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

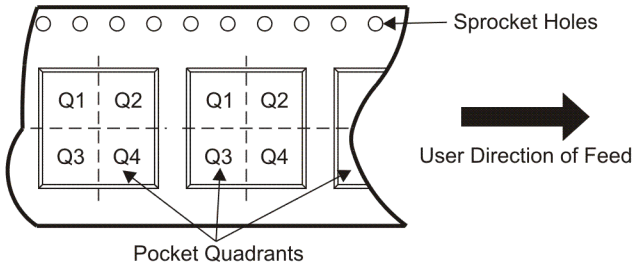


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

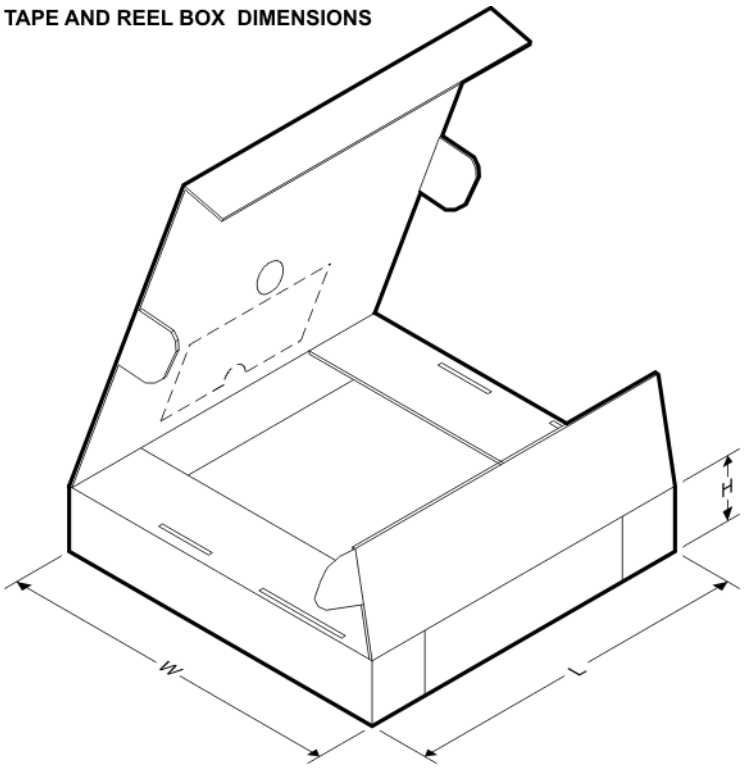
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65000RTER	QFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q2
TPS65000RTET	QFN	RTE	16	250	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q2
TPS65001RUKR	QFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q1
TPS65001RUKT	QFN	RUK	20	250	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q1

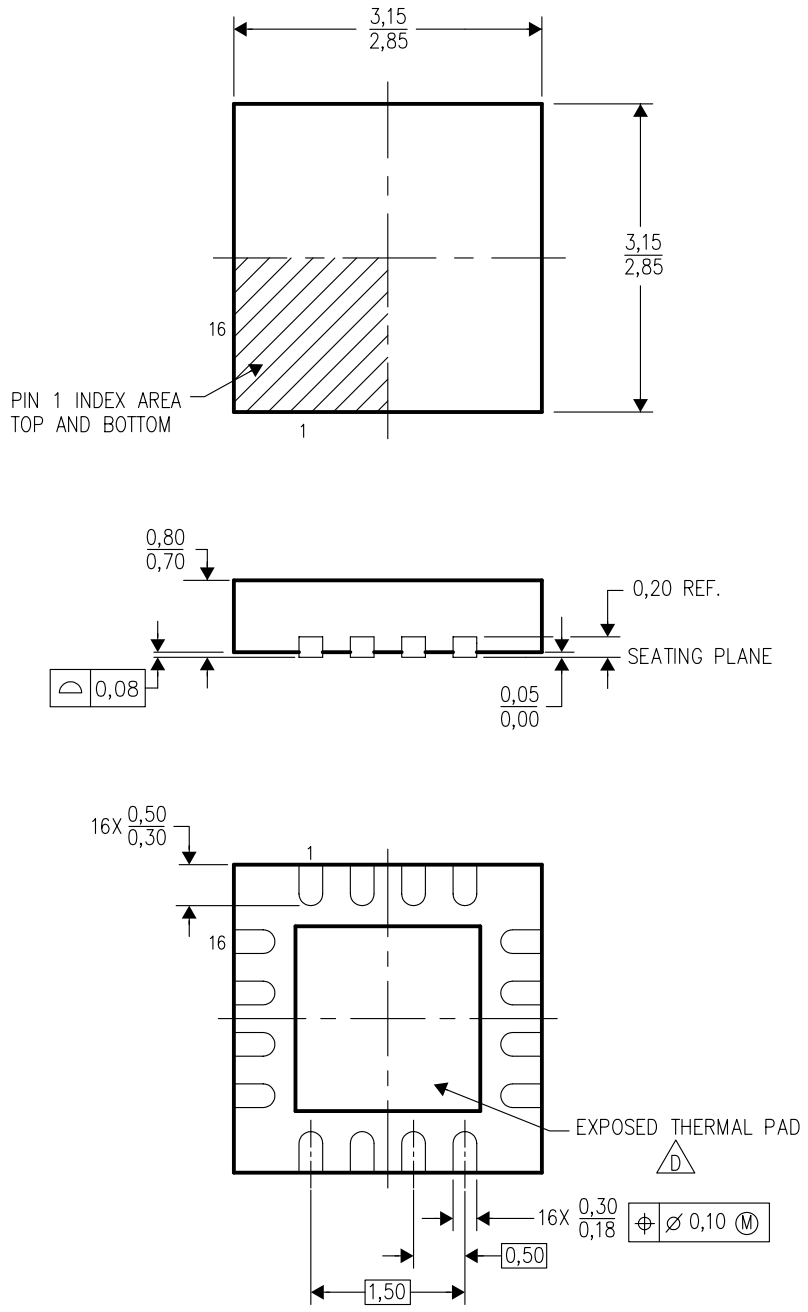
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65000RTER	QFN	RTE	16	3000	340.5	338.1	20.6
TPS65000RTET	QFN	RTE	16	250	340.5	338.1	20.6
TPS65001RUKR	QFN	RUK	20	3000	340.5	338.1	20.6
TPS65001RUKT	QFN	RUK	20	250	340.5	338.1	20.6

RTE (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

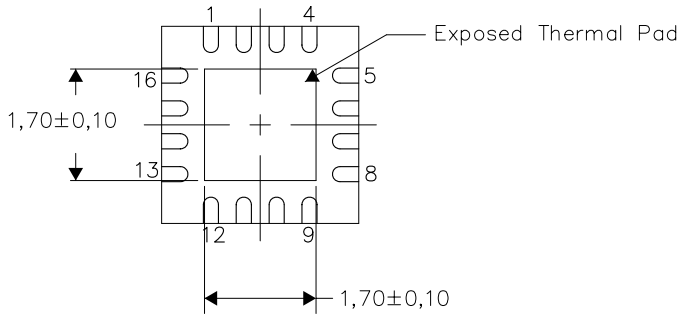
RTE (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

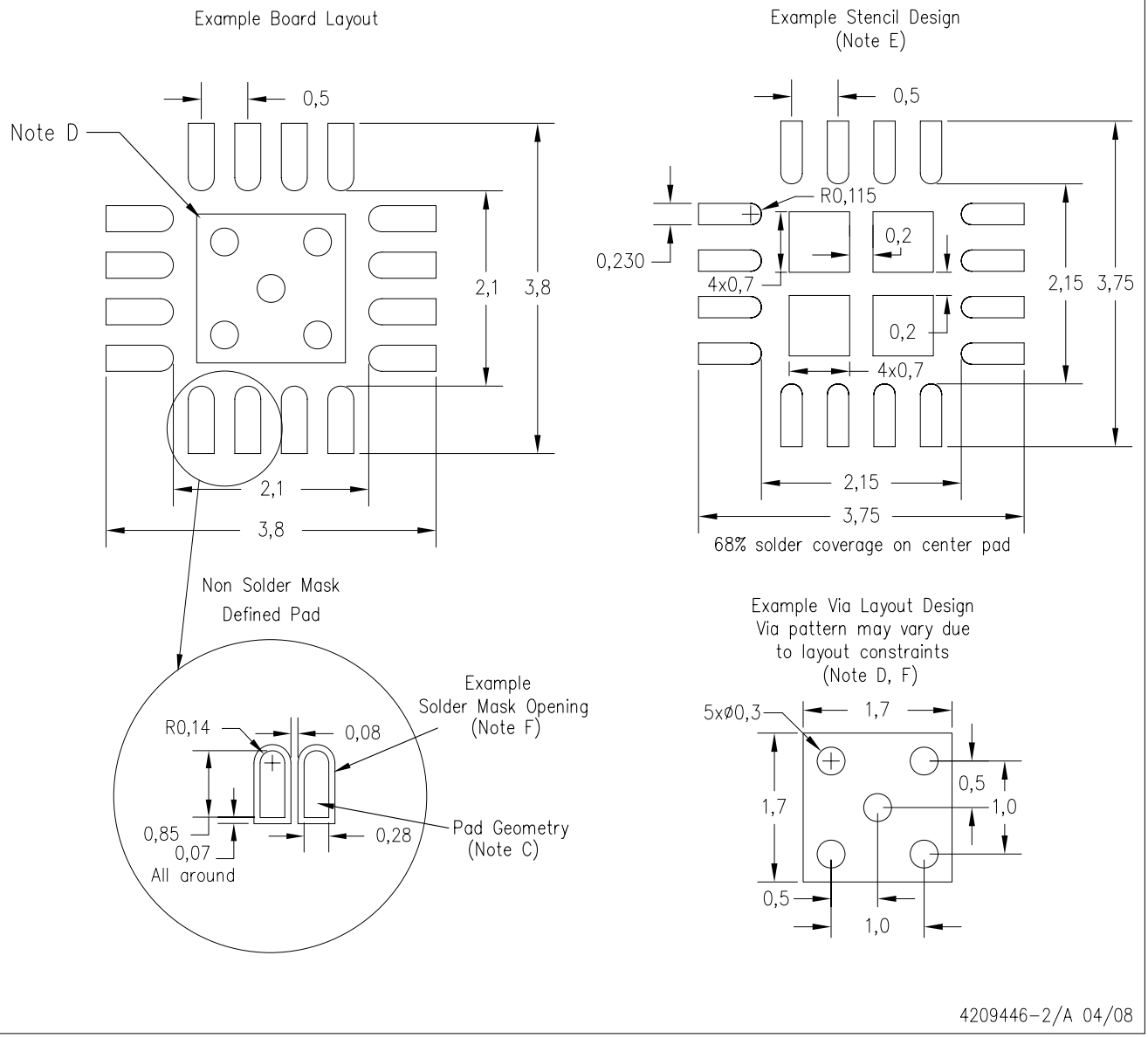


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

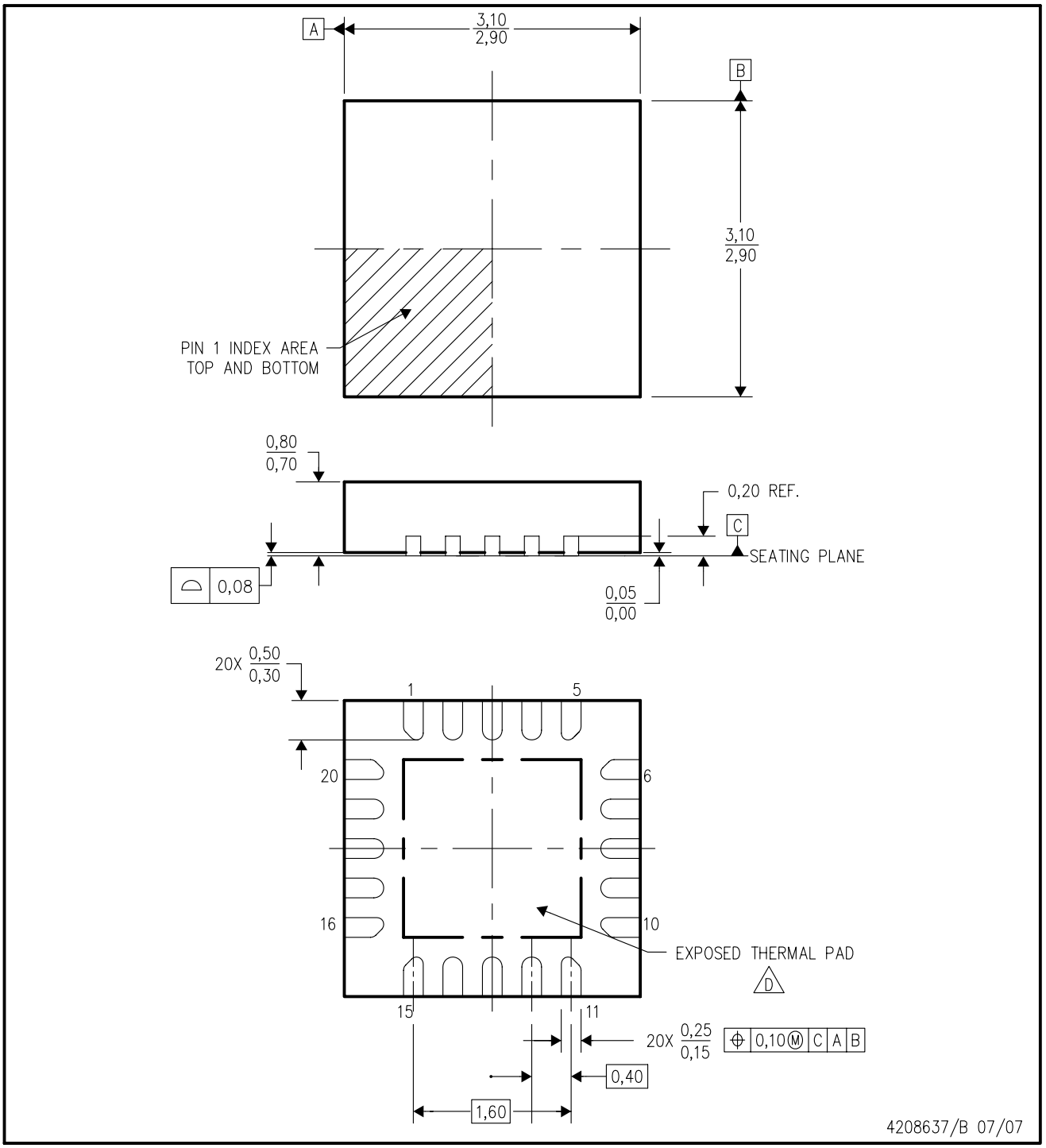
RTE (S–PWQFN–N16)



4209446–2/A 04/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RUK (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

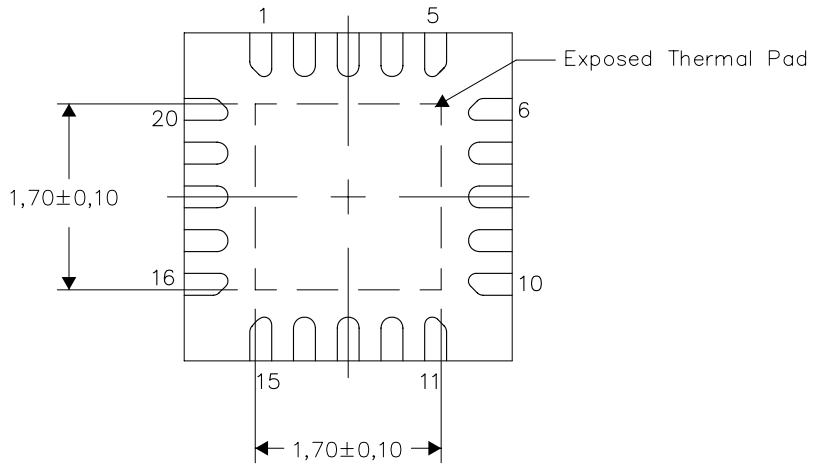
RUK (S–PWQFN–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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