# A²SI-Lite 14 / A²SI-Lite 16

Data Sheet

Low End Device AS-Interface IC

## 1 Features

- Fully operable in AS-interface networking systems and capable of working in extended networks with up to 62 slaves (V2.11)

- Dedicated IO-port structure: two data inputs, two data outputs, no parameter port pins

- Integrated EEPROM stores relevant AS-i information and IC configuration data (e.g. enabling/disabling of the PWM feature)

- Programmable PWM of output signals can be used to control intensity of driven LEDs

## 2 Description

This integrated circuit shall be used as simplified interface IC for key control panels, simple sensors and small actuators based on the AS-i specifications. The device shall be in compliance with AS-i Specification V2.11. The IC performs multiple interface functions.

There are two package options; the 14 pin SOP option A²SI-Lite 14 (A²SI-L14) and the 16 pin SOP option A²SI-Lite 16 (A²SI-L16). In contrast to the A²SI-L14 IC the A²SI-L16 IC has two more pins; a diagnostic LED output pin (LED pin) and a fault indicator input pin (FID pin).
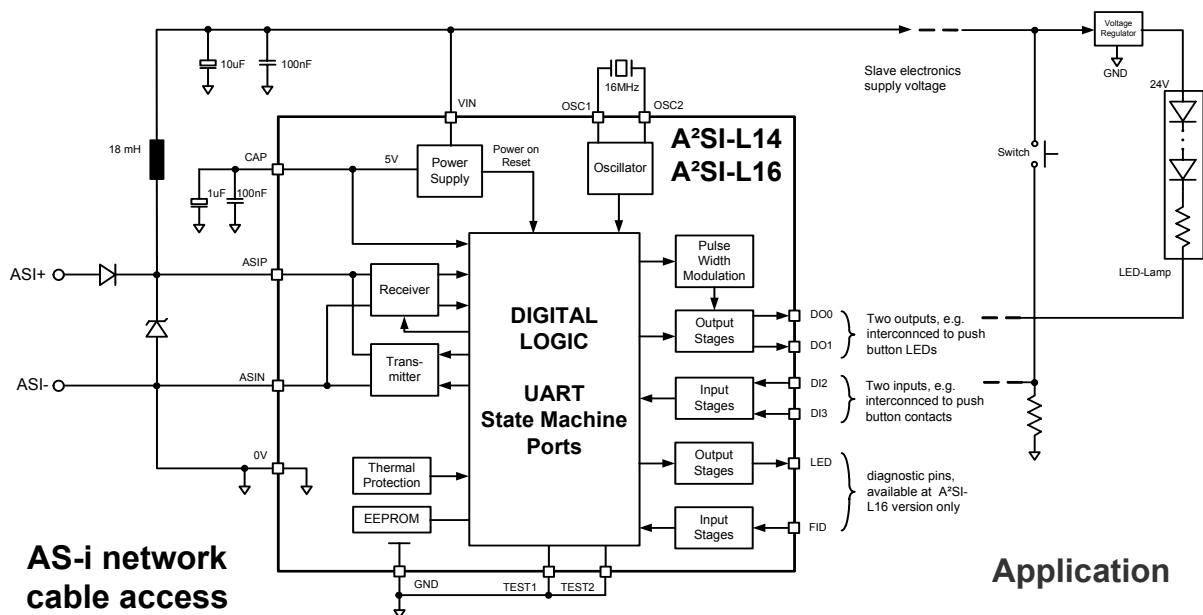
## 3 Block Diagram



*Figure 3-1: Block Diagram*

## 4 Application Support

Configuration of the chip is handled through programming of the on-chip E²PROM. ZMD provides a special

*AS-Interface Programmer Tool*
*(Ordering Code: 3000003356 )*

to ease product evaluation and selection of different operation modes.

Further application support is available through e-mail hotline under asi@zmd.de

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# A²SI-Lite 14 / A²SI-Lite 16
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## 5    Pin Description

Table 5-1 shows the pin description for both the A²SI-L14 and the A²SI-L16 IC. The graphical representation (pin-out symbols) are shown in chapter 6.

*Table 5-1: A²SI-L14/ A²SI-L16 Pin Description*

| Pin# SOIC16 | Pin# SOIC14 | Name | Description |
|---|---|---|---|
| 1 | 1 | ASIPOS | positive ASI supply, high voltage supply |
| 2 | 2 | ASINEG | negative ASI supply |
| 3 | 3 | TEST1 | test mode input/output |
| 4 | 4 | TEST2 | test mode input |
| 5 | | FID | digital input |
| 6 | 5 | DI2 | digital input |
| 7 | 6 | DI3 | digital input |
| 8 | 7 | OSC1 | crystal oscillator input |
| 9 | 8 | OSC2 | crystal oscillator output |
| 10 | 9 | DO1 | digital output |
| 11 | 10 | DO0 | digital output |
| 12 | | LED | digital output |
| 13 | 11 | GND | digital ground |
| 14 | 12 | CAP | regulator output |
| 15 | 13 | 0V | analog ground |
| 16 | 14 | VIN | High voltage supply |

## 6    Pin Configuration

There is only one die used for both the 14- and 16-pin-version of the A²SI-L. In the 14-pin-version, the internal ports FID and LED are not bonded to external pins.
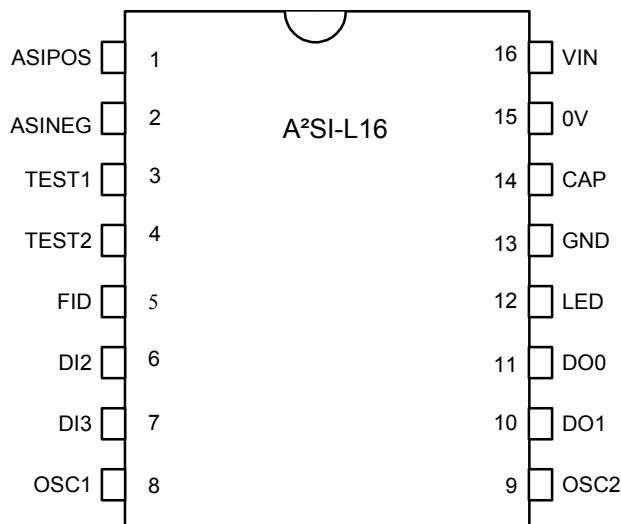


*Figure 6-1: SOP16 Pin out*

# A²SI-Lite 14 / A²SI-Lite 16
Data Sheet
Low End Device AS-Interface IC
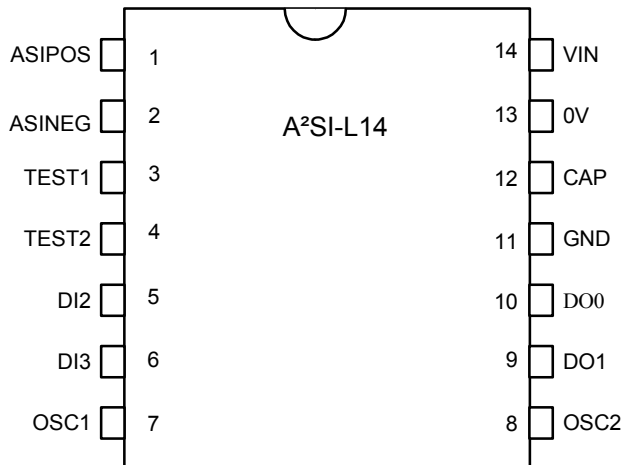


*Figure 6-2: SOP14 Pin out*

## 7    Electrical Specification

### 7.1    Absolute Maximum Ratings (Non Operating)

*Table 7-1: Absolute Maximum Ratings*

| Symbol | Parameter | min | max. | Unit | Note |
|---|---|---|---|---|---|
| V0V ,VGND | Voltage reference | 0 | 0 | V | |
| VASIP | Positive AS-i supply voltage | -0.3 | 40 | V | |
| VASIN | Negative AS-i supply voltage | -0.3 | 20 | V | 1 |
| VASIP-ASIN | Voltage difference from ASIP to ASIN ($V_{ASIP}$ - $V_{ASIN}$) | -0.3 | 40 | V | 2 |
| VASIPP | AS-i supply pulse voltage, voltage difference between pins ASIP and ASIN (from ASIP to ASIN) | | 50 | V | 3 |
| VVIN | Power supply input voltage | -0.3 | 40 | V | |
| Vinputs1 | Voltage at pins DI2, DI3, DO0, DO1, LED, FID | -0.3 | VVIN + 0.3 | V | |
| Vinputs2 | Voltage at pins OSC1, OSC2, CAP, TEST1, TEST2 | -0.3 | 7 | V | |
| Iin | Input current into any pin except supply pins | -25 | 25 | mA | |
| H | Humidity non-condensing | | | | 4 |
| VHBM1 | Electrostatic discharge – human body model (HBM1) | 3000 | | V | 5 |
| VHBM2 | Electrostatic discharge – human body model (HBM2) | 2000 | | V | 6 |
| VEDM | Electrostatic discharge – equipment discharge model (EDM) | 400 | | V | 7 |
| $T_{STG}$ | Storage temperature | -55 | 125 | °C | |
| Ptot | Total power dissipation | | 500 | mW | 8 |

[1] ASIN-pin shall be shorted to the 0V and GND pin on the PCB
[2] reverse polarity protection has to be performed externally
[3] pulse with =< 50us, repetition rate =< 0.5 Hz
[4] defined in DIN 40040 cond. F
[5] HBM1: C = 100pF charged to $V_{HBM1}$ with resistor R = 1.5kOhm in series, valid for ASIP-ASIN only.
[6] HBM2: C = 100pF charged to $V_{HBM2}$ with resistor R = 1.5kOhm in series, valid for all pins except ASIP-ASIN
[7] EDM: C = 200pF charged to $V_{EDM}$ with no resistor in series, valid for ASIP-ASIN only

[8] at max. operating temperature, the allowed total power dissipation depends on the additional thermal resistance from case to ambient and on the operation ambient temperature.

## 7.2 Recommended Operating Conditions

*Table 7-2: Recommended Operating Conditions*

| Symbol | Parameter | min | max. | Unit | Note |
|---|---|---|---|---|---|
| $V_{VIN,1}$ | Positive supply voltage | 12 | 31.6 | V | 1 |
| $V_{VIN,2}$ | Positive supply voltage | 20 | 31.6 | V | 2 |
| $V_{ASIN}$ | Negative AS-i supply voltage | 0 | 0 | V | 3 |
| $V_{0V}$, $V_{GND}$ | Negative supply voltage | 0 | 0 | V | |
| $I_{VIN}$ | Supply current at $V_{VIN}$ = 30V | | 8.5 | mA | 4 |
| $I_{CL1}$ | max. output sink current at pins DO0, DO1 | | 15 | mA | |
| $T_{amb}$ | Ambient temperature range, operating range | -25 | 85 | °C | |

1 all operations without EEPROM-write access are allowed
2 necessary for operations with EEPROM-write access only (processing of ADRA and WID1 master calls,
  refer to Table 8-1)
3 ASIN shall be shorted with 0V and GND in order to ensure proper functionality of transmitter circuit.
4 fc = 16.000 MHz, no load at any pin, without reaction of the circuit, ASIN is short-circuit to 0V, VIN = 30V.

Table 7-3 describes the crystal parameter that shall be satisfied by the x-tal that is interconnected to the pins OSC1 and OSC2. Due to the fact that the crystal parameter do not represent the entire internal and external oscillator circuit at all practical tests must indicate whether a crystal may work in a certain application circuit (PCB) or not. Appendix A list certain types of crystals that are going to be used as reference devices.

*Table 7-3: Crystal Properties[1]*

| Symbol | Parameter | Nom. | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $F_c$ | Crystal frequency | 16000 | Fc – 60 ppm | Fc + 60 ppm | kHz | |
| Cs | Series capacitor | | 5 | 13 | fF | |
| Rs | Series resistor | | | 65 | Ohm | |
| Cp | Parasitic parallel capacitor | | | 5 | pF | |
| Cload | Crystal dedicated parallel load | 15[2] | | | pF | |

[1] Crystal properties according to the crystal manufacturer data sheet
[2] In order to keep the influence of the crystal to the network error rate low as possible it is recommended to keep the crystal dedicated load between 8 pF and 32 pF. The IC provides approximately a load capacity of about 10 pF to 15 pF (correct by design).

## 7.3 Quality Assurance

The quality of the IC will be ensured accordingly to the ZMD quality standards.

## 7.4 DC and AC Characteristic of all Pins and Functions

All parameters are valid for the recommended range of $V_{ASIP}$ - $V_{ASIN}$ and $T_{AMB}$. The devices are tested within the recommended range of $V_{ASIP}$ - $V_{ASIN}$, $T_{AMB}$ = +25°C (+ 85°C and - 25°C on sample base only) unless otherwise stated. Unused input pins shall be connected to a suitable potential within the application circuit because there are no internal pull-up/down resistors. It is recommended to connect these pins either to 0V or via resistor to VIN.
In order to ensure a normal operation of the IC the pins TEST1 and TEST must be connected to ground potential (GND).

## 7.4.1 Digital input and output Pins

Controlled by a configuration flag that is stored inside the EEPROM the data output signals can be pulse width modulated (PWM, for information refer to chapter 8.6.2).
The functionality of the FID output port is described in chapter 8.7.

*Table 7-4: Input Voltages and Currents: Pins DI2, DI3, FID, TEST1/2 [1]*

| Symbol | Parameter | Min | Max. | Unit | Note |
|---|---|---|---|---|---|
| $V_{IL}$ | Voltage range for input "low" level | 0 | 2.5 | V | |
| $V_{IH}$ | Voltage range for input "high" level | 3.5 | $V_{VIN}$ | V | 3 |
| $V_{HYST}$ | Hysteresis for switching level | 0.25 | | V | 2 |
| $I_{IL}$ | Current range for input "low" level | -20 | -5 | µA | |
| $I_{IH}$ | Current range for input "high" level | -10 | 10 | µA | $V_O$ = 5V |
| $I_{IHV}$ | Current range for high voltage input | | 2 | mA | $V_O$ = 30V |

[1] TEST1/2 are inputs for test purposes only.
[2] switching level approx. 3V, i.e. 3V +/- $V_{HYST}$ ; the maximum hysteresis is determined by (min.) $V_{IH}$ – (max) $V_{IL}$
[3] Valid for high voltage input pins DI2, DI3 and FID. The regular logic swing is 0 .. 5V although higher input voltages might be applied (refer to parameter $V_{inputs1}$ in Table 7-1). In the case of input voltages that exceed 5V a significant higher input current will flow into the input that is caused by the input protection circuitry (refer to parameter $I_{IHV}$ of Table 7-4 and Figure 7-1).
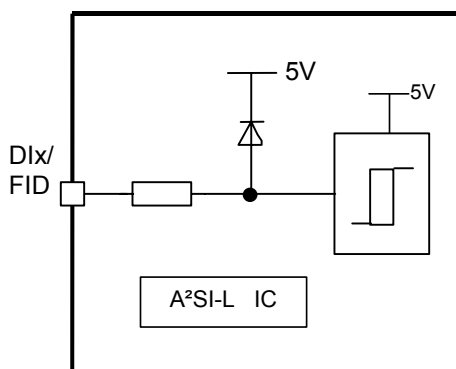
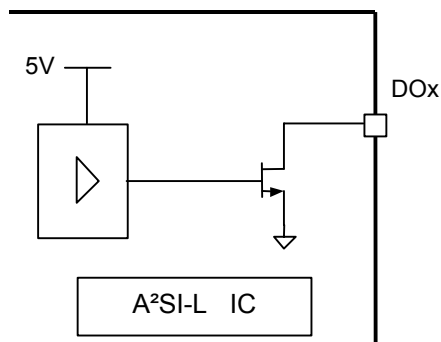*Figure 7-1: Data Input Schematic in Principle*

*Figure 7-2: Data Output Schematic in Principle*

*Table 7-5: Output Voltages and Currents: Pins DO0, DO1, LED*

| Symbol | Parameter | Min | Max. | Unit | Note |
|---|---|---|---|---|---|
| $V_{OL}$ | Voltage range for output "low" level | | 1 | V | $I_{OL1}$ = 15mA |
| $I_{OH}$ | Output leakage current | -10 | 5 | µA | $V_{OH}$ = 30V |

## 7.4.2 AS-i Bus Load (Pins ASIP/ASIN and Power Supply Input VIN)

The following parameters are determined with short-cut between the pins ASIN, GND, and 0V (GROUND). The pin VIN is connected to ASIP via an external coil. A decoupling capacitor has to be interconnected between VIN and GROUND as shown in Figure 8-1.

*Table 7-6: AS-i Bus Interface Properties*

| Symbol | Parameter | min | max. | Unit | Note |
|---|---|---|---|---|---|
| ILIN | Input current limit at $V_{IN}$ | | 25 | mA | |
| VSIG | Input signal voltage difference between ASIP and ASIN | 3 | 8 | $V_{PP}$ | |
| ISIG | Modulated output peak current from ASIP to ASIN | 55 | 68 | $mA_P$ | |
| $C_{zener}$ | Parasitic capacitance of the external over-voltage protection diode (Zener diode) | | 20 | pF | 1 |
| RIN | Equivalent resistor of the ASIC | 50 | | kOhm | 1 |
| CIN | Equivalent capacitor of the ASIC | | 15 | pF | 1 |

[1] The equivalent circuit of a slave has to satisfy the Complete AS-i Specification v.2.11 concerning the requirements for the extended address range. The input impedance as function of frequency is considered as correct by design.

## 7.4.3 Pins OSC1, OSC2

The on chip x-tal oscillator requires a 16 MHz crystal that must be interconnected to the pins OSC1 and OSC2. Internal capacitors make sure that no external capacitors from OSC1/OSC2 to ground are required. Furthermore no external capacitors shall be added to OSC1 and OSC2, respectively. Due to this parasitic capacitors shall be limited to $C_{OSC}$ (Table 7-7). Appendix A shows the parameter of the crystal that is supposed to be used in A²SI-L IC application circuits.

*Table 7-7: Oscillator Pins*

| Symbol | Parameter | Min | max. | Unit | Note |
|---|---|---|---|---|---|
| COSC | External parasitic capacitor at oscillator pins OSC1, OSC2 | 0 | 7 | pF | |
| VIL | Input "low" voltage | 0 | 1.5 | V | 1 |
| VIH | Input "high" voltage | 3.5 | 5 | V | 2 |

[1] for external clock applied to OSC1 only
[2] for external clock applied to OSC1 only

## 7.5 Information Data for Development

*Table 7-8: Information Data*

| Symbol | Parameter | min | max. | Unit | Note |
|---|---|---|---|---|---|
| $V_{PORIF}$ | Falling edge of the internal 5V supply voltage that activates the internal power-on-reset signal | 3 | 4 | V | 1 |
| $V_{PORIR}$ | Rising edge of the internal voltage 5V supply voltage that causes the deactivation of the internal power-on-reset signal what will cause the start of the INIT procedure | 2.5 | 3.5 | V | 1 |
| $T_{shut}$ | Chip temperature that causes an overtemp shut down | 125 | 160 | $^o$C | |
| Symbol | Parameter | min | max. | Unit | Note |

| $V_{LSIGon}$ | Receiver comparator threshold level (refer to Figure 7-3) | 45 | 50 | % | related to amplitude of $1^{st}$ pulse |
|---|---|---|---|---|---|
| $t_{reset1}$ | Reset time - either after the end bit of the sent out slave response that is related to a received master Call Reset AS-i-Slave - or after the IC has deactivated its power-on-reset signal | | 2 | ms | 1 |
| $T_{Low}$ | Power-on reset pulse width | 4 | 6 | us | 1 |

[1] guaranteed by design only



"DC level"

The IC determines the amplitude of the first negative pulse of the ASI telegram. This amplitude is asserted to be VSIG / 2.

first negative pulse of the ASI telegram

$V_{LSIGon} = (0.45 ... 0.5) * V_{SIG} / 2$

$V_{LSIGon}$

$V_{SIG} / 2$
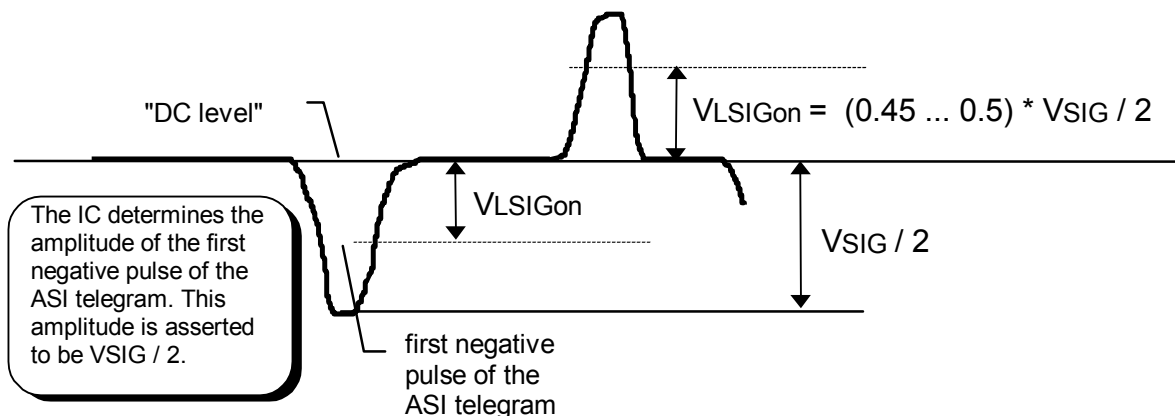
*Figure 7-3: Receiver comparator threshold set-up in principle*



$V_{VIN}$

< ca. 15V

$V_{CAP}$

$V_{POR1F}$

$V_{POR1R}$

0V

POR (low active)

$t_{Low}$

Power-on Reset will be active if the $V_{CAP}$ drops below $V_{POR1F}$
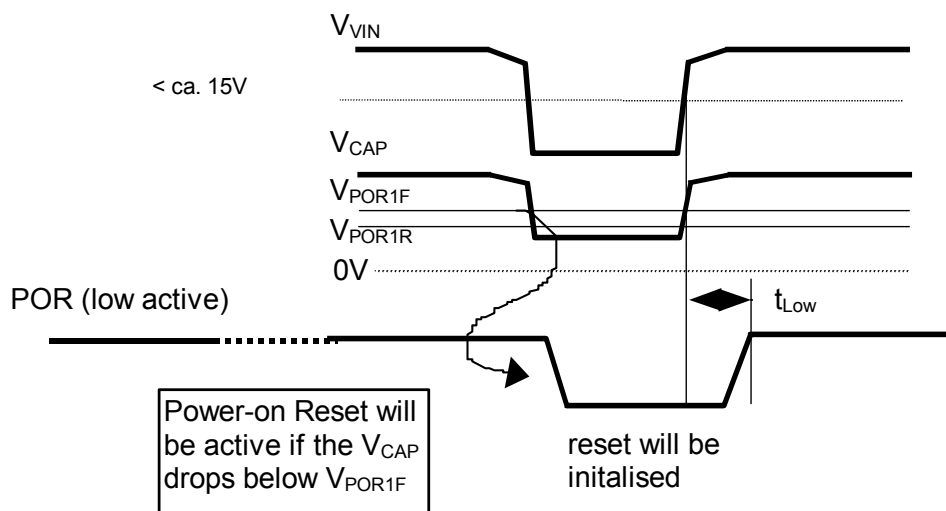
reset will be initalised

*Figure 7-4: Reset Behavior*

Note: The power-on reset circuit has a threshold voltage reference. This reference matches the process tolerance of the logic levels and is not required to be very accurate. All values depend slightly on the raise and fall time of the supply voltage.

# 8 Functional Description

## 8.1 Functional Block Diagram
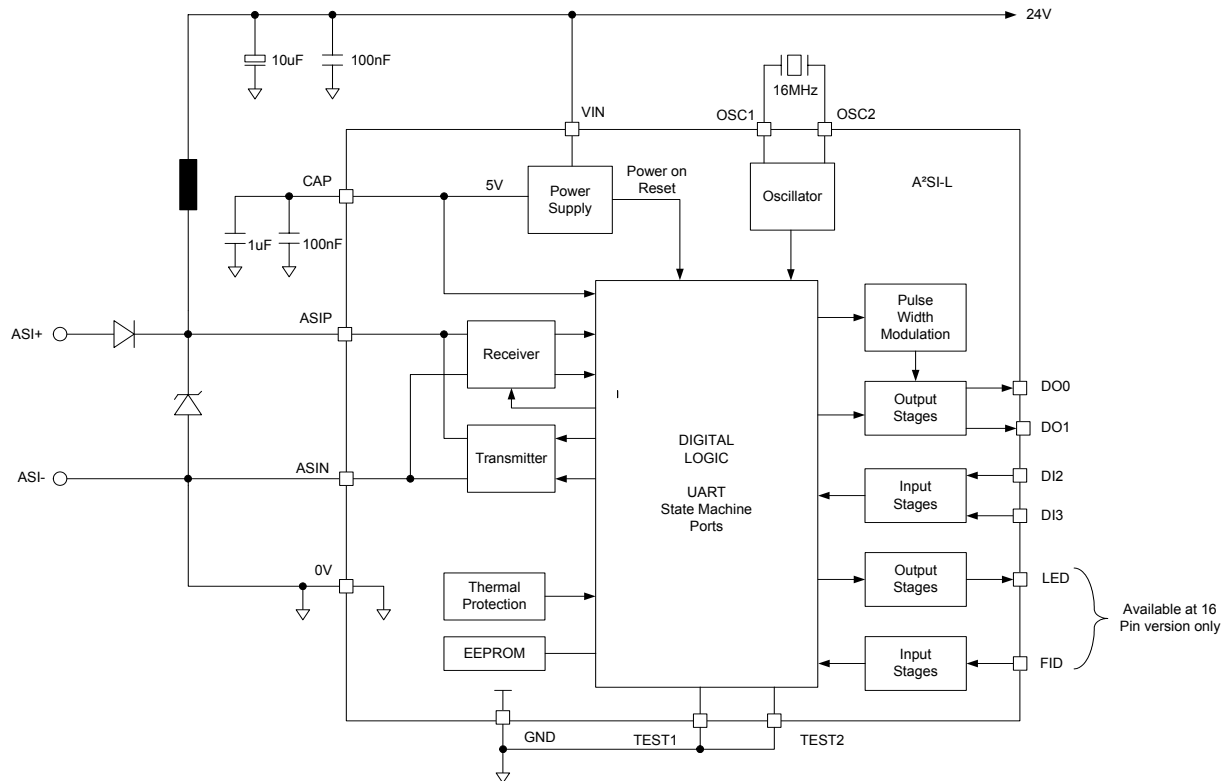


*Figure 8-1: Functional Block Diagram*

## 8.2 Power Supply

The power supply is derived from the AS-i line through an external reverse polarity protection diode and coil, and provided at pin $V_{IN}$. An on-chip voltage regulator regulates the voltage at approximately 5V.

## 8.3 Receiver

The receiver detects the signals on the AS-i line and delivers the appropriate pulses to the digital logic. The DC value of the input signal is removed and the AC signal is band-pass filtered. This circuit is operating on both ASI+ and ASI- lines to take the differential nature of the signals into account. The digital output signals are extracted from the $\sin^2$-shaped input pulses by a set of comparators. The maximum voltage of the first pulse determines the threshold level for all following pulses. This maximum value is digitally filtered to guarantee stable conditions (burst spikes have no effect). This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The receiver delivers the positive and negative pulses to the ASIC's logic. The logic resets the comparators after receiving with the REC_RESET signal. When the receiver is turned on the transmitter is turned off to reduce the power consumption.

## 8.4 Transmitter

The transmitter draws a modulated current between the ASI+ and ASI- pins to generate the communication signals. The shape of the current corresponds to the integral of a $\sin^2$-function. The transmitter uses a current DAC and a high current driver. This driver must be activated before the transmission to achieve operating conditions. A small current is required which will be ramped up slowly to avoid any false voltage pulses on the

AS-i line. The amount of circuitry between the ASI+ and ASI- pins is minimized to allow high impedance values. When the transmitter is turned on the receiver is turned off to reduce the power consumption.

## 8.5 Digital Logic

The digital logic block analyses the received signal, controls the reaction of the slave, transmits the slave response and switches the output ports.

Essential parts of the digital logic are as follows:
- The *UART* performs a syntactical analysis of the incoming master signal and executes the Manchester-coding of the outgoing slave answer.
- The *STATE MACHINE* controls the overall behavior of the slave. Depending on the configuration data provided by the EEPROM and the logic levels at the digital input ports it computes the contents of the slave answer where required. Table 8-1 lists all master calls that will be decoded by the **A²SI-L** IC. Moreover, the logic state of the digital output ports is controlled by the *STATE MACHINE* as well. Chapters 8.6 and 8.7 contain more detailed descriptions of the digital I/O-ports.
- The *EEPROM* stores the non-volatile data of the **A²SI-L** circuit. A specification of the *EEPROM* contents is given in Table C-1 on page 22. The meaning of some configuration flags are explained below and in Chapter 8.6, respectively.

By setting the *Program_Mode_Disable* flag (refer to Table C-1), the manufacturers of AS-i slave components may protect the entire firmware area – addresses 0x8 up to 0xC – against accidental overwriting.

The *Watchdog_Active* flag enables the internal communication watchdog. Once the communication was activated, it will trigger an unconditional reset as soon as it detects a data communication pause longer than 40ms. It should be noted that only the reception of a *Write Parameter (WPAR)* or *Data Exchange (DEXG)* master call can reset the watchdog.

*Table 8-1: A²SI-L Master Calls and Related Slave Responses*

| Instruction | MNE | ST | CB | A4 | A3 | A2 | A1 | A0 | I4 | I3 | I2 | I1 | I0 | PB | EB | SB | I3 | I2 | I1 | I0 | PB | EB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Master Request | | | | | | | | | | | | Slave Response | | | |
| Data Exchange | DEXG | 0 | 0 | A4 | A3 | A2 | A1 | A0 | 0 | D3 ~Sel | D2 | D1 | D0 | PB | 1 | 0 | 0 E3 | 0 E2 | D1 E1 | D0 E0 | PB | 1 |
| Write Parameter | WPAR | 0 | 0 | A4 | A3 | A2 | A1 | A0 | 1 | P3 ~Sel | P2 | P1 | P0 | PB | 1 | 0 | P3 I3 | P2 I2 | P1 I1 | P0 I0 | PB | 1 |
| Address Assignment | ADRA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A4 | A3 | A2 | A1 | A0 | PB | 1 | 0 | 0 | 1 | 1 | 0 | PB | 1 |
| Write Extented ID Code_1 | WID1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ID3 | ID2 | ID1 | ID0 | PB | 1 | 0 | 0 | 0 | 0 | 0 | PB | 1 |
| Delete Address | DELA | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 0 | 0 Sel | 0 | 0 | 0 | PB | 1 | 0 | 0 | 0 | 0 | 0 | PB | 1 |
| Reset Slave | RES | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 1 ~Sel | 1 | 0 | 0 | PB | 1 | 0 | 0 | 1 | 1 | 0 | PB | 1 |
| Read IO Configuration | RDIO | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 0 Sel | 0 | 0 | 0 | PB | 1 | 0 | IO3 | IO2 | IO1 | IO0 | PB | 1 |
| Read ID Code | RDID | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 0 Sel | 0 | 0 | 1 | PB | 1 | 0 | ID3 | ID2 | ID1 | ID0 | PB | 1 |
| Read ID Code_1 | RID1 | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 0 Sel | 0 | 1 | 0 | PB | 1 | 0 | ID3 | ID2 | ID1 | ID0 | PB | 1 |
| Read ID Code_2 | RID2 | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 0 Sel | 0 | 1 | 1 | PB | 1 | 0 | ID3 | ID2 | ID1 | ID0 | PB | 1 |
| Read Status | RDST | 0 | 1 | A4 | A3 | A2 | A1 | A0 | 1 | 1 ~Sel | 1 | 1 | 0 | PB | 1 | 0 | S3 | S2 | S1 | S0 | PB | 1 |
| Broadcast (Reset) | BR01 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | PB | 1 | --- no slave response --- | | | | | | |
| Enter Program Mode | PRGM | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | PB | 1 | --- no slave response --- | | | | | | |

Notes:

- In extended address mode the "Select Bit" defines whether the A- Slave or B- Slave is being addressed.
- The *Enter Program Mode* master call is intended for factory programming of the IC only. In order to achieve EEPROM firmware protection and in order to satisfy the AS-interface Complete Specification the call *Enter Program Mode* must be deactivated by setting the *Program_Mode_Disable* flag before shipment of the slave.

## 8.6    Data I/O Ports

### 8.6.1    Data Exchange Model

All Data_Out and Data_In signals are directly connected to the respective port (refer to Figure 8-2). The **A²SI-L** IC has only two data output pins (DO0 and DO1). Therefore the information bits I3 and I2 of the master call are not transferred to the **A²SI-L** data outputs. Since the **A²SI-L** IC has only two data input pins (DI2 and DI3) both lower order information bit (I1 and I0) of the slave response are set to "0" if the IC answers a *Data Exchange* master telegram.

If the EEPROM flag *Invert_Data_In* (refer to Table C-1) is set, all input data is inverted. This feature will simplify the circuitry for NPN-inputs.
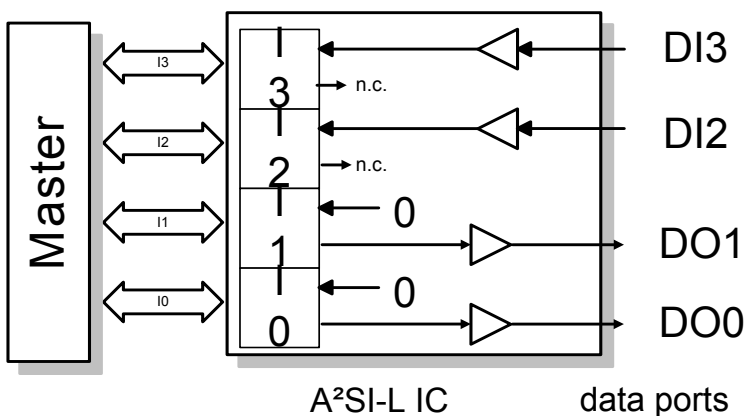
*Figure 8-2: A²SI-L IC Data Exchange master call data model*

The data input pins (DI2 and DI3) are sampled in a time frame that starts not earlier as the point in time of the end bit of the related *Data Exchange* master call and ends at least at the end of the start bit of the corresponding slave response. In the same time frame the data output pins will change their state if appropriated.

### 8.6.2    PWM Function

The regular function of the data pins DO0 and DO1 is to send out the corresponding master telegram data of the call *Data Exchange* (DEXG, refer to Table 7-5). DO0 corresponds to I0 and DO1 corresponds to I1. In addition to that the **A²SI-L** IC performs a PWM function which is dedicated for the brightness control of LEDs that are interconnected to DO0 and/or DO1, respectively. The PWM function may be enabled by the EEPROM flag *PWM_enable* (refer to Table C-1).

*Table 8-2: PWM specification of Outputs: Pins DO0, DO1*

| Intensity of LED | "Write Parameter" command from Master [1] | | | PWM Frequency [2] $1 / t_{PWM}$ | Pulse duty ratio [3] $t_{on} / t_{PWM}$ |
|---|---|---|---|---|---|
| | P2 | P1 | P0 | | |
| 100.00% | Select DO0 or DO1 | 1 | 1 | DC (default) | 16/16 |
| 50.00% | Select DO0 or DO1 | 0 | 1 | 125Hz | 8/16 |
| 25.00% | Select DO0 or DO1 | 1 | 0 | 125Hz | 4/16 |
| 12.50% | Select DO0 or DO1 | 0 | 0 | 125Hz | 2/16 |

[1] The write parameter call is used to control the intensity of LEDs that are interconnect to the data output pins.
[2] Correct by design
[3] Pulse/duty ratio is defined as the quotient ton / tPWM (refer to Table 8-2)

Provided that a lit LED is caused by a logic low level output signal of the related data pin brightness of the LED can be controlled by the master call *Write Parameter* (WPAR, refer to Table 8-1) as shown in Figure 8-3. After a *Write Parameter* call has been received the pulse duty ratio will be effective after the slave response has been sent. The default duty pause ration is 100% which is set after the initialization phase of the IC automatically. Figure 8-3 shows the telegram structure of the *Write Parameter* call. and the related slave response data.
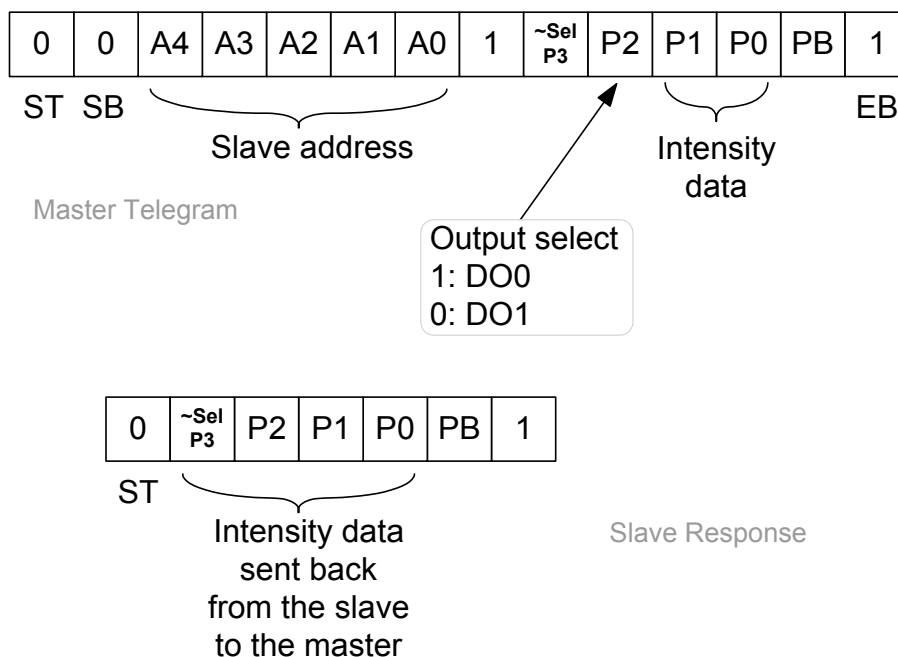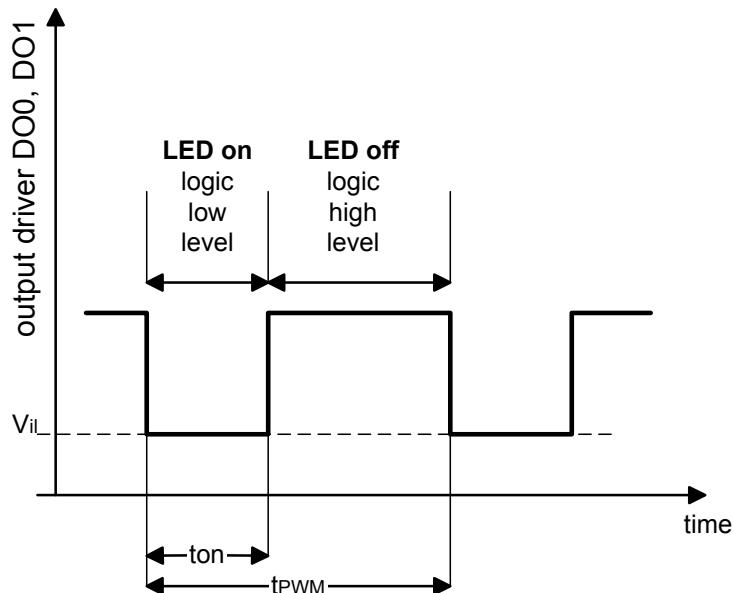


*Figure 8-3: PWM control*

*Figure 8-4: PWM Output Signal Timing*

## 8.7 FID Input and LED Output Ports

The fault indication input FID is a digital input that is dedicated for a periphery fault messaging signal (for electrical properties refer to Table 7-4 on page 7). The S1 status bit is equivalent to the FID input signal. An FID transition will occur at S1 with a certain delay due to a synchronizer circuit which is put in between.
In case of the 14 pin IC version the FID input is not available. The manufacturer (ZMD) will disable this function by setting the EEPROM flag *FID_Disable* (refer to Table C-1). A disabled FID pin function is equivalent to a logic low input signal at an enabled FID pin. Therefore the status bit S1 is always cleared if an IC is having a disabled FID pin.

The LED output port is used as a status indicator.  An active FID (logic high) signal causes a flashing status LED (frequency approx. 2Hz). Otherwise, if FID is not active (logic low) the status LED operation depends on the communication status of the **A²SI-L** device. If the internal  *Data_Exchange_Disable* flag is set (no data exchange allowed), a steady-on LED shall indicate that the communication is off.
Notes:
* An active FID has priority and will cause a flashing LED even if the *Data_Exchange_Disable* flag is set.
* If the FID pin is disabled (EEPROM flag *FID_Disable* set), the LED output is always set to logic high state.

## 9   Typical application circuit of A²SI-L
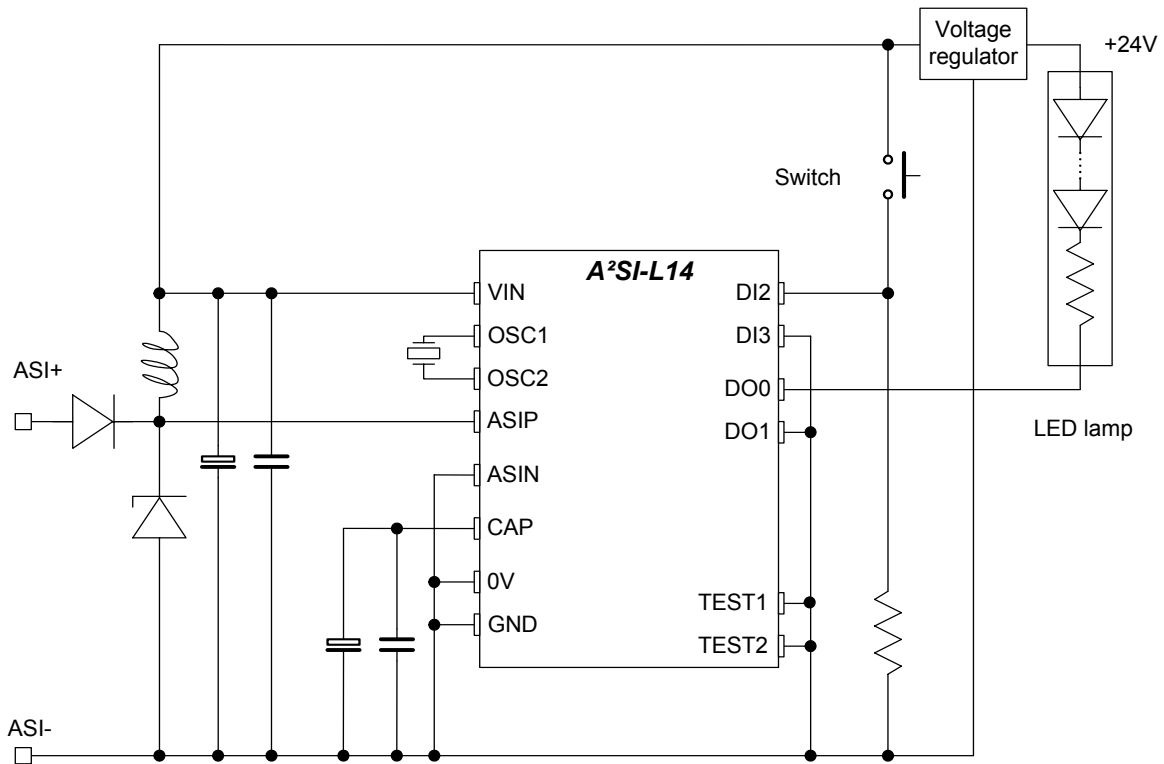


Figure 9-1: Typical Application of A²SI-L14 IC

The pins ASIN, 0V and GND must be connected on the PCB.
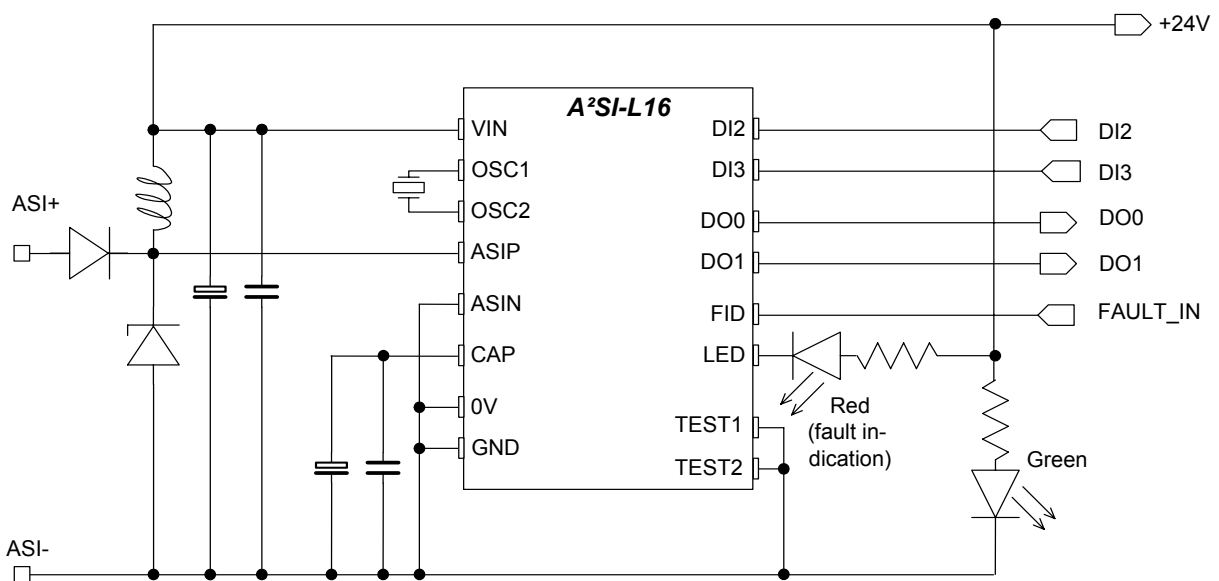


Figure 9-2: Typical Application of A²SI-L16 IC

# A²SI-Lite 14 / A²SI-Lite 16
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## 10  Package Outline and Device Marking

The IC is available in a 14 or 16 pin SOIC-package (Figure 10-1). It has the dimensions as shown in Table 10-1. Figure 10-2 and Figure 10-3 indicate the device marking.



*Figure 10-1: SOIC Package Outline Dimensions*

# A²SI-Lite 14 / A²SI-Lite 16
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*Table 10-1: Package Outline Dimensions*

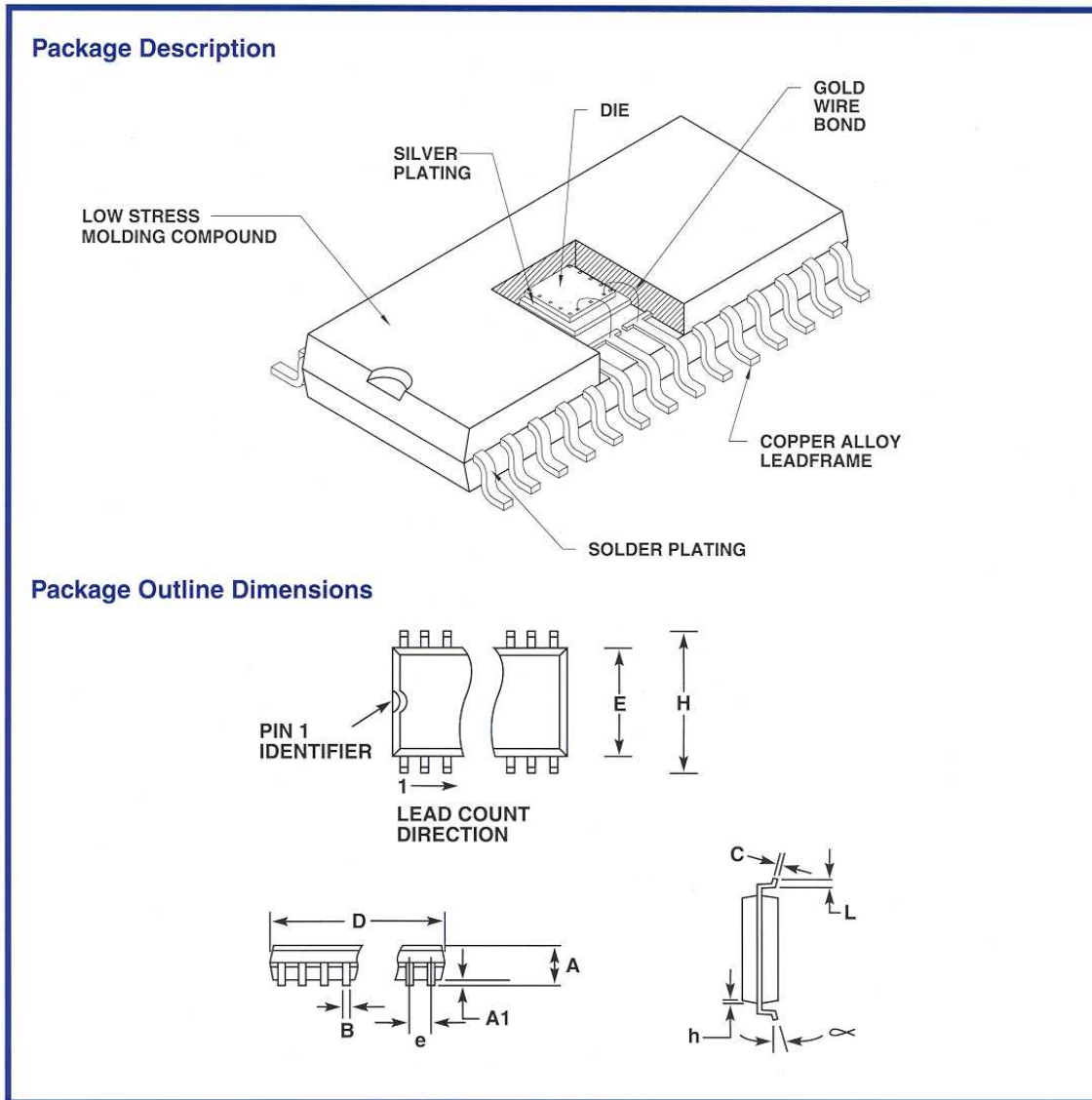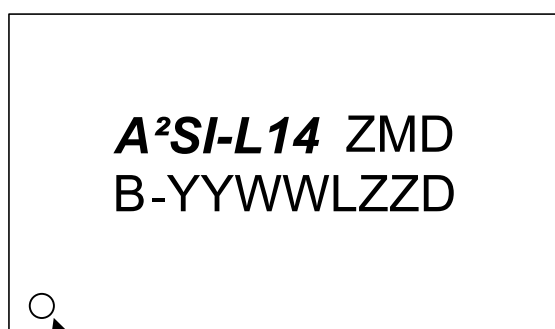|  | A | A1 | B | C | e | D | E | L | H | h | alpha |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SOIC 14 | Inches | | | | | | | | | | |
| Min. | 0.061 | 0.004 | 0.0138 | 0.0075 | 0.050 Typ. | 0.337 | 0.150 | 0.016 | 0.230 | 0.010 | 0° |
| Max. | 0.068 | 0.0098 | 0.0192 | 0.0098 | | 0.344 | 0.157 | 0.035 | 0.244 | 0.016 | 8° |
| SOIC 16 | Inches | | | | | | | | | | |
| Min. | 0.061 | 0.004 | 0.0138 | 0.0075 | 0.050 Typ. | 0.386 | 0.150 | 0.016 | 0.230 | 0.010 | 0° |
| Max. | 0.068 | 0.0098 | 0.0192 | 0.0098 | | 0.393 | 0.157 | 0.035 | 0.244 | 0.016 | 8° |

*A²SI-L14* ZMD
B-YYWWLZZD

○ Pin 1 mark

A²SI-L14: Product Name
ZMD: Manufacturer
B: Revision Code
YYWW: Year / Workweek (Datecode)
L: Assembly Location
ZZD: Traceability and Status Code

*A²SI-L16* ZMD
B-YYWWLZZD
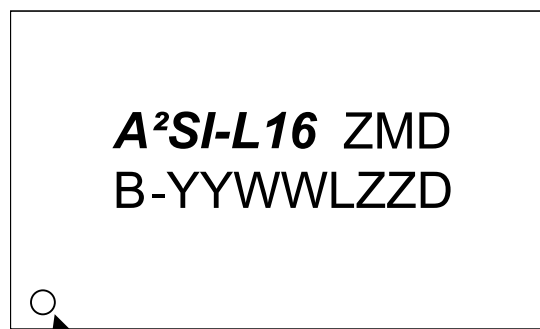
○ Pin 1 mark

A²SI-L16 : Product Name
ZMD: Manufacturer
B: Revision Code
YYWW: Year / Workweek (Datecode)
L: Assembly Location
ZZD: Traceability and Status Code

*Figure 10-2: Mark Diagram of 14 Pin SOIC Version* *Figure 10-3: Mark Diagram of 16 Pin SOIC Version*

## 11 Ordering Information

| Ordering Code | Description | Operating Temperature Range | Package Type | Shipping Form |
|---|---|---|---|---|
| **A2SI-L14-ST** | 14 pin version | -25°C to 85°C | SOP14 (150 mil) | Tubes (55 parts/tube) |
| **A2SI-L14-SR** | 14 pin version | -25°C to 85°C | SOP14 (150 mil) | Tape-and-Reel (2500 parts/reel) |
| **A2SI-L16-ST** | 16 pin version with FID / LED pin | -25°C to 85°C | SOP16 (150 mil) | Tubes (55 parts/tube) |
| **A2SI-L16-SR** | 16 pin version | -25°C to 85°C | SOP16 (150 mil) | Tape-and-Reel |

| | with FID / LED pin | | | (2500 parts/reel) |
|---|---|---|---|---|

## 12  Application Support

### 12.1  AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

**AS-International Association**
*Contact - Rolf Becker*
Zum Taubengarten 52
D-63571 Gelnhausen
PO Box 1103 Zip (63551)
Tel: +49 6051 47 32 12
Fax: +49 6051 4732 82
Email: as-interface@t-online.de
http://www.as-interface.net

Refer to the Association's website hereabove for contact info on different local AS-Interface associations which provide local support within Europe, in the US and in Japan.

### 12.2  ZMD

A²SI-L14 / A²SI-L16 device related application support requests can be addressed to asi@zmd.de

### 12.3  ZMD Application Support Partners

| ZMD Application Support Partners: | Bihl+Wiedemann | ICS Industrial Communication Solutions GmbH |
|---|---|---|
| | Flosswoerthstrasse 41<br>D-68199 Mannheim, Germany<br>Tel.: +49(0) 621 3 3996 0<br>Fax: +49(0) 621 3 3922 39<br>Email: mail@bihl-wiedemann.de<br>http://www.bihl-wiedemann.de | Hopfenstraße 1<br>D-88069 Tettnang, Germany<br>Tel: +49 (0) 7542 98 04 50<br>Fax: +49 (0) 7542 97 88 650<br>e-mail: info@ics-gmbh.com<br>http://www.ics-gmbh.com |

## 13  ZMD Sales Contacts

| For further information: | ZMD AG | ZMD America Inc. |
|---|---|---|
| | Grenzstrasse 28<br>01109 Dresden, Germany<br>Tel.: +49 (0)351.8822.366<br>Fax: +49 (0)351.8822.337<br>sales@zmd.de | 201 Old Country Road, Suite 204<br>Melville, NY 11747<br>Tel.: (631) 549-2666<br>Fax: (631) 549-2882<br>sensors@zmda.com |

## 14  ZMD Distribution Partners

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Fax:      +49 8121 775 592
E-mail: juergen.dudda@wbc-europe.com

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ZMD reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

# A²SI-Lite 14 / A²SI-Lite 16
Data Sheet
Low End Device AS-Interface IC

## Appendix A:  Crystal Parameter

### A.1 Parameter data of Crystal

Different crystals types are described in Table A-1. The models of those crystals are described in Table A-2.

*Table A-1: 16 MHz crystals*

| Symbol | Model | Maker | Size W* D* H (mm) | Operating Temperature Range (°C) |
|--------|-------|-------|-------------------|----------------------------------|
| A | LIM-T-16.000 | Kyusyu Dentsu Co. | 7.5*5.0*1.2 | -25 … +85 |
| B | LAP-16.000 | Kyusyu Dentsu Co. | 6.0*3.5*1.2 | -25 … +85 |
| C | SXN-A 16 MHz | Nippon Industries | 6.0*3.5*1.2 | -40 … +85 |
| D | SXH-A 16 MHz | Nippon Industries | 7.5*5.0*1.0 | -40 … +85 |
| E | DSX630G | Daishinku corp. | 6.0*3.5*1.2 | -25 … +85 |

*Table A-2: Crystal models*

| Symbol | L1 (mH) | | | C1 (fF) | | | R1 (Ohm) | | | C0 (pF) | | | CL (pF) | | |
|--------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 6.7 | 7.9 | 9.1 | 9.0 | 10.6 | 12.2 | - | - | 60.0 | 2.4 | 2.9 | 3.3 | 12.0 | 16.0 | 20.0 |
| B | 7.9 | 9.3 | 10.7 | 9.0 | 10.6 | 12.2 | - | - | 60.0 | 2.4 | 2.9 | 3.3 | 12.0 | 16.0 | 20.0 |
| C | 7.9 | 9.3 | 10.7 | 9.0 | 10.6 | 12.2 | - | 10.0 | 60.0 | 2.4 | 2.9 | 3.3 | 8.0 | - | 32.0 |
| D | 6.7 | 7.9 | 9.1 | 9.0 | 10.6 | 12.2 | - | 10.0 | 60.0 | 2.4 | 2.9 | 3.3 | 8.0 | - | 32.0 |
| E | 14.1 | 16.6 | 19.1 | 5.1 | 6.0 | 6.9 | 10.0 | 50.0 | - | 1.8 | 2.1 | 2.4 | 12.0 | - | 20.0 |

Note: A crystal is fabricated for a dedicated load capacitor. This load capacitor CL is equivalent to the sum of CL' (internal oscillator circuit capacitor) and the parasitic capacitor CP (capacity that is caused by the PCB, e.g. by copper areas and wires on the PCB).
Figure A-1 shows an equivalent circuit of the crystal oscillator that should illustrate the modeling method.
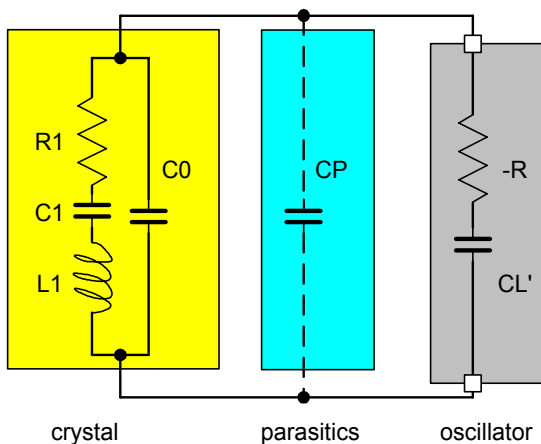
### A.2 Capacitance on PCB



*Figure A-1: Crystal oscillator equivalent circuit*

# Appendix B:  External Coil

### B.1 Target Coil

In order to satisfy the Complete Specification AS-interface an application circuit has to achieve a certain input impedance. Besides the A²SI-L IC properties the applied external coil will have an significant influence. Therefore a suitable coil shall be recommended. During the product development period recommended data of this coil have to be worked out. The following coil is considered as target component and shall be applied (between ASIP and VIN, refer to Figure 9-1 and Figure 9-2, respectively) as long no other recommendation has been made:

Coil No, SD75-183k
Core No, M5D DR7.8*5.0 DIM
Maker EASY MAGNET Corp. http://www.easymagnet.com.tw
Inductance: 18mH +-10% (f=1kHz Ambient Temperature : 20'C DC Bias 0A)
DC resistance : Max 72.0 ohm ( Ambient Temperature :20'C DC Bias 0A)
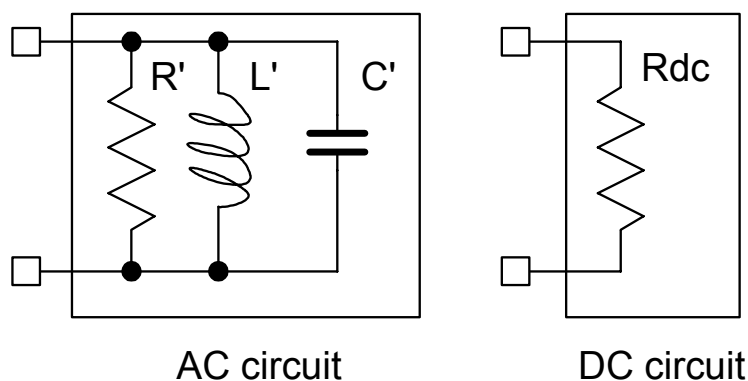
### B.2  Coil Modeling



*Figure B-1: External Coil equivalent circuits*

Figure B-1 shows the model parameters that will be used in order to recommend suitable external coils. Until the end of the development process the following parameters have shall be recommended by ZMD:

L' : Real value of Inductance
C' : Parasitic capacitor
R' : AC Resistance
Rdc : DC Resistance
Measurement frequency : 50k...300kHz C' R' L'

### B.3  Electronic Inductor

ZMD provides an optional application (see separate application note) for a bipolar (GND free) electronic inductor* to replace a mechanical coil with some inexpensive electronic parts. This solution save costs, board space and will be more resistant against mechanical vibrations. This inductor provides a supply current up to 90mA to Vin and the connected circuit, respectively.

ZMD AG provides a license  to ZMD AS-Interface IC customers free of charge.

* patent pending

# A²SI-Lite 14 / A²SI-Lite 16
Data Sheet
Low End Device AS-Interface IC

For further information, please contact:

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01109 Dresden,Germany
asi@zmd.de

## Appendix C:  EEPROM

*Table C-1: Contents of the A²SI-L14 / A²SI-L16 EEPROM*

| EEPROM Address | Bit Position | EEPROM Cell Content | EEPROM Register Content |
|---|---|---|---|
| 0x0 | 0 ... 3 | A0 ... A3 | Slave Address low nibble |
| 0x1 | 0 | A4 | Slave Address high nibble |
| 0x1 | 1 ... 3 | (not useable) | none |
| 0x2 | 0 ... 3 | ID1_0 ... ID1_3 | ID code extension 1 |
| 0x3 | 0 ... 3 | Not implemented - do not access | |
| 0x4 ... 0x7 | 0 ... 3 | Not implemented - do not access | |
| 0x8 | 0 ... 3 | ID_0 ... ID_3 | ID code |
| 0x9 | 0 ... 3 | ID2_0 ... ID2_3 | ID code extension 2 |
| 0xA | 0 ... 3 | IO_0 ... IO_3 | IO code |
| 0xB | 0 | PWM_enable | Configuration Flags |
| 0xB | 1 | PWM_32k_mode | |
| 0xB | 2 | Reserved | |
| 0xB | 3 | Reserved | |
| 0xC | 0 | FID_Disable | Configuration Flags |
| 0xC | 1 | Program_Mode_Disable | |
| 0xC | 2 | Watchdog_Active | |
| 0xC | 3 | Invert_Data_In | |
| 0xD | 0 ... 3 | Not implemented - do not access | |
| 0xE | 0 ... 3 | Trimm Information, do not access | |
| 0xF | 0 ... 3 | Trimm Information, do not access | |